# Simulation guide, ece145C/218C
# Problem set 2

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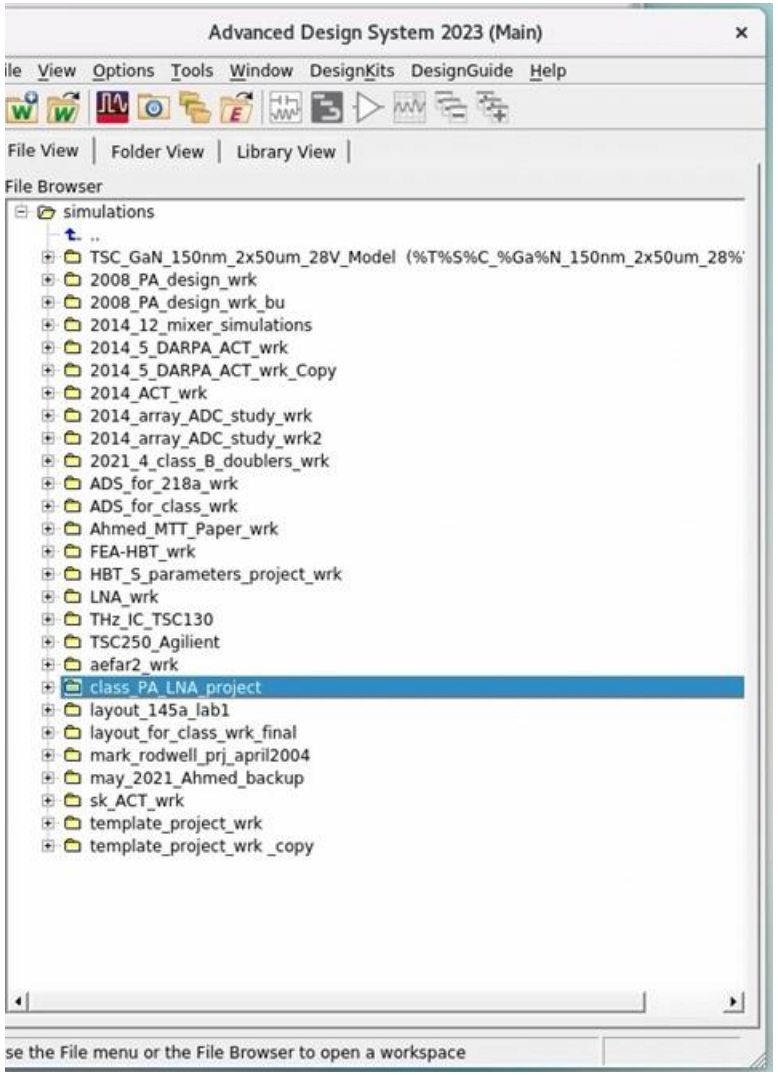
# Simulation directory

from the class web site download the archived ADS directory class_PA_LNA_project

Unarchive it, and open it.

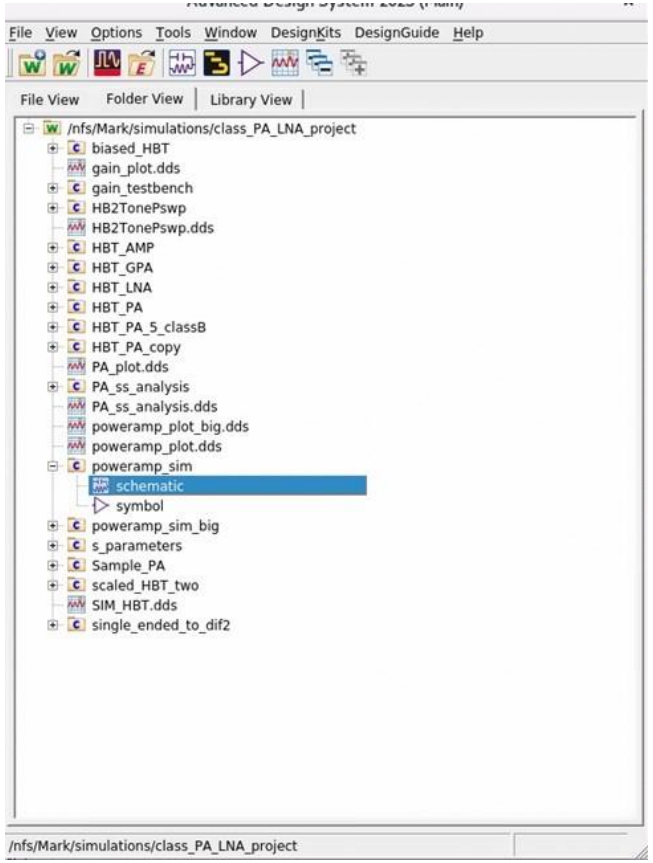


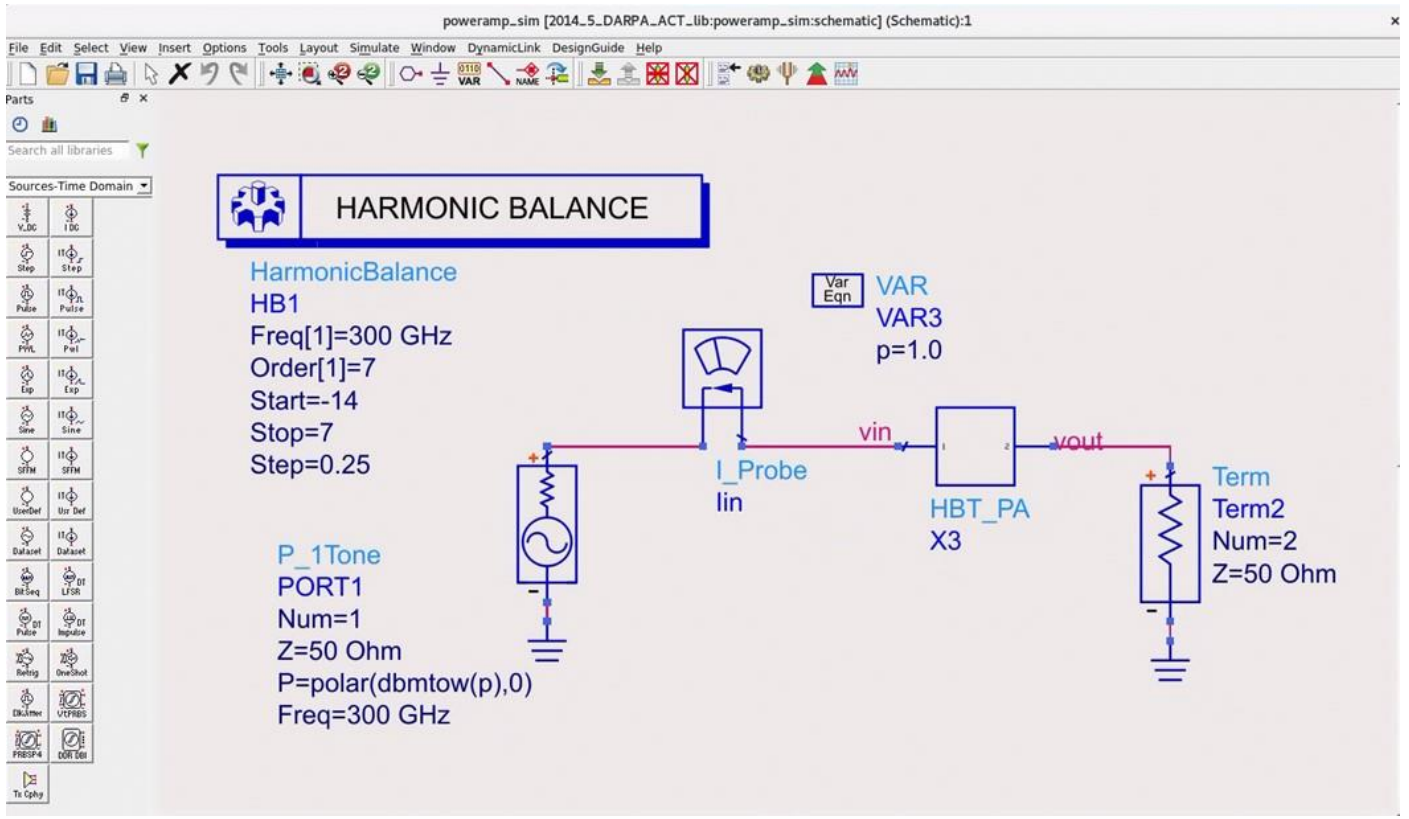
# Power Amplifier Simulation

start by opening the simulation file poweramp_sim

This is presently set up to simulate a 300 gigahertz power amplifier design called HBT_PA

The simulation mode is called harmonic balance: This is a large signal but frequency domain means of simulation. You might want to read the online ads documentation about it



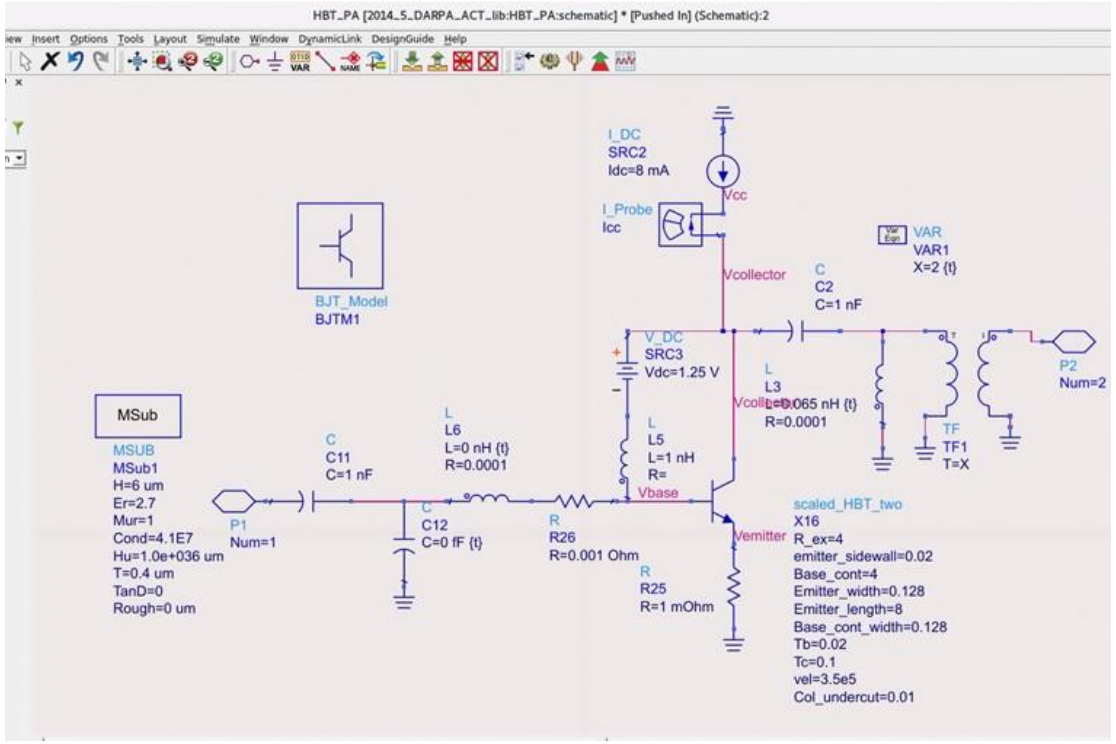



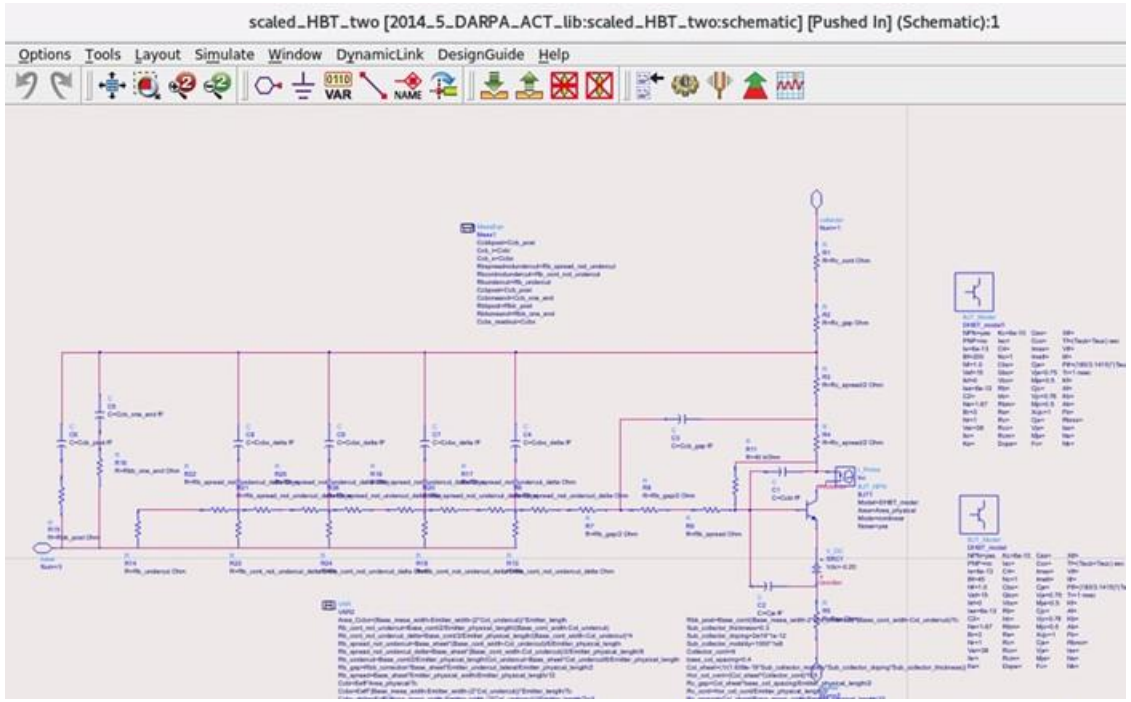
# Circuit and device models

On the left is the circuit diagram on the right is the transistor model.

In this particular example I am using a ucsb built model of a high frequency bipolar transistor. This allows me to place the current meter in the correct place without resorting to the negative capacitance tricks discussed in the notes.

In the circuit note that I am using the ideal output tuning network described in the lecture notes, and I'm using a bias network that is convenient for simulation but that could never be used in a real circuit



# power amplifier simulation

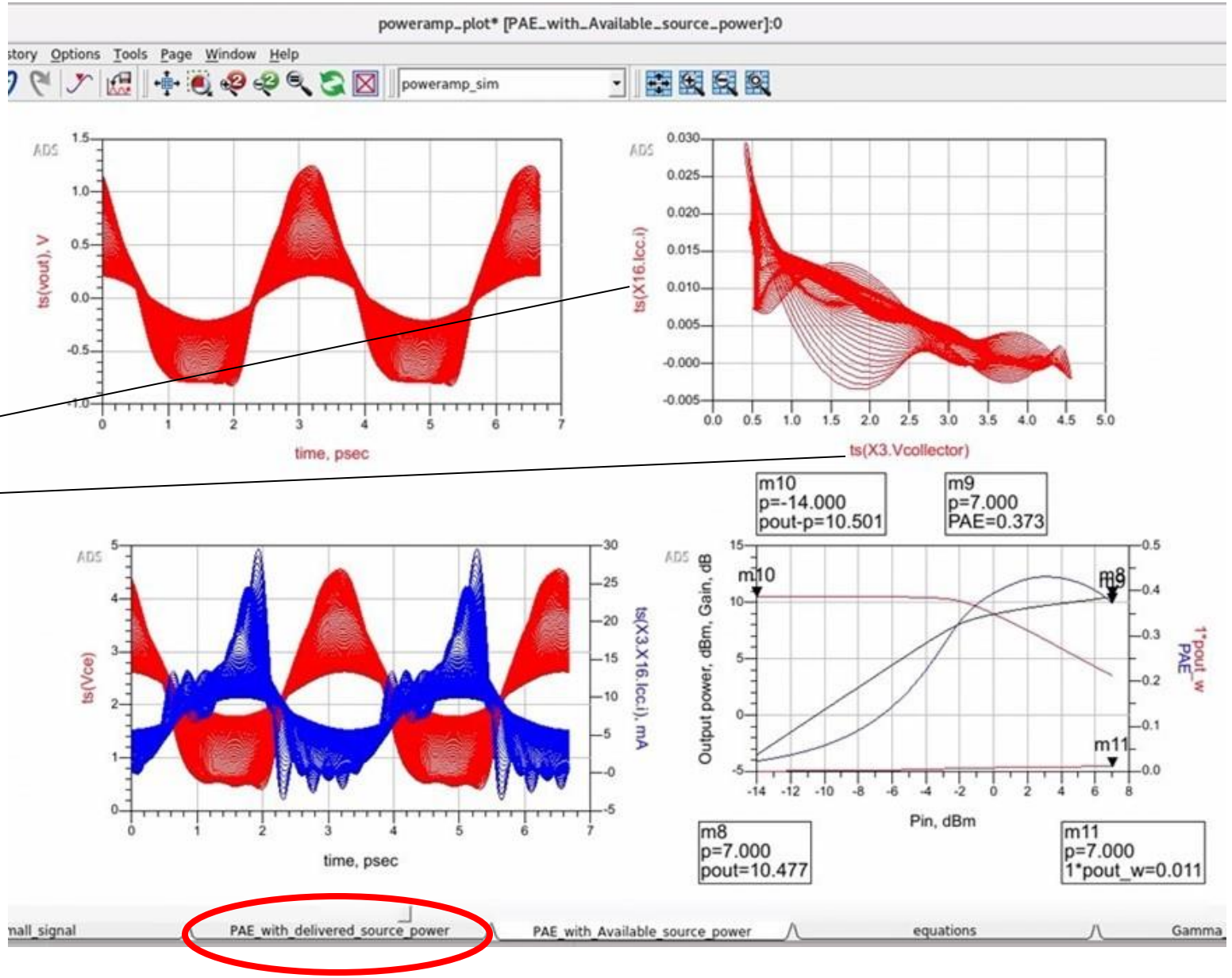
The load tuning procedure is described in the notes.

here I'm showing you the resulting design after the load is correctly tuned.

This display window computes gains with the delivered source power, Not the available source power, because the input matching network hasn't been designed yet

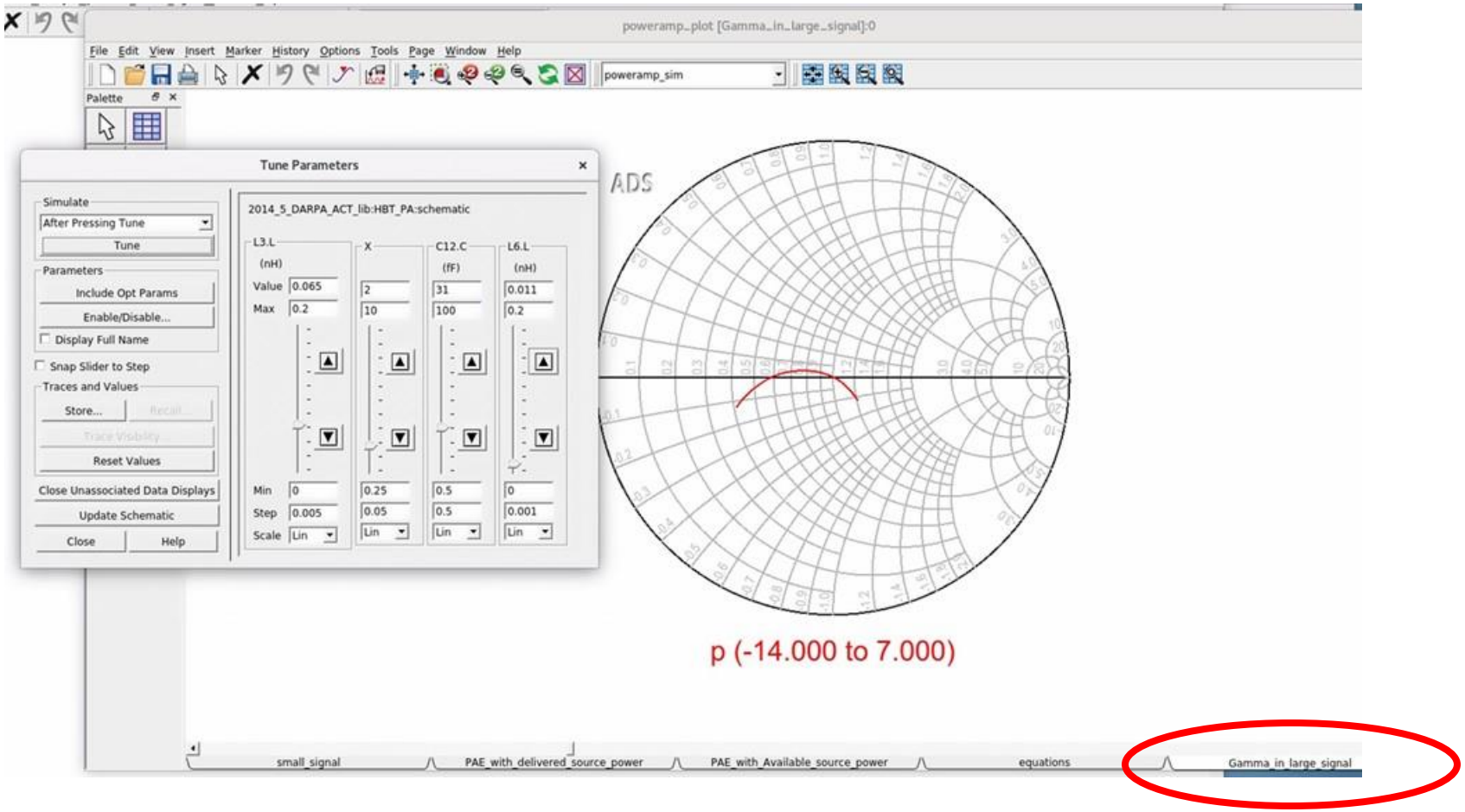
this is the collector current

this is Vce



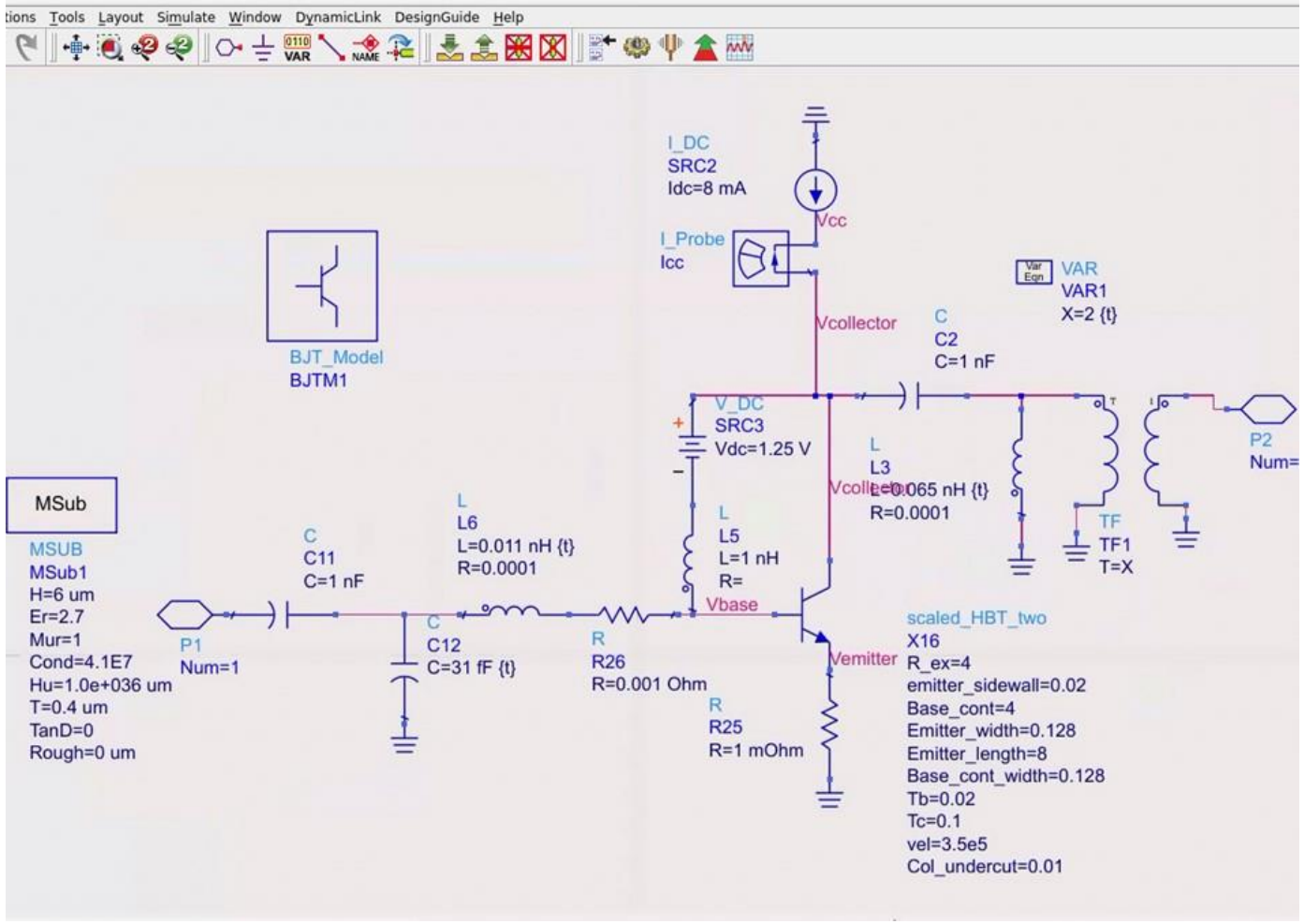
# tuning the input network

I've used the tab called  "Gamma_in_large_signal" To tune the input network to obtain a good large signal input match.



# tuning the input network

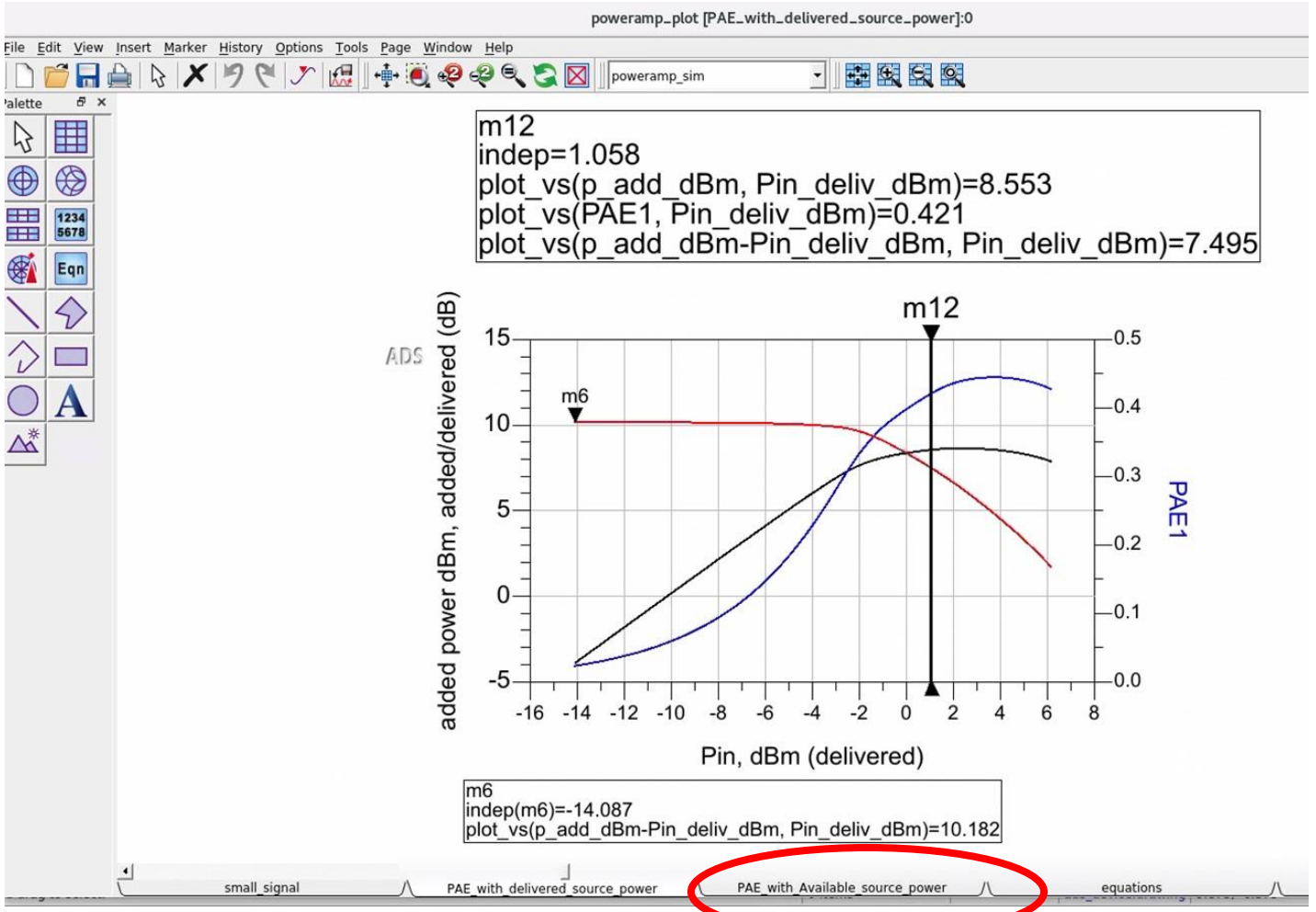
Here's the resulting overall circuit including the input matching network



# tuning the input network

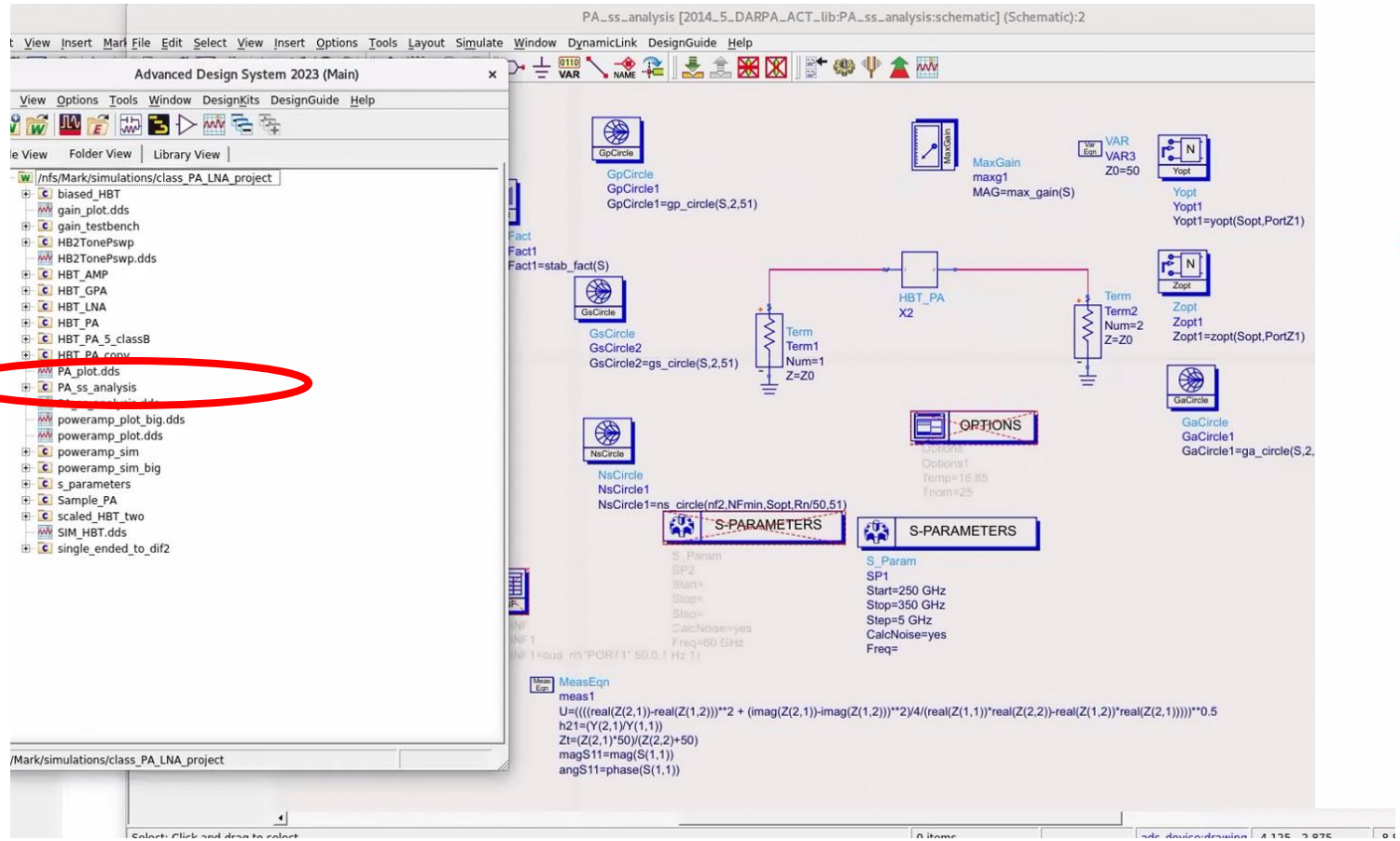
And now with the input correctly tuned here's the gain in efficiency as a function of the available source power

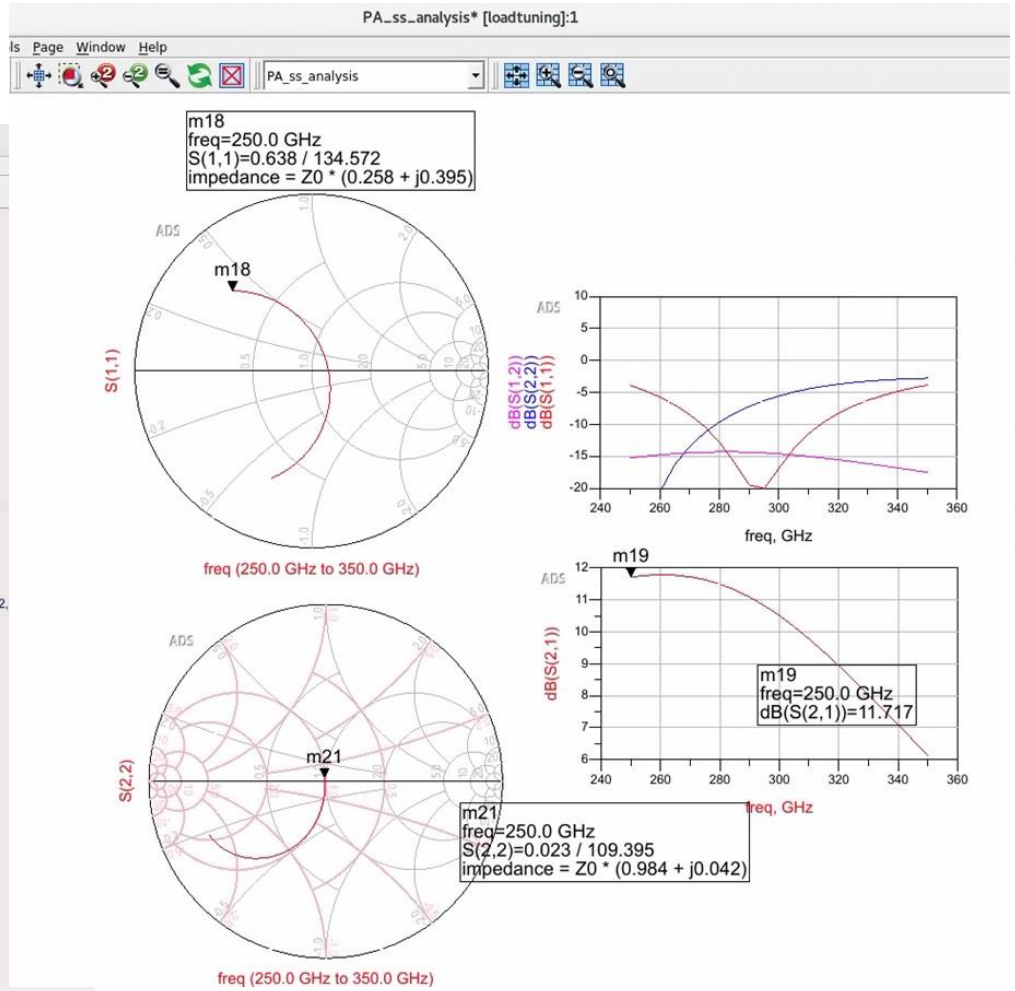
To make these utilities work with your circuits you may need to go to the equations tab to redefine variables



# Small signal gain frequency simulation

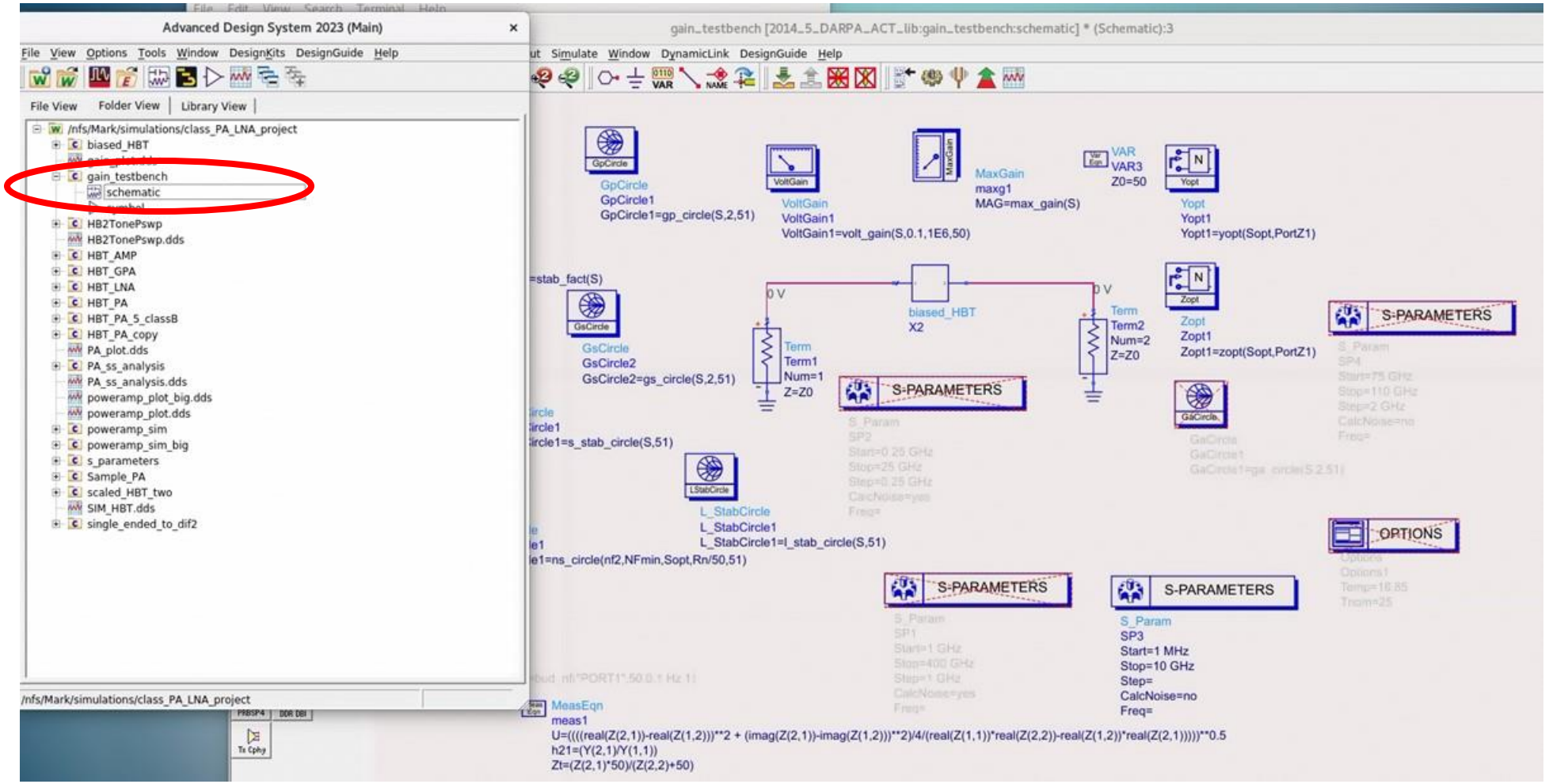
I can now open up the file PA_ss_analysis To simulate the small signal gain frequency characteristics of the circuit



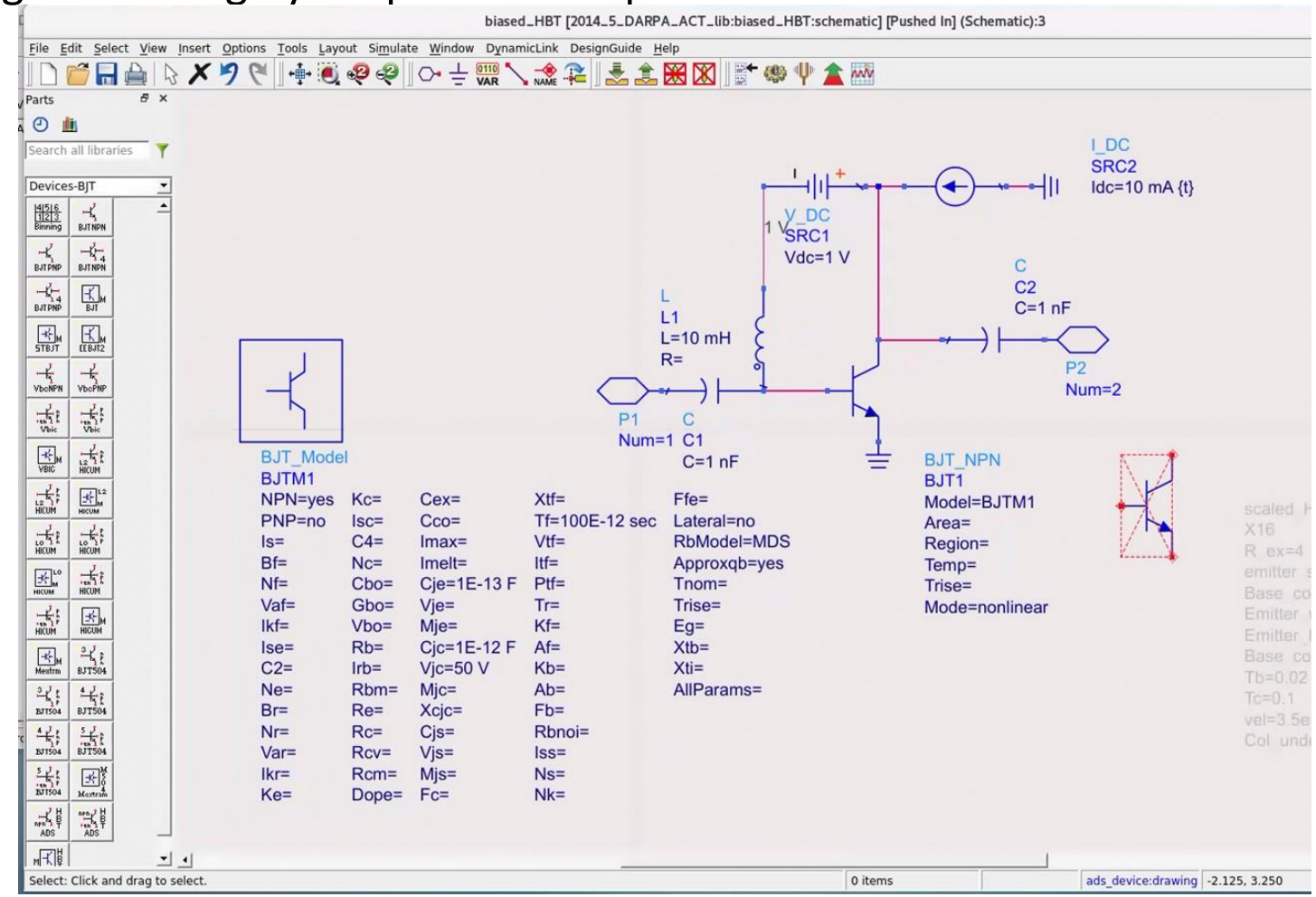
# Modeling a transistor without a built in ammeter

Let's open up the file called gain_testbench



# Modeling a transistor without a built in ammeter

You would place here the transistor you are working with, probably an mrf 901. Since I don't have that installed on my computer I've instead created a fake transistor, highly idealized, with infinite current gain, 100 picoseconds for transit time, Cje=0.1 pF, and Cjc=1 pF. I've made both the capacitances independent of voltage in this highly simplified example



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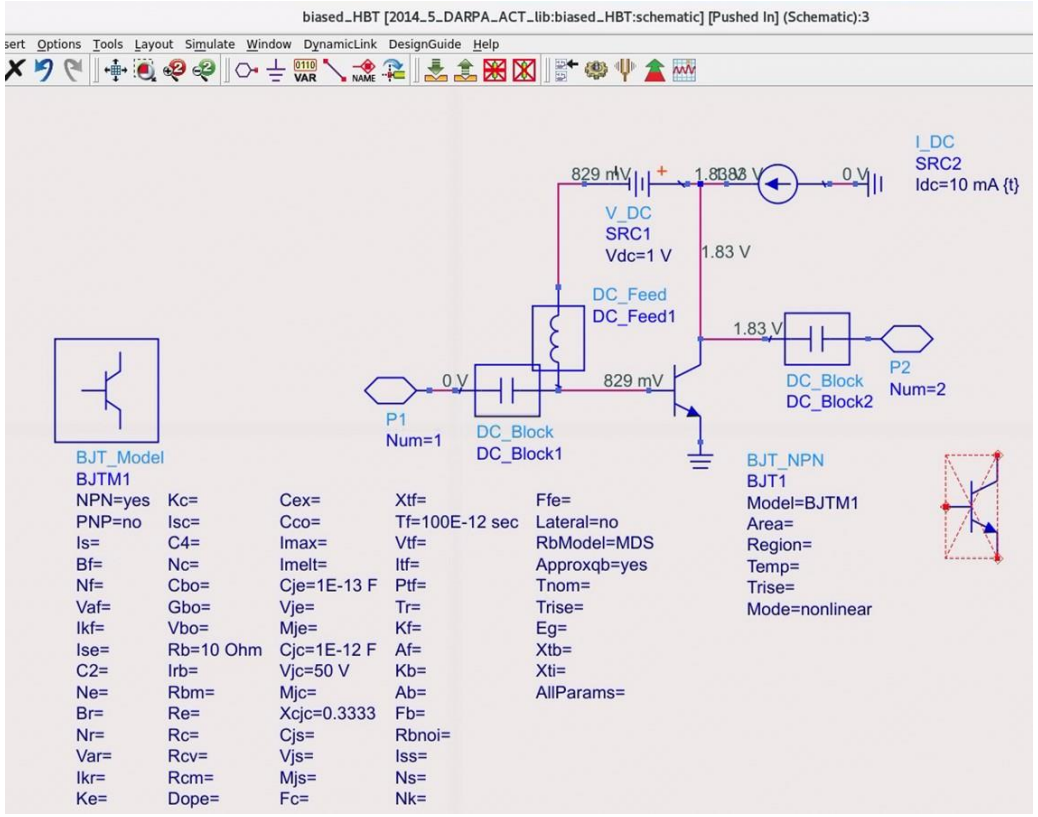
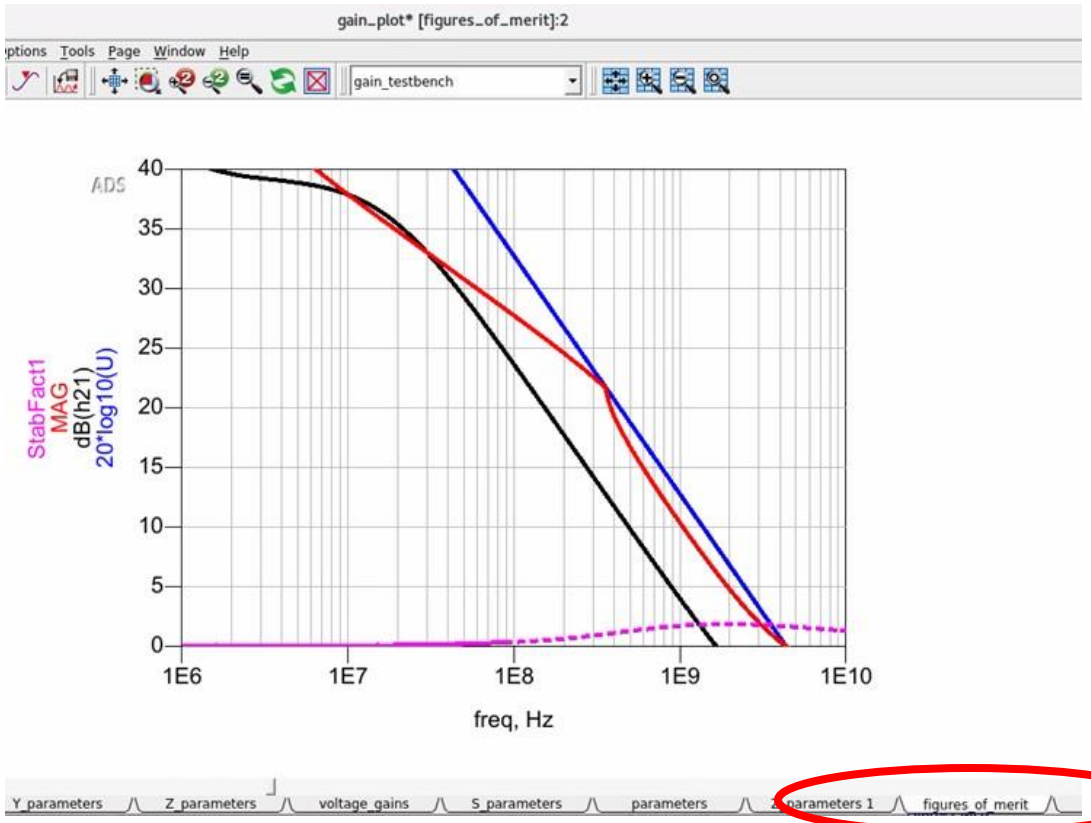
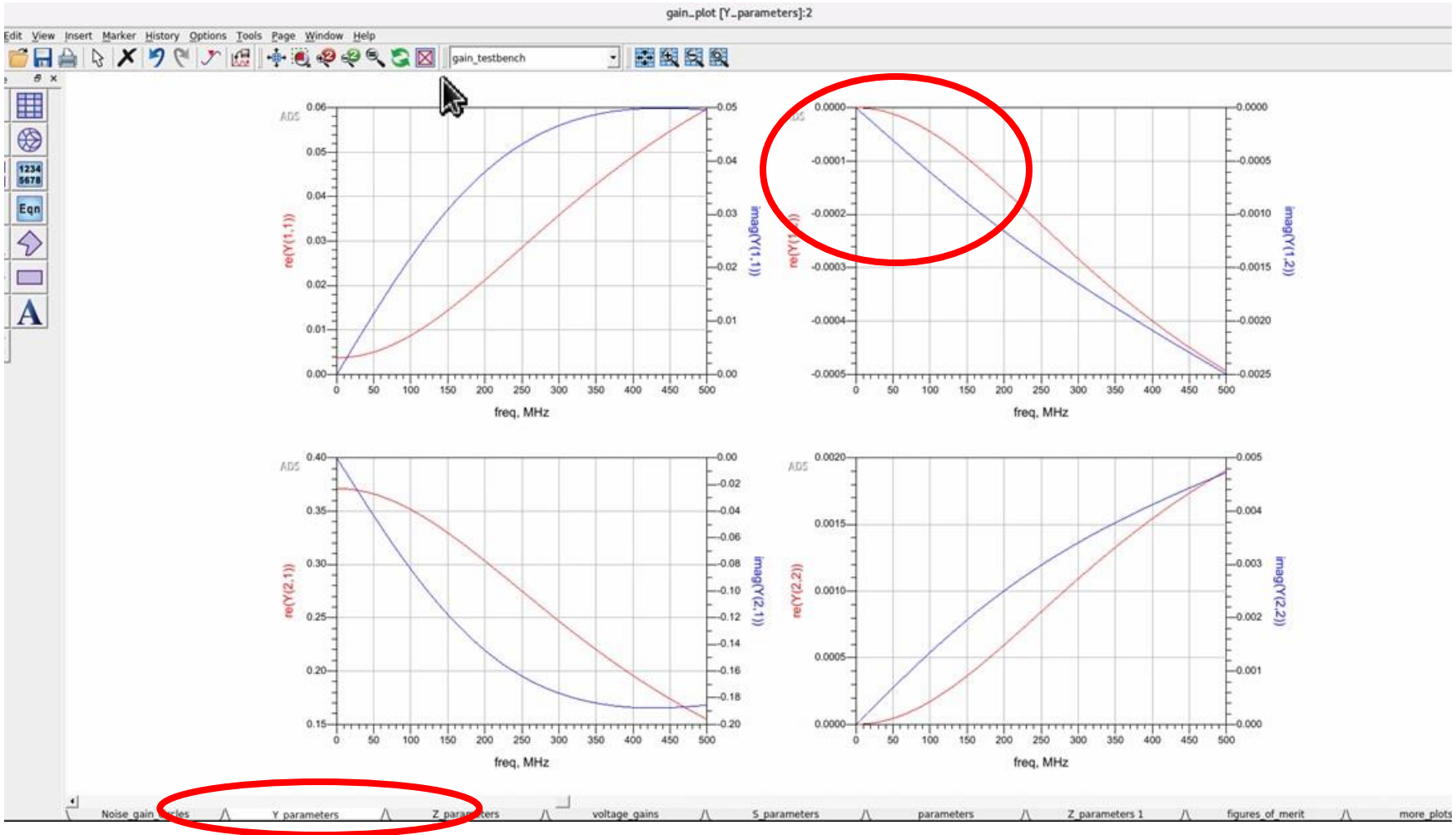
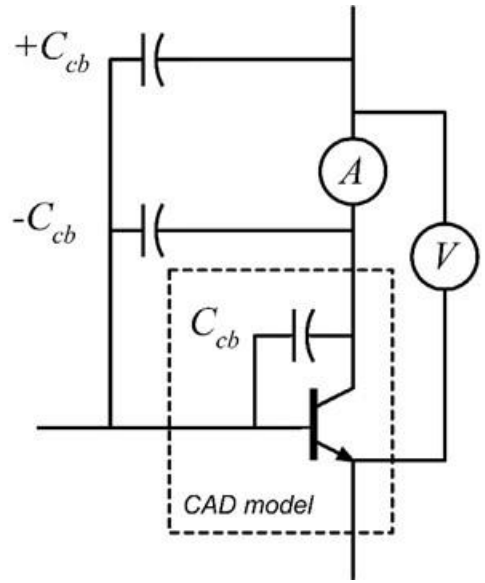


# Modeling a transistor without a built in ammeter

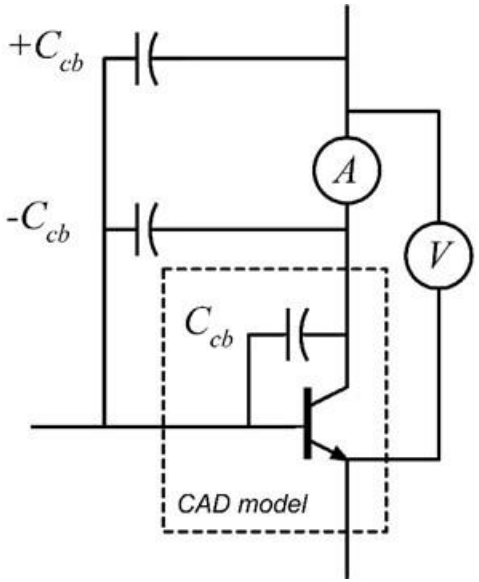
I now narrow the frequency range of simulation to something well below the transistor cutoff frequencies
I then use the value of the slope of Im(Y12) to determine the value of the transistor Ccb
One can then correctly place the ammeter for power amplifier simulations as was discussed in the notes.

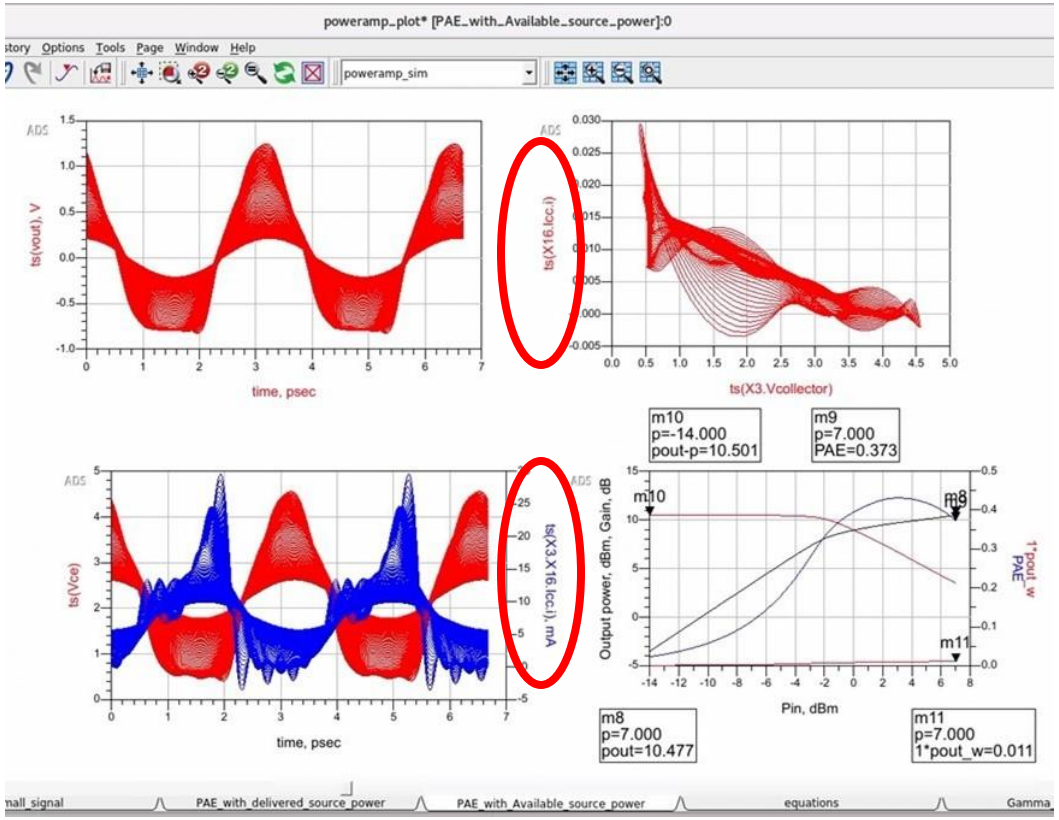


# Modeling a transistor without a built in ammeter

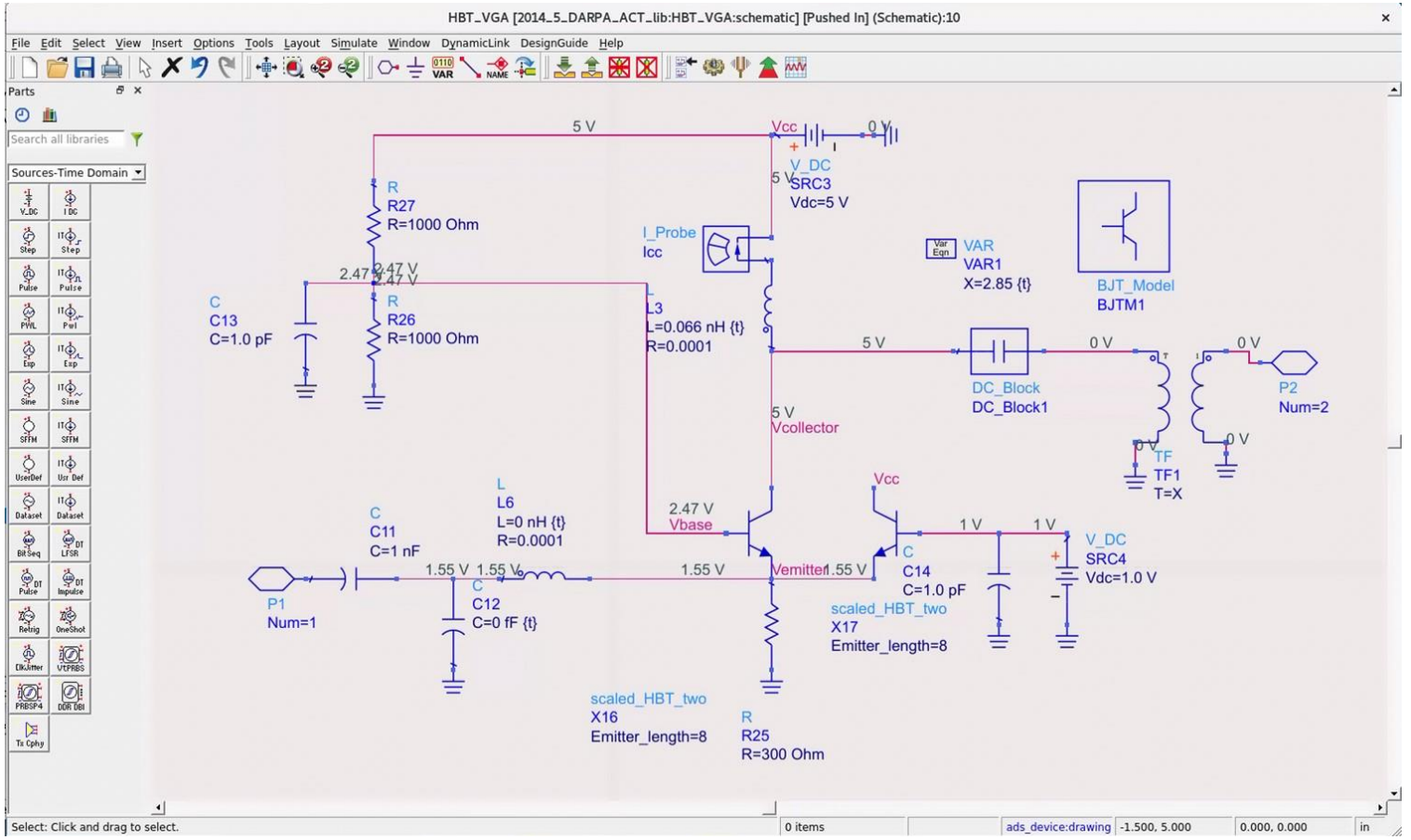
Note that you will have to edit the graphs in the power amplifier plot window file to point to the current meter you are using



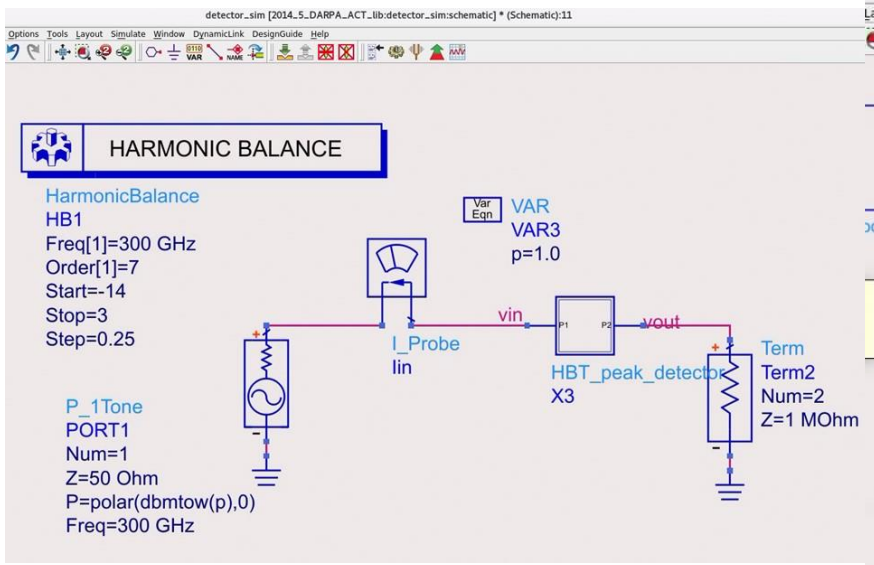
# Simulating a variable gain amplifier

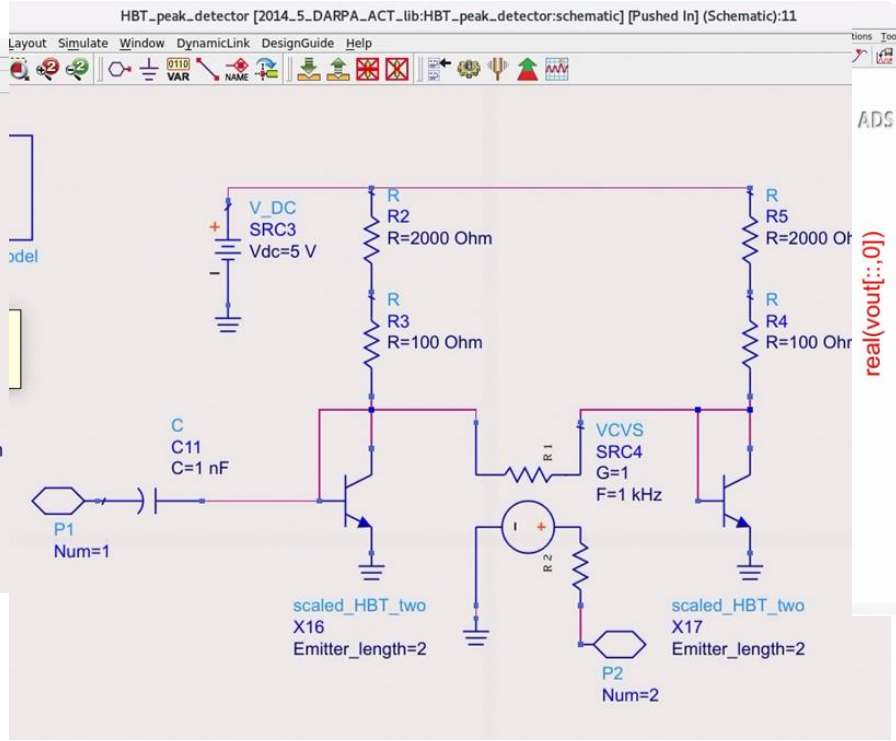
I have created an amplifier file called  HBT_VGA. You will need to change the design frequency to 915 MHz, to replace the transistors with MRF901 models, And to replace the ideal components with real ones.  First, with SRC4 set so that the right transistor is off, Follow the design procedure to design the circuit as if it was a power amplifier, following the procedure on slides 1-14. You can then vary src for and observe the gain and output power characteristics vary as you vary this control voltage

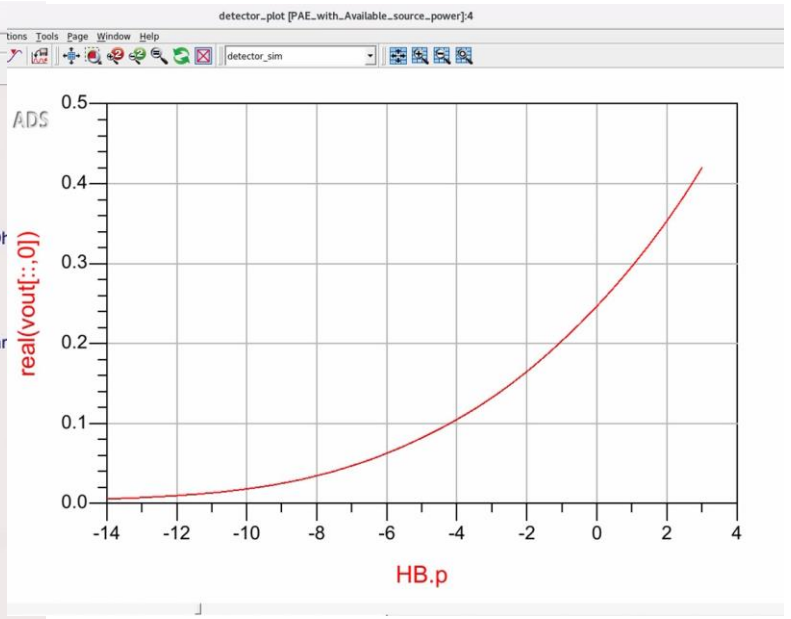


# Simulating the peak detector

I have created files called detector_sim, HBT_peak_detector, and detector_plot which allow you to simulate and plot the relationship between available source power and DC output voltage of the peak detector. The right plot shows output voltage in V vs. available source power in dBm. You will of course have to change the frequency range the element values and possibly the circuit topology to represent the problem you are working in the problem set

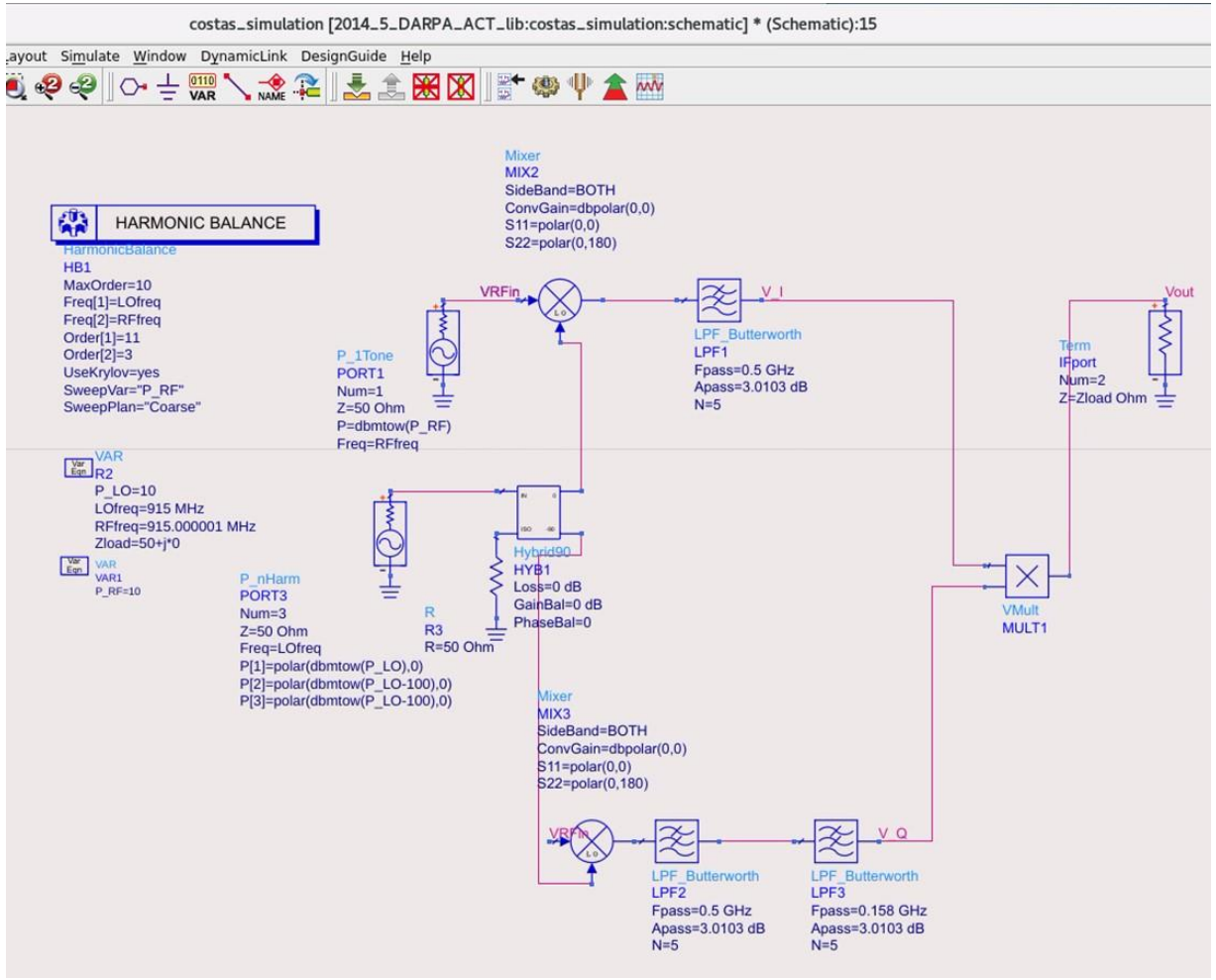


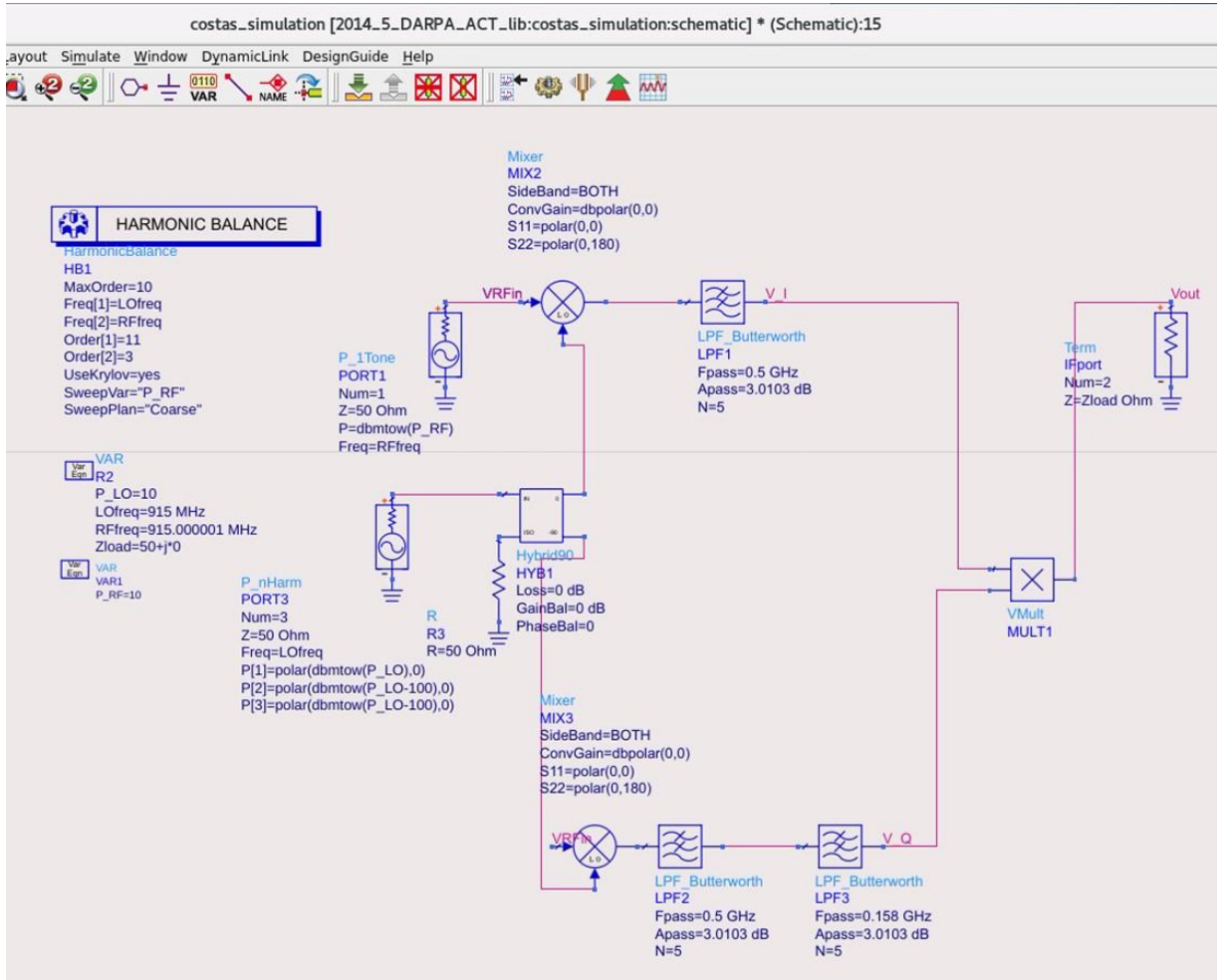
# Simulating the phase frequency difference detector

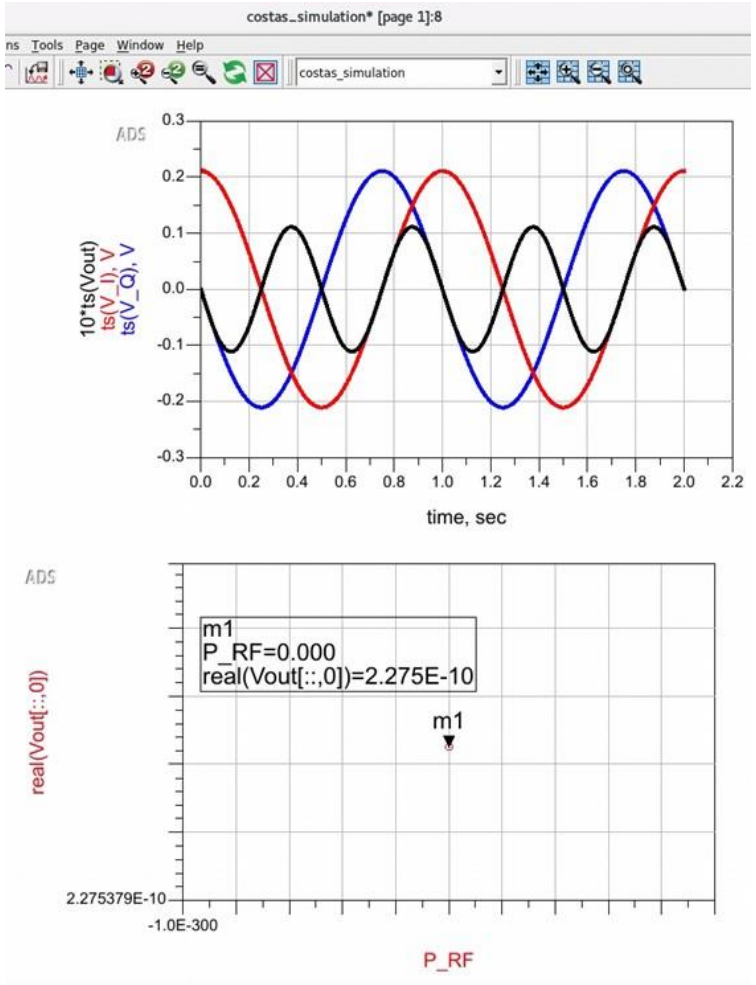
Here is a template for simulating the phase frequency difference detector. It uses ideal mixer and filter models. LPF1 and LPF2 Are just to suppress the harmonics of 915 MHz. LPF3 Is the delay in the phase frequency detector. VMULT Is an ideal voltage multiplier which you must replace with your actual transistor circuit.



# Simulating the phase frequency difference detector

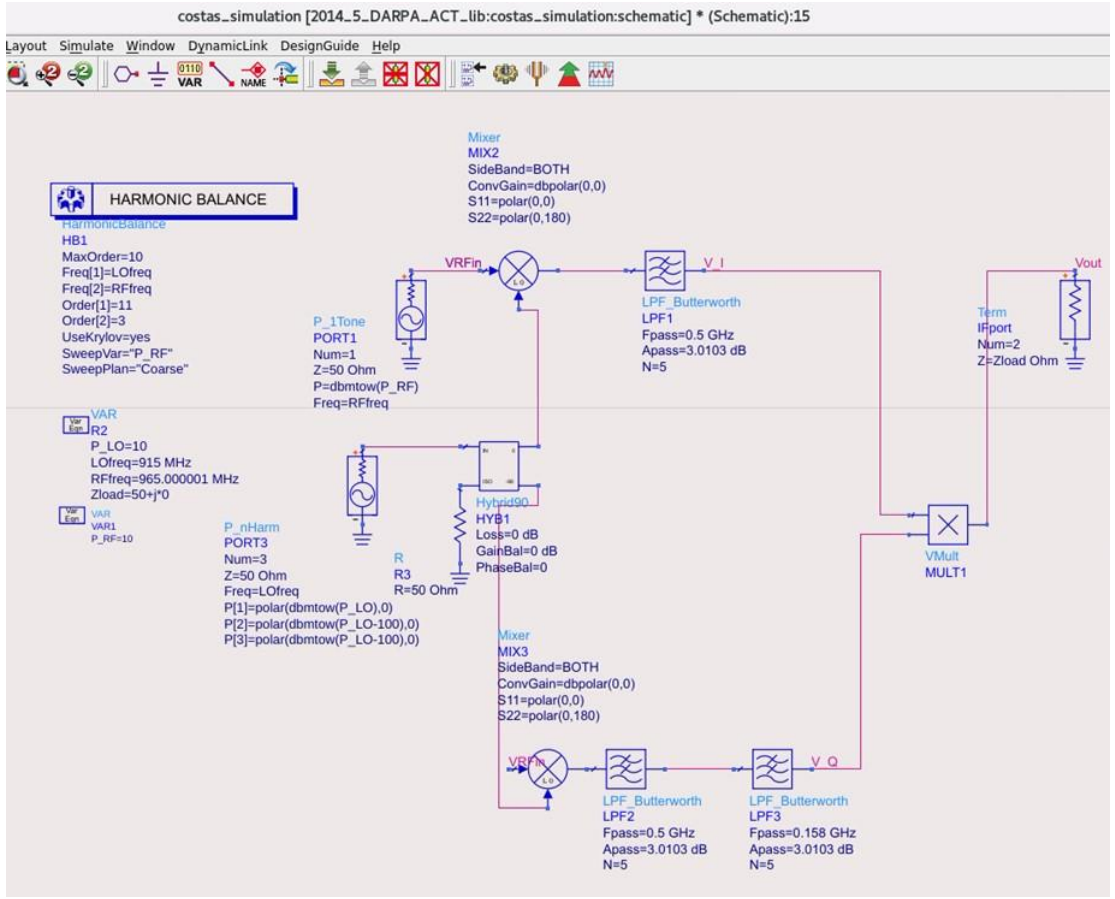
with a 1 Hz offset between the RF and LO frequencies, the output is 10 mV*sin(2*Pi*1 Hz*t).
K_detector can be calculated from this
Note that the dc output of the detector is in the range of ten to the minus ten volts

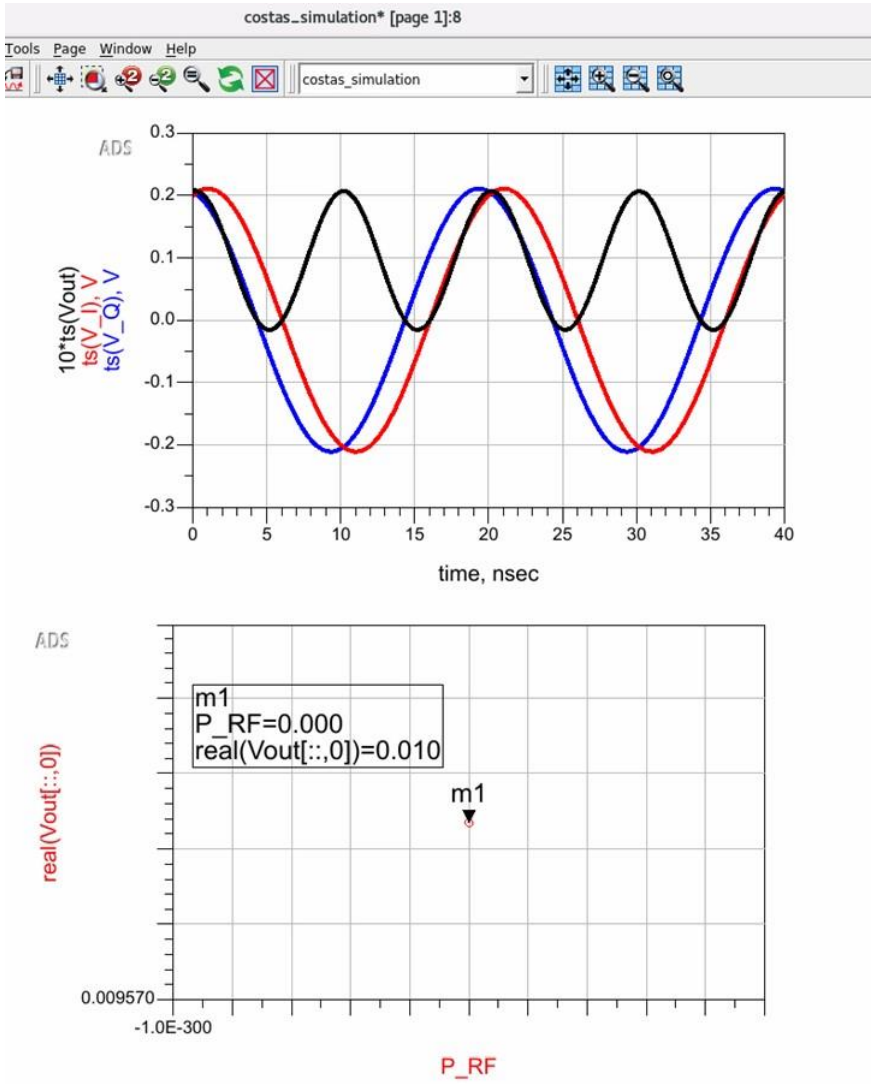


# Simulating the phase frequency difference detector

with a 50 MHz offset between the RF and LO frequencies, the output is 10 mV*cos(2*Pi*1 Hz*t)+10 mV.
K_detector can be calculated from this
Note that the dc output of the detector is 10mV



# Simulating the phase frequency difference detector

It is clear that I must give you further guidance on how to design this for your lab project.
You must replace the ideal voltage multiplier with your actual transistor circuit.
We must decide the PLL Loop bandwidth.
The maximum range of the frequency difference detector should be about ten times that.
That will determine the appropriate delay for the delay line filter. And consequently its bandwidth.
We must put a voltage limiter on the tuning voltage for the voltage controlled oscillator so that it can't tune outside the frequency range of the frequency difference detector.

Finally we must make sure that the sign of phase detection end of frequency detection are the same so that the loop locks properly