Performance Analysis of Carbon Nanotube Interconnects for VLSI Applications

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Abstract

The work in this paper analyses the applicability of carbon nanotube (CNT) bundles as interconnects for VLSI circuits, while taking into account the practical limitations in this technology. A model is developed to calculate equivalent circuit parameters for a CNT-bundle interconnect based on interconnect geometry. Using this model, the performance of CNT-bundle interconnects (at local, intermediate and global levels) is compared to copper wires of the future. It is shown that CNT bundles can outperform copper for long intermediate and global interconnects, and can be engineered to compete with copper for local level interconnects. The technological requirements necessary to make CNT bundles viable as future interconnects are also laid out.

1. Introduction

The resistance of copper interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu at room temperature) in current and imminent technologies [1], is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of the highly resistive diffusion barrier layer [2]. The steep rise in parasitic resistance of copper interconnects poses serious challenges for interconnect delay [1] (especially at the global level where wires traverse long distances) and for interconnect reliability [3], hence it has a significant impact on the performance and reliability of VLSI circuits.

In order to alleviate such problems, changes in the material used for on-chip interconnections have been sought even in earlier technology generations, for example the transition from aluminum to copper some years back. Carbon nanotubes have recently been proposed as a possible replacement for metal interconnects in future technologies [4, 5]. Carbon nanotubes (CNTs) are graphene sheets rolled up into cylinders with diameter of the order of a nanometer. Depending on the direction in which CNTs are rolled up (chirality), they demonstrate either metallic or semi-conducting properties (see **Fig. 1(a)**). Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [6, 7, 8], CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. However, the high resistance associated with an isolated CNT (greater than 6.45 KΩ) [9] necessitates the use of a bundle (rope) of CNTs conducting current in parallel to form an interconnection [4, 5]. Moreover, due to the lack of control on chirality, any bundle of CNTs consists of metallic as well as semi-conducting nanotubes (the semi-conducting CNTs do not contribute to current conduction in an interconnect). CNTs are also classified into single-walled and multi-walled (comprising multiple concentric cylindrical shells) nanotubes. Although multi-walled CNTs (MWCNTs) are predominantly metallic, it is difficult to achieve ballistic transport over long lengths with them [10, 11]. Single-walled CNTs (SWCNTs) on the other hand have electron mean free paths of the order of a micron [9]. Hence, in the domain of interconnects, metallic SWCNTs are the preferred candidates. The scope of this work is limited to such bundles of single-walled carbon nanotubes that are best suited for interconnect applications.

Carbon nanotube bundle structures have recently been demonstrated and their metallic conducting properties reported in the literature [4, 12, 13, 14]. **Fig. 1(b-d)** shows different strategies reported in the literature that can potentially be used for forming interconnects and vias using carbon nanotube bundles. As research in the processing of carbon nanotube interconnects progresses, the performance of this novel technology needs to be evaluated vis-à-vis copper in order to ascertain whether they can be feasible alternatives to copper interconnects.

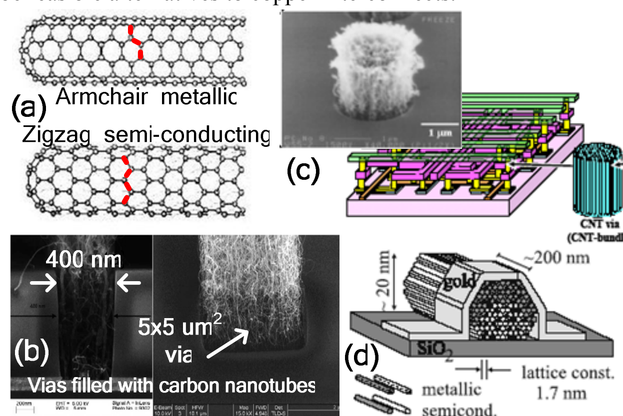

Figure 1: (a) Different configurations and resulting electrical conduction types of carbon nanotubes depending on the direction along which the graphene sheets are rolled up (chirality) [9]. (b-d) Strategies to form interconnects and vias using carbon nanotube bundles (b: [4], c: [14], d: [15]).

While it has been shown that FETs made of carbon nanotubes can be competitive with Si FETs in the sub-20 nm gate length regime [16], there are few works so far that examine the practical applicability of CNT bundles as interconnects in VLSI circuits. These initial works, discussed in the following section, provide a very simplified analysis of CNT interconnections vis-à-vis copper and do not consider the capabilities or practical limitations of this emerging technology. Hence there is a pressing need for a realistic and complete performance analysis of CNT bundle interconnects as part of a VLSI circuit that takes into account their advantages as well as the practical limitations (such as imperfect contact resistances and the lack of control on chirality) that naturally accompany them. There is also a need to identify the domains of on-chip interconnections (local, intermediate or global) where this novel interconnect technology is most suited to replace copper. Finally, there is a need to lay out the requirements for processing technology in order to make CNT bundles the interconnection material of choice in the near or distant future.

This work is aimed at filling these gaps in the existing literature. A comprehensive analysis of the performance of CNT bundle VLSI interconnects vis-à-vis copper interconnects is per-

formed in a detailed and realistic manner for the first time. This analysis is used to identify the parameters in CNT bundle interconnects that can be exploited to derive maximum benefit from them as well as those that give rise to major limitations in their applicability as interconnects.

The paper is organized as follows. The following Section 2 describes the equivalent circuit model for a CNT that is useful in the performance analysis of CNT-bundle interconnects and discusses existing work in the literature that compare CNT interconnects with copper. Section 3 presents a detailed discussion of the derivation of equivalent circuit parameters for a CNT bundle interconnect and describes the models used for evaluating interconnect performance. The results of the analysis are presented in Section 4 and the lessons learned are summarized in Section 5.

2. Background and Previous Work

2.1 Resistivity Increase in Cu Interconnects

The resistivity of wires with dimensions in the range of, or less than, the mean free path of metal (copper: 40 nm at room temperature) has been modeled and experimentally verified on sub-100 nm copper wires [2]. The resistivity model is based on the Fuchs-Sondheimer model for surface scattering of electrons (Eq. 1) and the theory of Mayadas and Shatzkes for the scattering of electrons at grain boundaries (Eqs. 2 and 3) [2]. Here ρ_0 is resistivity of the bulk material, p is the fraction of electrons scattered specularly at the surface, d is width of the wire, l is mean free path, R is the reflectivity coefficient that denotes the fraction of electrons that are not scattered by the potential barrier at a grain boundary, and d' is the average distance between grain boundaries.

$$\frac{\rho}{\rho_0} = 1 + \frac{3}{4}(1-p)\frac{l}{d} \tag{1}$$

$$\frac{\rho_0}{\rho} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right] \tag{2}$$

$$\alpha = \frac{l}{d'}\frac{R}{1-R} \tag{3}$$

The combined effects of these phenomena, along with the presence of a finite diffusion barrier layer that is needed for copper interconnects and reduces the effective copper conducting area, cause a sharp rise in the resistivity of interconnects when dimensions are of the order of the mean free path of electrons. **Fig. 2** shows the values of Cu resistivity at sub-90 nm technology nodes when these effects are taken into account. It can be observed that the resistivity of Cu increases many times over its bulk value of 1.9 μΩ-cm. The values p=0.6 and R=0.5 are used in these calculations as reported in [2] based on experimental observations.

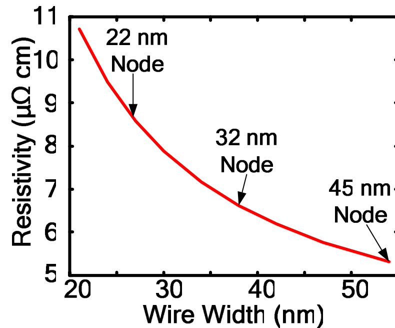

Figure 2: Cu interconnect resistivity as a result of barrier scattering, grain boundary scattering and finite barrier layer thickness (at 120°C).

2.2 Equivalent Circuit Model for an Isolated Single Walled Carbon Nanotube (SWCNT)

The equivalent circuit model for an isolated single-walled carbon nanotube [17] is shown schematically in **Fig. 3**. The model and its components are explained in detail in the following subsections.

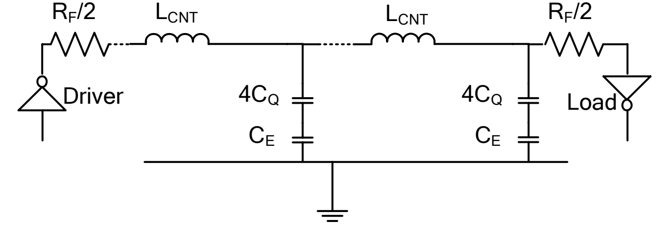

Figure 3: Equivalent circuit model [17] for an isolated SWCNT, length less than the mean free path of electrons, assuming ideal contacts.

<u>**Resistance of an Isolated SWCNT**</u>

The conductance of a carbon nanotube is evaluated using the two-terminal Landauer-Buttiker formula. This formula states that, for a 1-D system with N channels in parallel, the conductance $G=(Ne^2/h)T$, where T is the transmission coefficient for electrons through the sample [9]. Due to spin degeneracy and sublattice degeneracy of electrons in graphene, each nanotube has four conducting channels in parallel ($N=4$). Hence the conductance of a single ballistic single-walled CNT (SWCNT) assuming perfect contacts ($T=1$), is given by $4e^2/h$ = 155 μS, which yields a resistance of 6.45 KΩ [9]. This is the fundamental resistance associated with a SWCNT that cannot be avoided [18]. As shown in **Fig. 3**, this fundamental resistance (R_F) is equally divided between the two contacts on either side of the nanotube.

$$R_F = \frac{h}{4e^2} \tag{4}$$

The mean free path of electrons (the distance across which no scattering occurs) in a CNT is typically 1 μm [9, 19, 20]. For CNT lengths less than 1 μm, electron transport is essentially ballistic within the nanotube and the resistance is independent of length (6.45 KΩ). However, for lengths greater than the mean free path, resistance increases with length as shown in Equation 5 [21], where L_0 is the mean free path and L is the length of the CNT. This has also been confirmed by experimental observations [15, 20]. In the equivalent circuit, this additional scattering resistance would appear as a distributed resistance per unit length to account for resistive losses along the CNT length.

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{L_0} \tag{5}$$

In practice, the observed d.c. resistance of a CNT (at low bias) is much higher than the resistance derived above. This is due to the presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance. As observed in [22], making a reliable contact to a CNT is very challenging, and the resistance arising from these imperfect contacts is often so high that it masks the observation of intrinsic transport properties. The observed resistance for CNTs has typically been in the range of 100 KΩ [22, 23], although in a few cases the lowest observed resistance has been seen to approach the theoretical limit of ~7 KΩ [23]. In the equivalent circuit, this additional imperfect contact resistance would appear in series with the fundamental resistance (R_F) divided equally among the two end contacts as shown for R_F.

An important consideration for conductance in nanotubes is its dependence on voltage bias. At high electric fields, current

through a nanotube saturates [24]. However, it can easily be shown that a low voltage bias is always applicable in the domain of VLSI interconnect applications, as has also been argued in [25]. In this bias range, the nanotubes display excellent ohmic behavior [24], hence the resistance models described above are valid.

The total resistance of a CNT is then expressed as the sum of resistances arising from the above three aspects: the fundamental one-dimensional system (CNT) contact resistance, scattering resistance and the imperfect metal-nanotube contact resistance. Evidently the resistance associated with an isolated CNT is too high for realizing an interconnection. Hence, a bundle/rope of CNTs is needed that has much lower effective resistance and may work effectively as an interconnection.

Capacitance of an Isolated SWCNT

The capacitance of a CNT arises from two sources. The *electrostatic capacitance* (C_E) is calculated by treating the CNT as a thin wire, with diameter '*d*', placed a distance '*y*' away from a ground plane, and is given by the formula in Equation 6 (C_E per unit length) [17] for $y>2d$. The quantities *y* and *d* are shown in **Fig. 4**. For $d=1\ nm$, $y=1\ \mu m$, $C_E \approx 30$ aF/um. This is the intrinsic plate capacitance of an isolated CNT.

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{6}$$

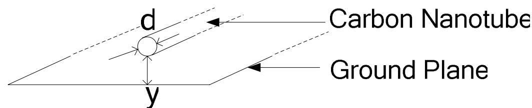

Figure 4: Isolated conductor, with diameter 'd', over a ground plane at a distance 'y' below it.

The *quantum capacitance* (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Due to the Pauli exclusion principle, it is only possible to add electrons into the nanotube at an available quantum state above the Fermi energy level. By equating this energy to an effective capacitance, the expression for the quantum capacitance (per unit length) is obtained as shown in Equation 7 [17], where *h* is the Planck's constant and v_F is the Fermi velocity. For a carbon nanotube ($v_F \approx 8\text{x}10^5$m/s), $C_Q \approx 100$aF/um [17].

$$C_Q = \frac{2e^2}{hv_F} \tag{7}$$

As a CNT has four conducting channels as described in the previous sub-section, the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$.

The same effective charge resides on both these capacitances (C_E and $4C_Q$) when the CNT carries current, as is true for any two capacitances in series. Hence these capacitances appear in series in the effective circuit model shown in **Fig. 3**.

Inductance of an Isolated SWCNT

The inductance associated with an isolated SWCNT can be calculated from the magnetic field of an isolated current carrying wire some distance away from a ground plane, as depicted in **Fig. 4**. In addition to this *magnetic inductance* (L_M), the *kinetic inductance* is calculated in [17] (following [26]) by equating the kinetic energy stored in each conducting channel of the CNT to an effective inductance. The four parallel conducting channels in a CNT give rise to an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are shown in Equation 8 below.

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \qquad L_K = \frac{h}{2e^2 v_F} \tag{8}$$

For $d=1\ nm$ and $y=1\ um$, L_M (per unit length) evaluates to ≈1.4 pH/um. On the other hand, L_K (per unit length) for a CNT evaluates to 16 nH/um. However, the *kinetic inductance* (L_K) in [26] is derived considering no potential drop along the nanotube; hence it must be treated with care. Since $L_K>>L_M$, the inclusion of L_K can have a significant impact on the delay model for interconnects. In the light of experimental evidence of potential drop appearing along the length of a nanotube [27], L_K *is excluded* from the calculations in this work. This is further justified by the experimental measurements of the high frequency characteristics of carbon nanotubes recently reported in [28], wherein the *large inductive effects expected due to* L_K *are not observed* up to frequencies as high as 10 GHz and the high frequency response is effectively damped by the nanotube resistance.

2.3 Previous Work on Performance of CNT Interconnects

Over the past year, several attempts have been made at evaluating the prospects of CNT-bundle interconnects vis-à-vis copper interconnects of the future. In [3] it is shown that while carbon nanotube interconnects can alleviate the severe reliability limitations of future copper interconnects, high density CNT bundles are needed in order to achieve performance comparable to copper. The work in [29] compares the performance of an isolated CNT and a flat array of CNTs (see **Fig. 6**) behaving as interconnections and reports that CNT interconnects do not compare favorably with copper conductors. It is in fact trivial to see that such configurations cannot be compared to copper interconnects due to the intrinsically high resistance associated with an isolated CNT, hence technologists have always focused on CNT *bundles* in practice [4, 5]. The coupling capacitance model for CNT interconnects in [29] considers only the coupling between adjacent CNTs and not that between bundles forming adjacent interconnects (coupling between adjacent interconnects is considered for copper interconnects, using a simplistic parallel plate capacitance). Evidently the coupling capacitance between adjacent CNTs forming the same bundle will always be very high due to their physical proximity. However, this capacitance does not appear as a load when the CNTs form part of the same interconnection (discussed in further detail in Section 3.2). These shortcomings lead to the (incorrect) conclusion in [29] that carbon nanotube interconnects are not suitable for VLSI applications.

The work in [25] and [30] (in contrast with [29]) shows that ideal, densely packed CNT-bundle interconnects can provide significant improvement in interconnection speed. The conclusion is, however, based on optimistic assumptions (ideal metal-nanotube contacts and completely metallic nanotube bundles) which are far removed from the technological realities of carbon nanotube interconnects. In fact, the significance of the error (an order of magnitude) in neglecting the imperfect metal-nanotube contact resistance leads to the wrong conclusion in [31] that a *flat array* of CNTs is better suited than copper for *local* interconnects. The treatment of the critical issue of CNT bundle capacitance also raises concern. While [30] avoids the calculation of capacitance by unjustifiably assuming that the capacitance for a CNT bundle is the same as that for copper interconnects, [31] does not explain how the same interconnect analysis program can be used to extract capacitances for CNT bundles as for copper interconnects.

The reduction in delay variation and overall digital circuit power dissipation by the use of a flat array of CNTs [31] also does not reflect reality.

All these works fail to comprehend technology issues, such as imperfect metal-nanotube contacts and the density of metallic CNTs forming a bundle (further complicated by the presence of semi-conducting nanotubes). The inclusion of kinetic inductance in the delay model must also be viewed with caution in the light of the arguments made in Section 2.2. Moreover, they provide no appreciation of the changing scenarios as the interconnect domains change from the local to intermediate and global levels.

Contribution of This Work:

The work presented here provides the first comprehensive analysis of realistic carbon nanotube interconnects in VLSI applications and presents the advantages as well as the limitations of this emerging interconnect technology. The domains of on-chip interconnections where CNT-bundles can be applied in a realistic VLSI circuit are identified along with the requirements that must be fulfilled in order to make them viable as replacements for copper interconnects. The equivalent circuit model parameters for a *CNT-bundle interconnect* based on interconnect geometry are calculated explicitly for the first time. The performance evaluation of CNT bundle interconnects presented here takes into account practical limitations such as the inevitability of imperfect metal-nanotube contacts and low density of metallic CNTs in a bundle, as well as circuit parameters like the effect of realistic drivers and loads. In addition, the comparison of CNT-bundle interconnect performance to copper wires is performed at different interconnect levels of a VLSI chip for the first time. In the event that CNT-bundle interconnects do become a reality in the future, this work constitutes a significant first step towards developing a CAD methodology for evaluating the performance of such interconnects.

3. Equivalent Circuit Parameters for a Bundle of SWCNTs

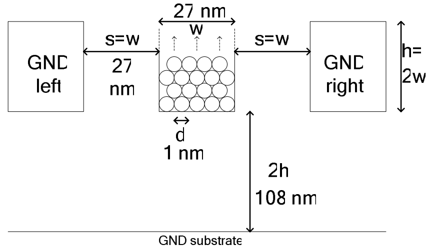

Figure 5: Schematic of interconnect geometry under consideration for performance comparison between CNT-bundle and copper interconnects.

Fig. 5 schematically shows a cross-section of the interconnect structure considered for the performance evaluation of CNT-bundle and copper interconnects. Two immediately adjacent metallic wires (held at ground potential) parallel to the interconnection under study are considered, while the interconnect itself switches from '0' to '1'. The technology dependent wire widths, aspect ratios and dielectric constants follow from the ITRS 2004 [1] predictions, and spacing between wires is assumed to be equal to wire width. The distance from substrate for local interconnects is assumed to be twice the thickness of interconnect (*2h*, as shown in **Fig. 5**). Coupling to successive orthogonal metal layers is neglected to keep the analysis simple. For the same reason, finite conductivity of the substrate and coupling with simultaneously switching wires are also beyond the scope of this work.

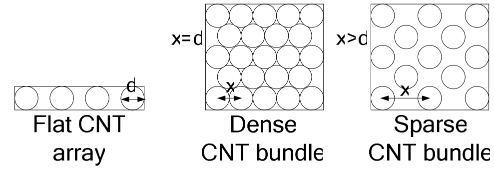

Figure 6: Flat CNT array and CNT bundles with varying density of metallic CNTs. CNT bundle interconnects give much better performance than flat arrays. Present day fabrication techniques cannot ensure all CNTs in a bundle are metallic. Varying density of metallic CNTs and presence of semi-conducting CNTs (considered to be insulating [15]) are modeled using inter-CNT distance, *x*.

A CNT-bundle interconnect is assumed to be composed of hexagonally packed identical metallic single-walled carbon nanotubes. Each CNT is surrounded by six immediate neighbors, their centers uniformly separated by a distance 'x'. The densely packed structure with 'x' = 'd' (CNT diameter), shown in **Fig. 6**, will lead to best interconnect performance. In practical reality, not all CNTs of a bundle are metallic. Non-metallic CNTs are treated as not contributing to current conduction and their presence is taken into account by considering "sparsely" populated bundles (**Fig. 6**). The expressions to calculate the number of CNTs in the bundle are shown in Equation 9, where n_H is the number of "rows" in the interconnect bundle, n_W is the number of "columns", n_{CNT} is the total number of CNTs, and $\lfloor y \rfloor$ denotes the largest integer less than or equal to 'y'.

$$n_W = \left\lfloor \frac{w-d}{x} \right\rfloor ; n_H = \left\lfloor \frac{h-d}{\left(\sqrt{3}/2\right)x} \right\rfloor + 1 \tag{9}$$

$$n_{CNT} = n_W n_H - \frac{n_H}{2}, \quad \text{if } n_H \text{ is even}$$
$$= n_W n_H - \frac{n_H - 1}{2}, \quad \text{if } n_H \text{ is odd}$$

For the case of copper, the interconnect under study is replaced by a solid metal of same dimensions. The rest of this section is devoted to calculation of equivalent circuit parameters for the CNT-bundle. The calculations for copper interconnect are well known already: resistance is calculated as explained in Section 2.1 while capacitance and inductance are evaluated using common field solvers. Note that inter-metal dielectric constants at different technology nodes are obtained from ITRS [1] predictions and assumed to be same for Cu as well as CNT bundle interconnects.

3.1 Resistance of a CNT-bundle

In order to calculate the effective resistance of a CNT-bundle, it is assumed that all CNTs packed into the interconnect structure are metallic and conducting. The fact that it is, in general, difficult to control the conductance properties of all CNTs in the bundle is accounted for by considering reduced packing densities as shown in **Fig. 6**. The CNT-bundle resistance is then given by Equation 10, where $R_{isolated}$ is the resistance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \tag{10}$$

It must be noted that it is implicit in this formulation that the coupling between adjacent CNTs of a bundle is weak. However, this is a fair assumption because it has been shown that there exists a large tunneling resistance (≈ 2 - 140 MΩ) between the CNTs forming a bundle [15].

3.2 Capacitance of a CNT-bundle

The electrostatic capacitance of a *CNT bundle* has not been the subject of much analysis in the existing literature. The work in [32] studies the electrostatic capacitive coupling to the gate electrode for a flat array of CNT FETs.

For the electrostatic analysis of a CNT bundle, each CNT is treated as a classical metal with equal potential over the tube, similar to the approach in [32]. The expression for the intrinsic plate capacitance for an isolated CNT (C_E) has been shown before (Equation 6). **Fig. 7(a)** schematically shows the electrostatic field lines emanating from an isolated CNT in this case. **Fig. 7(b)** shows the corresponding situation for a CNT at the bottom edge of an interconnect bundle which is surrounded by four other CNTs.

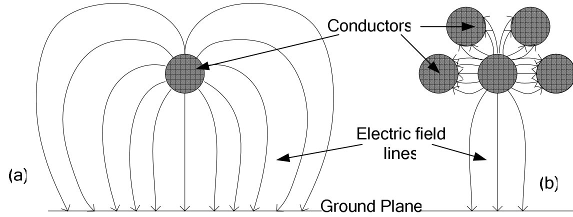

Figure 7: Schematic showing termination of electric field lines for (a) an isolated conductor over a ground plane, and (b) a conductor at the bottom edge of a bundle surrounded by four other conductors.

Applying the lessons learned from [32], some insights can be gained into the electrostatic capacitance of a CNT bundle. It can be expected that most field lines will terminate in the surrounding CNTs of the bundle, and the capacitive coupling to these will be very high due to the small distance separating them. A formula was presented in [29] for this capacitance. However, the mutual capacitance between CNTs of the same bundle is of no consequence as it does not place any additional load on the interconnect. This is because, when the CNT bundle carries current, it is assumed that each CNT conducting current is held at the same potential as any other. The electrostatic capacitance of the bundle that appears as a load on the interconnect is expected to arise mainly from the CNTs lying at the edges of the bundle (**Fig. 8**) that are capacitively coupled with the adjacent interconnects (left and right neighbors) as well as the substrate. The coupling to the adjacent interconnects is expected to be higher than that to the substrate due to higher proximity (see **Fig. 5**).

In the absence of actual data on the electrostatic capacitance of a CNT bundle of these dimensions, the strategy to develop a coarse model for the electrostatic capacitance is based on characterizations of an equivalent and familiar geometry using the field solver FastCap [33]. For this purpose, each CNT in the bundle is replaced by a square conductor circumscribing the tube as shown in **Fig. 8**. The intrinsic plate capacitance (C_E, refer to Section 2.2) for such an isolated square wire (isolated) is found to be of the same order of magnitude as that of the corresponding isolated nanotube. The total electrostatic coupling capacitance for each CNT marked in the **Fig. 8** with respect to the left/right neighbors and the substrate are evaluated using FastCap. It is observed that the total coupling capacitance for these CNTs can be roughly related to the value of intrinsic plate capacitance (C_E) of an isolated conductor with respect to the neighboring interconnects on either side (left/right). The relations are verified by simulations across dimensions corresponding to three different technology nodes (45, 32 and 22 nm) and are summarized in Equations 11. C_{En} and C_{Ef} are the intrinsic plate capacitances (C_E from Equation 6) calculated for an isolated CNT over a ground plane. C_{En} is calculated assuming the ground plane to be at a distance equal to the separation distance from the "near" adjacent interconnect (in **Fig. 8**, for the CNTs labeled 1, 4, 5 and 6, this distance is '*s*'). C_{Ef} is calculated assuming the ground plane to be at a distance equal to the separation distance from the "far" adjacent interconnect (in **Fig. 8**, for the CNTs labeled 1, 4, 5 and 6, this distance is '*s+w*').

$$C_{CNT1} = \frac{C_{En}}{2}; C_{CNT2} = \frac{C_{Ef}}{4}; C_{CNT4} = \frac{C_{En}}{4}\left(1+\frac{1}{5}\right); \tag{11}$$
$$C_{CNT5} = \frac{C_{En}}{2}; C_{CNT6} = \frac{C_{Ef}}{4}$$

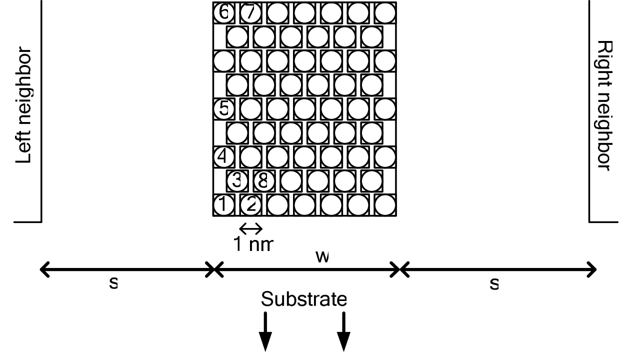

Figure 8: Schematic of CNT-bundle interconnect. Elements labeled with numbers are the ones characterizing the electrostatic coupling capacitance of the CNTs along the edges of the bundle. Each circular cross-section CNT is shown along with the circumscribing square conductor used for FastCap [33] simulations.

It is observed, as expected, that the CNTs completely surrounded by other nanotubes (for example CNT #8 in **Fig. 8**) have a very small electrostatic coupling capacitance to ground compared to those along the edges of the bundle (three orders of magnitude smaller). CNTs nearly completely surrounded as CNT #3 have capacitance (to ground) over an order of magnitude less than those along the edges. Their contribution to the total electrostatic capacitance is thus neglected. Using these relations, we calculate the electrostatic capacitance contributed by each "edge" CNT based on the corresponding value of C_E (Equation 12). The total electrostatic capacitance of the bundle is given by the sum of the contribution from each of these CNTs.

$$C_E^{bundle} = 2C_{En} + \frac{n_W - 2}{2}C_{Ef} + \frac{3(n_H - 2)}{5}C_{En} \tag{12}$$

Since the quantum capacitances of all the CNTs forming a CNT bundle appear in parallel, the effective quantum capacitance of the bundle is the sum of the individual quantum capacitances. This is shown in Equation 13, where C_Q^{CNT} is the quantum capacitance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

$$C_Q^{bundle} = C_Q^{CNT} \cdot n_{CNT} \tag{13}$$

The effective capacitance (C_{bundle}) of the series combination of a quantum and electrostatic capacitance is given by Equation 14.

$$\frac{1}{C_{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \tag{14}$$

3.3 Inductance of a CNT-bundle

The inductance of a *CNT bundle* is given by the parallel combination of the inductances corresponding to each CNT forming the bundle, as shown in Equation 15, where L^{CNT} is the (magnetic) inductance of an isolated SWCNT (Equation 8).

$$L_{bundle} = \frac{L^{CNT}}{n_{CNT}} \quad (15)$$

4. Performance Comparison of CNT-bundle vs. Copper Interconnects

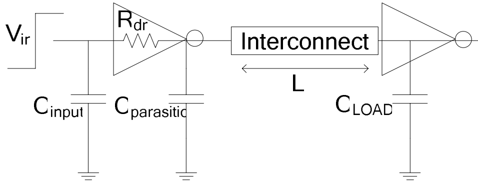

Figure 9: Schematic of interconnect circuit used for performance evaluation. The "interconnect" is replaced by the equivalent circuit representation for CNT-bundle or Cu interconnect.

The interconnect structure under study for performance comparison of CNT-bundle vs. copper interconnects is shown schematically in **Fig. 9**. The interconnect of length 'L' is replaced by the equivalent circuit for CNT-bundle and copper interconnects respectively. The driver is represented here by its equivalent input capacitance, resistance and output parasitic capacitance. The output appears only as a capacitive load representing the combined input capacitances of the driven gates. Without any loss of generality, the driver for local interconnects is assumed to be a minimum sized inverter driving a fan-out of four minimum sized inverters at the load end. For global interconnects, the interconnect is assumed to be part of an optimally buffered long interconnect, with identical buffer stages at its driver and load ends. For intermediate level interconnects, the driver and load devices are sized up as in the case of global wires, while interconnect lengths are typical values at the corresponding metal level. Driver and load device parasitic elements are determined from technology predictions by ITRS 2004 [1]. For global interconnects, [34] presents a detailed analysis of the conditions under which an RC model becomes inaccurate and RLC representation of interconnects is necessary. It is found that in the case of all the scenarios considered here, distributed RC models suffice, consistent with the results shown in [35] for scaled global wires. This is equivalent to saying that the RC charge-up time for these interconnects is larger than the wave propagation time.

For the sake of a fair performance comparison, the contributions from all interconnect parameters to circuit delay need to be considered. C_{input} and $C_{parasitic}$ (in **Fig. 9**) have equal contributions to delay irrespective of the interconnect technology used, hence these are omitted from the delay expression. However, it must be noted that R_{driver} and C_{LOAD} are important parameters for this calculation.

Local Interconnect Delay:

Local interconnects are typically a few hundred nanometers and no more than a few microns in length as longer wires are routed to higher metal layers. Hence it is safe to assume that local interconnect lengths are typically within the length of mean free path of electrons in a CNT.

Fig. 10(a) shows that the resistance of CNT bundles with imperfect contacts (120 KΩ [22]) remains higher than Cu wire across technology generations, while perfect contacts make the resistance much lesser than copper wires. This is the situation with maximum densely packed CNT-bundles. With the reduced densities that are realistically achievable, the resistance of CNT bundles will be higher. Capacitance of CNT bundles, on the other hand, remains higher than copper wires across all technology generations (**Fig. 10(b)**).

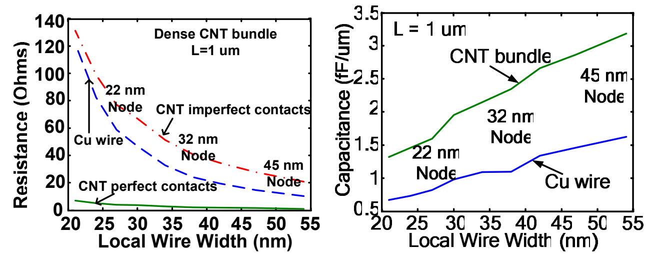

Figure 10: (a) Resistance and (b) Capacitance of 1um long local interconnect across different technology generations using densely packed CNT bundles versus copper wires.

Fig. 11 shows that the propagation delay of local interconnects with densely packed CNT bundles is higher than that with Cu wires across all technology generations, even if contacts are perfect and a mean free path (L_0) as large as 10um can be achieved. This is because the higher capacitance of CNT bundles and the high resistance of minimum sized drivers at the local interconnect level overshadow the advantage from low CNT-bundle resistance. Hence lowering the CNT bundle capacitance may lead to better performance.

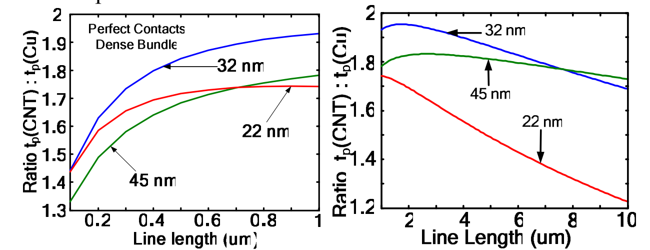

Figure 11: (a) Ratio of local interconnect propagation delay with dense CNT bundle interconnect to that with Cu wire as a function of interconnect length (*L*). (b) Ratio for larger values of *L*, assuming mean free path L_0>*L*. Both plots assume perfect contacts.

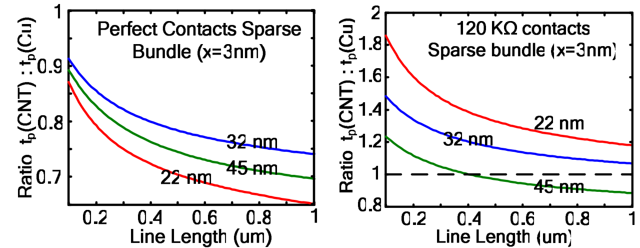

Figure 12: Ratio of local interconnect propagation delay with sparse CNT bundle interconnect with (a) perfect contacts and (b) imperfect (120 KΩ) contacts, to that with Cu wire as a function of interconnect length. Both plots assume x=3 nm (see Fig. 6).

It is observed from **Fig. 12** that the performance of CNT bundles with perfect contacts (**Fig. 12 (a)**) becomes better than Cu wires if the distance between adjacent metallic CNTs forming a bundle is increased. However, with realistic imperfect contacts (**Fig. 12(b)**), the delay is still higher than Cu wires (see **Fig. 6** for an explanation of CNT density in a bundle). This interesting result (that slightly lower metallic CNT density improves local interconnect performance) counters the expectation in previously reported works [3]. Also, it is worthy of note that it is very difficult to achieve the maximum packing density for CNTs [3], and these lower densities may be more easily achievable.

A small decrease in CNT density improves local interconnect performance as it reduces the capacitance of the bundle without increasing resistance too much. However, the density can be reduced only up to a small extent beyond which the improvement in performance is lost due to increasing resistance of the bundle. This behavior is evident from **Fig. 13** which shows that there

exists an optimal point where optimum performance can be achieved with the CNT bundle. **Fig. 13(a)** also points to the fact that, if the imperfect contact resistance is held constant, a reduction in CNT density may not lead to the same improvement in performance as technology scales. Hence it becomes increasingly important to achieve higher quality metal-nanotube contact resistances in order to derive a performance improvement from CNT bundle local interconnects (**Fig. 13(b)**).

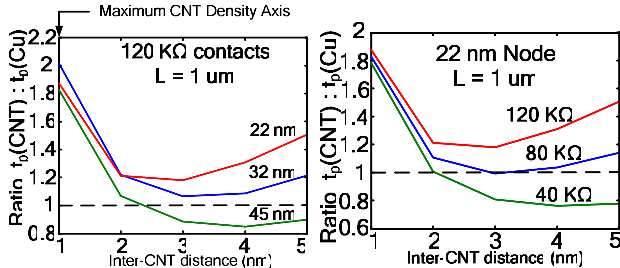

Figure 13: Ratio of local interconnect propagation delay with CNT bundle to that with Cu as a function of density of metallic CNTs in a bundle (a) at different technology nodes and (b) for different imperfect contact resistance values at 22nm node. For "inter-CNT distance" see Fig. 6.

Intermediate and Global Interconnect Delay:

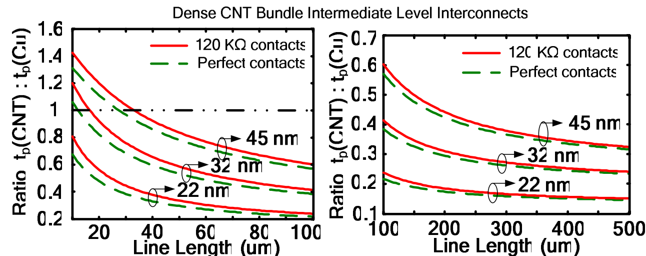

Figure 14: Ratio of propagation delay with dense CNT bundle interconnect to that with Cu wire as a function of intermediate level interconnect length. CNT mean free path (L_0) = 1um.

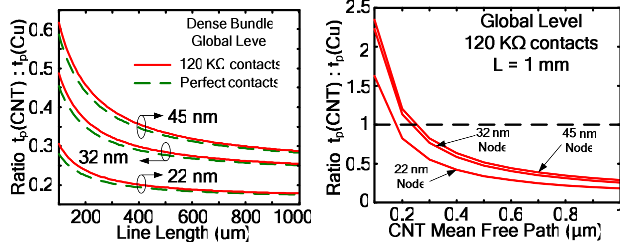

Figure 15: Ratio of global interconnect propagation delay with dense CNT bundle to that with Cu: (a) as a function of interconnect length (L_0 = 1um), (b) as a function of L_0 for 1mm long interconnect.

Fig. 14 shows the length dependence of densely packed CNT-bundle interconnects (mean free path $L_0=1\mu m$) at the intermediate level. It is observed that beyond a certain minimum length (for example about 35 um at the 45 nm node), the performance of CNT-bundle interconnects at this level is better than copper wires. As technology scales, this minimum length decreases while the improvement in performance increases. **Fig. 15(a)** shows that global interconnects implemented with CNT-bundles can achieve significantly better performance than copper. In the case of both intermediate and global interconnects, the improvement in performance with CNT-bundles is larger for longer interconnects and saturates beyond a certain length. For these results, it has been assumed that CNT mean free path length is 1um. In the presence of defects in a nanotube, the mean free path has been observed to be much less than the typical 1um [22]. The impact of reduced mean free path lengths on global interconnect propagation delay with CNT bundles is shown in **Fig. 15(b)**. Evidently it is critical to ensure that CNTs forming the bundle are free of such degrading effects so that mean free path lengths are maintained in the range of a micrometer.

The improved performance of long intermediate and global level CNT-bundle interconnects is because of the much lower resistance as compared to copper global interconnects. While copper interconnect resistance increases linearly with length, in the case of CNT bundle interconnects it is only the scattering resistance proportional to $h/4e^2$ that increases linearly. The additional resistance arising from imperfect metal-nanotube contacts (which dominates the resistance in the case of short local interconnects) does not increase with length. Hence **Fig. 14** and **Fig. 15** show only a minor difference between the performance of CNT-bundles with perfect contacts and with imperfect contacts.

The performance improvement in long intermediate and global interconnects, as a result of using CNT-bundles, decreases when the CNT packing density is decreased, as seen in **Fig. 16**. This again shows that the performance improvement for long interconnects is because of the lower resistance of CNT bundles as compared to copper. As CNT packing density is decreased, the effective resistance increases and hence performance degrades. This in contrast with the short local interconnects where the effect of interconnect capacitance dominates and a slightly lower CNT density (and hence lower interconnect capacitance) leads to improved performance.

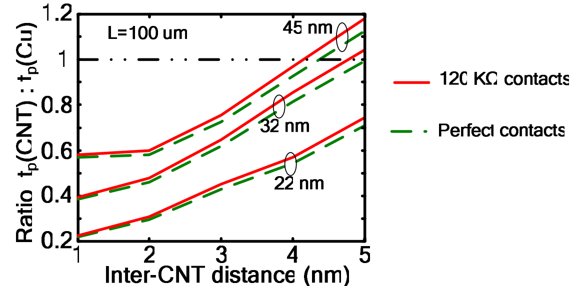

Figure 16: Ratio of propagation delay with sparse CNT bundle interconnect to that with Cu wire as a function of distance separating adjacent metallic CNTs of a bundle.

5. Summary

The applicability of carbon nanotube bundles as interconnects of the future has been analyzed while taking into account the practical limitations of this emerging technology. The performance of CNT-bundle interconnects has been compared to that of copper interconnects of future technology generations and their applicability at different metal tiers in a VLSI design is studied. At the local interconnect level, CNT-bundles with imperfect contacts do not give much performance improvement. It is also shown that there exists an optimal density less than the maximum packing density of CNT bundles at which the interconnect propagation delay is minimum. This is a useful finding in light of the fact that CNT-bundles fabricated till date do not have a very high density of CNTs [3] and all the CNTs in a bundle may not have metallic nature. Although this fact can be advantageous to the use of CNTs as interconnects, with technology scaling, it becomes imperative to also reduce the additional resistance associated with imperfect metal-nanotube contacts. In the case of long intermediate and global interconnects, densely packed CNT bundle interconnects show significant improvement in performance as compared to copper interconnects, in spite of imperfect metal-nanotube contacts. On the other hand, degradation in mean free path length of

CNTs (as may happen in the presence of defects) can off-set the benefits of using CNT-bundle interconnections. As mentioned in the ITRS 2004 [1], global interconnect delay is one of the VLSI industry's topmost interconnect challenges. Hence, if long lengths of densely packed carbon nanotube bundles with mean free path around 1um can be fabricated reliably, they will provide a valuable alternative to copper interconnections.

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