- X. Qiu, M.Marek-Sadowska and W. Maly, "3D Chips Can be Cool: Thermal Study of VeSFET-based ICs," *Proc. Information and Communication Technology Conference*, 2013, pp. 2349 – 2355
- 2. X. Qiu, M.Marek-Sadowska, "Routing Challenges for Designs With Super High Pin Density," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 9, September 2013, pp. 1357-1368.
- 3. X. Qiu, M.Marek-Sadowska and W. Maly, "Designing VeSFET-based ICs with CMOSoriented EDA Infrastructure," *Proc. International Symposium on Physical Design*, 2013, pp. 130-136.
- 4. X. Qiu, M.Marek-Sadowska and W. Maly, Characterizing VeSFET-based ICs with CMOS-oriented EDA Infrastructure, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, accepted for publication.
- 5. W. Kuzmicz, P. Mierzwinski, "Bipolar transistor in VESTIC technology," *Proc. of SPIE* vol. 8902 89020M-1, 2013.
- 6. D. Kasprowicz and B. Swacha, "VeSFET as an Analog-Circuit Component," *IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems* (DDECS), 2013, pp. 199-204.
- L. Barbut, F. Jazaeri, D. Bouvet, J-M. Sallese, "Design Space of Twin Gate Junctionless Vertical Slit Field Effect Transistors," *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2013, pp. 393-396.
- 8. L. Barbut, F. Jazaeri, D. Bouvet, J-M. Sallese, "Heavily Doped Junctionless Vertical Slit FETs with Slit Width Below 20nm," *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2013, pp. 397-400.

2012

- Z. Chen, A. Kamath, N. Singh, N. Shen, X. Li, G.-Q. Lo, D.-L. Kwong, D. Kasprowicz, A. Pfitzner and W. Maly, "N-channel Junction-less Vertical Slit Field-Effect Transistor (VeSFET): Fabrication-based Feasibility Assessment," 2012 International Conference on Solid-State and Integrated Circuit (ICSIC 2012), IPCSIT vol. 32 (2012) IACSIT Press, Singapore.
- A. Kamath, Z. Chen, N. Shen, X. Li, N. Singh, G.-Q. Lo, D.-L. Kwong, D. Kasprowicz, A. Pfitzner and W. Maly, "Logic Functionality in Vertical Slit Field Effect Transistor (Vesfet)," 2012 International Conference on Solid-State and Integrated Circuit (ICSIC 2012), IPCSIT vol. 32 (2012) IACSIT Press, Singapore.
- 3. X. Qiu, M.Marek-Sadowska and W. Maly, "Vertical Slit Field Effect Transistor in Ultra-Low Power Applications", *International Symposium on Quality in Electronic Design*, pp. 385-391.
- 4. V. S. Nandakumar, M. Marek-Sadowska, "A Low Energy Network-on-Chip Fabric for 3-D Multi-Core Architectures," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol.2, no.2, June 2012, pp.266-277.
- 5. X. Qiu and M.Marek-Sadowska, "Can Pin Access Limit the Footprint Scaling?," *Proceedings of Design Automation Conference*, 2012, pp. 1100-1106.

2013

2011

- A. Pfitzner and D. Kasprowicz, "Compact model of the Vertical Slit Field-Effect Transistor (VeSFET)," *MOS-AK/GSA ESSDERC/ESSCIRC* Workshop, Sept. 16, 2011, Helsinki.
- 2. M. Marek-Sadowska, X. Qiu, "A study on cell-level routing for VeSFET circuits," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2011, pp.127-132, 2011.
- 3. M. Pastre, F. Krummenacher, L. Barbut, J. Sallese, M. Kayal, "Towards Circuit Design using VeSFETs," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2011, pp.139-144, 2011.
- 4. L.Barbut, D. Bouvet and J. Sallese, "Towards Fabrication of Vertical Slit Field Effect Transistor (VeSFET) as New Device for Nano-Scale CMOS Technology," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2011, pp.325-328.
- W. Maly, N. Singh, Z. Chen, N. Shen, X. Li, A. Pfitzner, D. Kasprowicz, W. Kuzmicz, Y.-W. Lin, M. Marek-Sadowska, "Twin Gate, Vertical Slit FET (VeSFET) for highly periodic layout and 3D integration," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2011, pp.145-150, 2011.
- 6. A. Pfitzner, "Vertical-Slit Field-Effect Transistor (VeSFET) design space exploration and DC model," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2011, pp.151-156, 2011.
- D. Kasprowicz, "A compact model of VeSFET capacitances," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)* 2011, pp.121-126, 2011.
- Y.-W. Lin, M. Marek-Sadowska, W. P. Maly, "On Cell Layout-Performance Relationships in VeSFET-Based, High-Density Regular Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 30, Issue 2, pp 229-241, Feb 2011.
- 9. V. S. Nandakumar, M. Marek-Sadowska, "Low Power, High Throughput Network-on-Chip Fabric for 3D Multicore Processors," *Proc. Int. Conf. on Computer Design*, pp.453-454.

2010

- 1. Y.-W. Lin, M. Marek-Sadowska, W. Maly, "Performance study of VeSFET-based, highdensity regular circuits," *ISPD 2010*:161-16
- 2. Y.-W. Lin, M. Marek-Sadowska, W. P. Maly, "Layout generator for transistor-level high-density regular circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, v.29 n.2, p.197-210, February 2010.
- 3. W. Maly, "Vertical slit transistor based integrated circuits (VeSTICs) paradigm," *ISPD* 2009, pp.63-64

- 4. M. Weis and D. Schmitt-Landsiedel, "Circuit Design with Adjustable Threshold Using the Independently Controlled Double Gate Feature of the Vertical Slit Field Effect Transistor (VeSFET)," *Advances in Radio Science*, vol. 8, 2010, pp. 275-278
- 5. V. M. Srivastava, S. Kapoor, Nitasha, N. Jaswal, G. Singh, "Full Subtractor Circuit Design with Independent Double Gate Transistor," *International Conference on Recent Trends in Information, Telecommunication and Computing*, 2010, pp. 302-304.
- 6. V. M. Srivastava, N. Saubagya, G. Singh, "Circuit Design with Independent Double Gate Transistors," *International Conference on Advances in Computer Engineering*, 2010, pp. 289-291.

2009

- 1. M. Weis, Ph. Teichmann, T. Seybold, D. Kasprowicz, A. Pfitzner, W. Maly, and D. Schmitt-Landsiedel, "Adiabatic Circuits using Vertical Slit Field Effect Transistor," in *European Solid-State Circuits Conference ESSCIRC Fringe*, 2009.
- M. Weis, A. Pfitzner, D. Kasprowicz, R. Emling, T. Fischer, S. Henzler, W. Maly, and D. Schmitt-Landsiedel, "Stacked 3-Dimensional 6T SRAM Cell with Independent Double Gate Transistors," in *International Conference on Integrated Circuit Design and Technology ICICDT* 2009, pp. 169-172, 2009.
- 3. M. Weis, R. Emling, and D. Schmitt-Landsiedel, "Circuit design with Independent Double Gate Transistors," in *Advances in Radio Science.*, 7, pp. 231-236, 2009.
- 4. Y.-W. Lin, M. Marek-Sadowska, W. Maly, "Transistor-level layout of high-density regular circuits," *ISPD* 2009:83-90
- 5. M. Weis, A. Pfitzner, D. Kasprowicz, R. Emling, W. Maly, and D. Schmitt-Landsiedel, "Adder Circuits with Transistors Using Independently Controlled Gates,"*Proc. IEEE International Symposium on Circuits and Systems, 2009. ISCAS* 2009, pp. 449-452.

2008

- 1. Y.-W. Lin, M. Marek-Sadowska, W. Maly, A. Pfitzner, D. Kasprowicz, "Is there always performance overhead for regular fabric?," *ICCD* 2008:557-562
- M. Weis, A. Pfitzner, K. Kasprowicz, Y.-W. Lin, Th. Fischer, R. Emling, M. Marek-Sadowska, D. Schmitt-Landsiedel, and W. Maly, "Low Power SRAM Cell Using Vertical Slit Field Effect Transistor (VeSFET)," in *European Solid-State Circuits Conference ESSCIRC Fringe*, 2008.

2007

 W. Maly, Yi-Wei Lin, M. Marek-Sadowska, "OPC-free and minimally irregular IC design style," *Proceedings of the 44th annual Design Automation Conference*, June 04-08, 2007, San Diego, California.

Theses

- 1. Marcus Weis, "A Circuit Design Perspective for the Vertical Slit Field Effect Transistor (VESFET)," PhD. Thesis, University of Munich.
- 2. Yi-Wei Lin, "Physical Design for VeSFET-based High-Density Regular Circuits", PhD. Thesis, University of California, Santa Barbara, 2010.
- 3. Xiang Qiu, "Assessing Circuit-Level Properties of VeSFET-based ICs," PhD. Thesis, University of California, Santa Barbara, 2013.

Reports

- 1. W. Maly and A. Pfitzner, "Complementary Vertical Transistors," Carnegie Mellon University, CSSI Techreport, No. 08-02,01/2008
- 2. Tung Zhi Yan, "Electrical Characterization of the Novel Vertical Slit Field-Effect Transistor (VeSFET)," Final Year Project for Bachelor of Engineering (Electrical and Electronic Engineering) degree, Nanyang Technological University, Singapore, 2012

Patents

1. Wojciech Maly,"INTEGRATED CIRCUIT DEVICE, SYSTEM, AND METHOD OF FABRICATION", Pub No. US 2009/0321830, Pub Date: Dec 31, 2009, Assignee: Carnegie Mellon University.

Other

1. W. Maly, A. Pfitzner, N. Singh, D. Kasprowicz, M. Marek-Sadowska, Y-W. Lin, Z. Chen and X. Li, "Dual Gate Vertical Slit FET (VeSFET) for Highly Periodic Layout and 3D Integration", Rejected by IEDM 2010.