Terabit/Sec VCSEL-Based 48-Channel Optical Module Based on Holey CMOS Transceiver IC

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***Abstract*—We report here on the design, fabrication and characterization of 48-channel parallel optical transceivers demonstrating terabit/sec data transfer rate. The 0.48 Tb/s transmit plus 0.48 Tb/s receive throughput was achieved using a second-generation single-chip holey CMOS transceiver IC. In addition to 24 receiver (RX) and 24 laser diode driver circuits, the 5.2 mm $\times$ 5.8 mm single CMOS chip incorporates 48 through-substrate optical vias (holes), one for each transmitter (TX) and RX channel. A complete holey Optochip is formed following direct flip-chip attachment of 24-channel 850-nm VCSEL and PD arrays. The 48 optical vias enable optical access to the 24 VCSELs and 24 PDs. The holey Optochip concept provides a dense chip-scale package which is fully compatible with industry-standard top emitting/detecting 850-nm VCSELs/PDs providing optimized high-speed performance through close integration of the optoelectronic (OE) devices with their drive electronics. Furthermore, the optical vias and OE devices are arranged in a 4 $\times$ 12 array on 250 μm $\times$ 250 μm pitch to facilitate direct fiber-coupling to a standard 4 $\times$ 12 multi-mode fiber array.**

The Optochips are packaged into complete modules by flip-chip soldering to high-density, high-speed organic carriers. A pluggable connector soldered to the bottom of the carrier provides all module electrical I/O. The 18 mm $\times$ 18 mm overall module area is dictated by the 0.8 mm-pitch ball grid array (BGA) of the organic carrier and connector. Fully functional holey Optomodules with 24 TX and 24 RX channels operate up to 20 Gb/s/ch achieving efficiencies (including both TX and RX) of 7.3 pJ/bit. The terabit/sec data rate (480 Gb/s TX + 480 Gb/s RX) is highest reported for single-chip CMOS transceiver modules.

***Index Terms*—CMOS analog integrated circuits, optical communication, optoelectronic devices, optical interconnections, optical receivers, optical transmitters, photodiodes, semiconductor laser arrays.**

I. Introduction

PARALLEL optical interconnects are extensively deployed today for rack-to-rack interconnects in high performance computing (HPC) systems as they provide greater interconnect bandwidth and support several-meter links at lower power consumption than comparable electrical links. Large scale deployment of rack-to-rack optical interconnects in HPC systems has been implemented using commercial fiber-coupled optical modules and active optical cables with 8–12 fibers operating at data rates up to 5 or 10 Gb/s [1], [2]. Typical commercial datacom optical modules utilize arrays of Vertical Cavity Surface Emitting Lasers (VCSELs) and GaAs PIN photodiodes coupled to standard 50-μm core multi-mode fiber (MMF) designed for interconnect distances up to 300 m at 10 Gb/s. The ever-increasing interconnect bandwidth demands of these systems is leading to adoption of optics at shorter distances giving rise to a "computercom" market segment requiring not only short interconnect distance (<10 m) but also necessitating higher density, reduced power and cost of optical modules. An example of the emerging computercom applications is the recently-introduced IBM Power 775 Supercomputer which realizes the next generation of optical interconnects, in which all board-to-board high-speed links, both inter-rack and intra-rack, are optical [3], [4]. The system employs up to 5000 optical modules in a single rack using compact, 12-channel μ-POD™ optical modules operating at 10 Gb/s [4] that are densely packaged directly onto a high performance ceramic multi-chip module (MCM) [3].

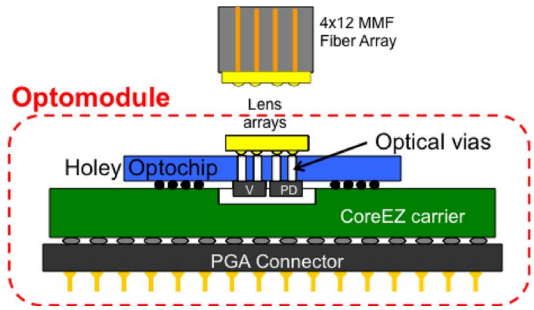

Fig. 1. Conceptual cross-section of Optomodule based on holey Optochip transceiver. V = VCSEL array, PD = photodiode array.

Compact 12-channel modules occupying an area of about 1 cm^2 have thus been demonstrated commercially with 120 Gb/s bandwidth [4] as well as prototypes operating up to 240 Gb/s aggregate bandwidth [5]. Previously we described a novel parallel optical module based on holey CMOS Optochip [6], [7], a highly-integrated chip-like package based on a single-chip CMOS IC with flip-chip attached 850-nm VCSEL and PD arrays. The key to the holey Optochip concept is the incorporation of optical vias (holes) in the IC to enable optical access to/from industry-standard 850-nm VCSEL and photodiode (PD) arrays through the IC silicon substrate. The Optochip is then flip-chip attached to an organic carrier which is further soldered to a pluggable pin-grid-array (PGA) connector to form the parallel transceiver Optomodule depicted in Fig. 1.

The first generation (Gen1) module utilized a single chip 90-nm CMOS IC with 24 transmitter circuits plus 24 receiver circuits. 2 $\times$ 12 VCSEL and PD arrays were flip-chip attached

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using AuSn solder to the center of the IC incorporating 48 optical vias. The optical vias and the OEs are arranged on a 250 μm $\times$ 250 μm pitch to match standard 4 $\times$ 12 MMF array. The periphery of the chip contains bond pads for flip-chip attachment of the Optochip to the organic carrier. High-speed characterization of the module showed good performance for all 24 TX channels and all 24 RX channels at 12.5 Gb/s, providing up to 300 Gb/s bidirectional aggregate bandwidth [6], [7].

The Gen1 fully packaged holey Optomodule operated error-free ($\mathrm{BER} < 10^{-12}$) at datarates up to 12.5 Gb/s with a few select channels reaching 15 Gb/s operation. This high-speed performance included limitations associated with electrical signal propagation within the package (e.g., organic carrier, PGA connector/socket, and differential electrical traces of the test motherboard) as well as the intrinsic Optochip performance. In this paper, we describe the design and fabrication of the second generation (Gen2) holey Optomodule with overall design similar to the original, described in detail in [6], but includes enhancement in the CMOS IC, the optoelectronic arrays, the high-density, high-speed organic carrier, and the pluggable PGA connector in order to achieve the target goal 20 Gb/s/ch.

II. Second Generation Holey Optochip

A. Optochip Enhancements

The single-chip CMOS IC with 24 transmitter circuits plus 24 receiver circuits measures 5.2 mm $\times$ 5.8 mm and is fabricated in IBM 90 nm CMOS technology. The circuit area for each channel is about 125 μm $\times$ 600 μm. In the second generation, both TX and RX amplifier circuits were optimized for reduced power dissipation and maximum bandwidth targeting 20 Gb/s operation. In addition, a significant modification was the incorporation of a feed-forward equalizer (FFE) output block implemented into the RX design following the improved TIA and five amplifier stages. The FFE circuit [8] provides tunable pre-emphasis of the RX outputs to drive ac-coupled 50-Ω off-chip loads with improved performance for lossy/dispersive electrical channels. This enhancement overcomes Gen1 RX bandwidth limitations due to packaging parasitics associated with the few cm-long transmission lines on the test motherboard and the PGA connector.

The layout of the IC remains the same with optical vias and OE bond pads in the center, and C4 pads on the periphery of the chip. The 48 optical vias are fabricated into fully-processed 200 mm CMOS wafers using a reactive ion etch (RIE) process to etch 150-μm diameter features in the Si substrate to a depth of about 150 μm. Optical via formation is completed by thinning the wafer to 150 μm thickness using a backside grind process.

The transceiver IC is designed for 850-nm VCSEL and PD arrays, with each OE array having a 2 $\times$ 12 layout of devices on a 250 μm $\times$ 250 μm pitch. The 48 optical vias are arranged in a 4 $\times$ 12 array on the same 250 μm $\times$ 250 μm pitch for optical coupling to standard 4 $\times$ 12 MT MMF array. Latest generation high-speed optoelectronic arrays fabricated by Emcore Inc. [9] were used for this assembly. For optimum high-speed performance, the assemblies used VCSELs with 5 μm diameters and PIN photodiodes with diameters of 25 μm. Dual topside contacts are employed for both the photodiodes and the lasers. In order to facilitate the assembly process, about 4 μm of AuSn solder with a diameter of 40 μm was pre-deposited on the bond pads of the OE arrays. A photograph of the transceiver IC and the 2 optoelectronic arrays is shown in Fig. 2.

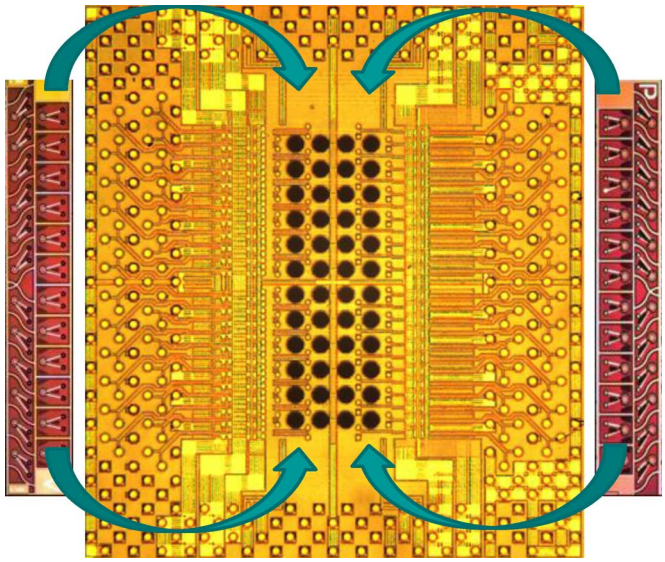

Fig. 2. Photograph of the holey CMOS IC and 24-channel OE arrays.

B. Packaging Enhancements

Enhancements in both the organic carrier and the PGA connector have been implemented. The high-speed, high-density CoreEZ™ [10] organic carrier provides electrical interconnects from the dense IC pad pitch to PCB pitch. It was redesigned with reduced BGA pad pitch of 0.8 mm resulting in 17 mm $\times$ 17 mm module dimensions. The top surface C4 pads (100 μm pads on 200 μm pitch) for mounting of the Optochip remain the same, and the electrical signals are routed to the bottom BGA pads. All 48 differential channels to/from the Optochip are routed to BGA pads on the periphery while the low speed bias and control signals are routed to pads near the center. The total thickness of the CoreEZ substrate is about 700 μm.

For the pluggable connector, a new higher performance version of the Interconnect Systems Inc. HiLo™ pin-grid connector (PGA) [11] was used with a denser pitch (0.8 mm), lower profile, and improved high-speed characteristics for >10 Gb/s performance. The connector has 363 contacts on a 0.8 mm pitch, matching the organic carrier, and is comprised of two halves: an 18 mm $\times$ 18 mm pin connector attached to the optical module and a 17 mm $\times$ 17 mm socket connector attached to the test circuit board.

C. Optomodule Assembly

Fabrication of the complete transceiver Optomodule involves the exclusive use of flip-chip soldering throughout the assembly process offering the potential of unprecedented high-speed performance and I/O density. The OE arrays are sequentially flip-chip attached to the holey CMOS IC using the AuSn solder pre-deposited on the OE arrays. The high melting temperature

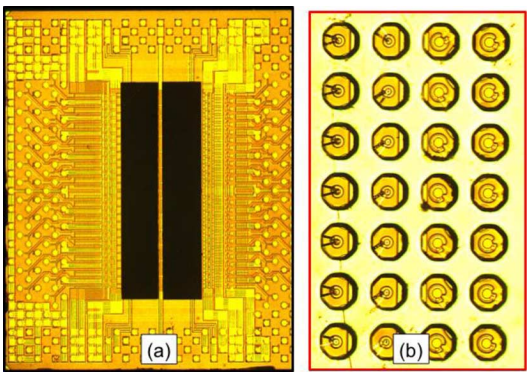

Fig. 3. (a) Optochip (5.2 mm × 5.8 mm) with flip-chip attached VCSEL and PD arrays. (b) Expanded bottom view showing individual VCSELs (left) and PDs (right) in the center of the optical vias.

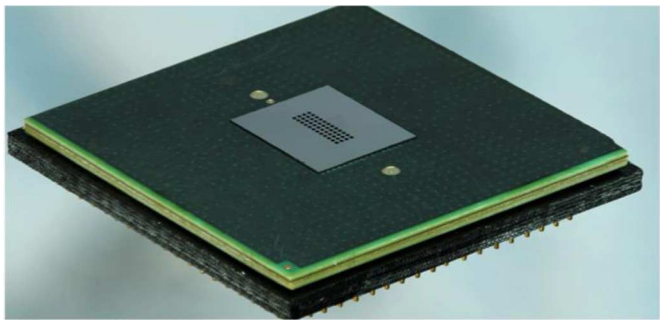

Fig. 4. Fully assembled pluggable transceiver Optomodule. The holey Optochip is at the center of the assembly, with the 4 × 12 array of optical vias clearly visible.

of the AuSn solder (>280°C) allows the subsequent flip-chip attachment of the Optochip to the organic carrier using eutectic SnPb solder, with a melting temperature of 183°C.

The assembled Optochip is shown in Fig. 3. The top view in Fig. 3(a) shows the CMOS IC with the OE arrays appearing in the center. The view from the opposite side of the Optochip (b) shows a magnified image of the octagonal optical vias with the individual VCSELs and PDs clearly evident.

The complete optical module involves the attachment of the Optochip to the organic carrier and PGA connector. Prior to assembly, a 3.8 mm × 2.1 mm cavity is milled into the center of the carrier to a depth of 0.4 mm to accommodate the OE arrays. After soldering the pin part of the PGA connector to the organic carrier, the Optochip is aligned and placed onto the solder pads of the organic carrier. As the assembly is heated to >200°C, the solder reflow process provides both self-centering and attachment of the Optochip to the organic carrier. A photograph of the complete Optomodule is shown in Fig. 4.

For characterization of the assembled 850-nm Optomodules, a test board incorporating the socket half of the PGA connector was designed and fabricated using low-loss Nelco 4000-13 material. Fig. 5 shows an example of a holey Optomodule plugged into the test board. On this board, the low-speed bias and control signals are routed from the center of the PGA socket to ribbon cable connectors on the edges of the board. As seen in

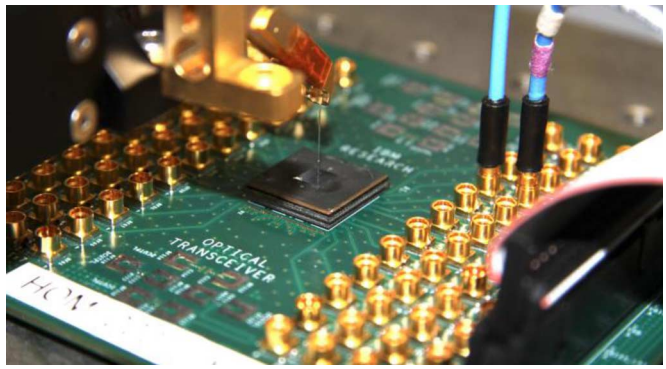

Fig. 5. Complete transceiver Optomodule plugged into test board. Ribbon cables on card edges provide low-speed electrical signals. 96 high-speed connectors are used for high-speed input/output. A single lensed MMF probe is used for optical input/output.

Fig. 5, ribbon cables are used on the edge of the test card to provide the low-speed bias and control signals. The 48 high-speed differential pairs are routed to high-speed electrical connectors through high-speed transmission lines with nominal differential impedance of 100 Ω. In order to accommodate the 96 high-speed connectors, an area of about 10 cm × 10 cm was required, leading to transmission line lengths ranging between 3–6 cm.

The high speed electrical input/output is provided through a matched pair of high-speed electrical cables. A single lensed multimode fiber (MMF) probe is used for optical access to individual VSCEL output or PD input.

III. Optomodule Characterization

A. High-Speed Measurements

High-speed characterization was carried out using the set up depicted in Fig. 5. The test pattern used was $2^7 - 1$ PRBS. Measurements were carried out using a 25 Gb/s Anritsu MP1800A pattern generator and error detector. Pre-emphasized electrical drive signals were used to overcome electrical trace losses at the input to the TX module. Eye diagrams were collected on a Tektronix DSA 8300 sampling oscilloscope with 30 GHz bandwidth.

High-speed electrical input/output to the Optomodule was accessed using the subminiature push-on (SMP) connectors shown in Fig. 5. Lensed 50-μm MMF probes were used to supply/collect the optical inputs/outputs. The data shown in this section was obtained on an Optochip with 5-μm diameter VCSELs and 25-μm diameter photodiodes.

1) Transmitter High-Speed Characterization: Fig. 6 presents the TX optical output eye diagrams for all 24 transmitter channels at 15 Gb/s and 20 Gb/s under the same operating conditions. The fiber coupled optical power level for the TX channels was approximately −3 dBm for the data in Fig. 6, and the photodiode used was a Newport D25XR. The 24 channels in both the TX and RX portion of the Optochip are laid out in four 1 × 6 banks, wherein the six devices share a common bias/control signal. The four banks of the TX are delineated in Fig. 6, and correspond to the physical layout of the 24 Optochip channels. The vertical

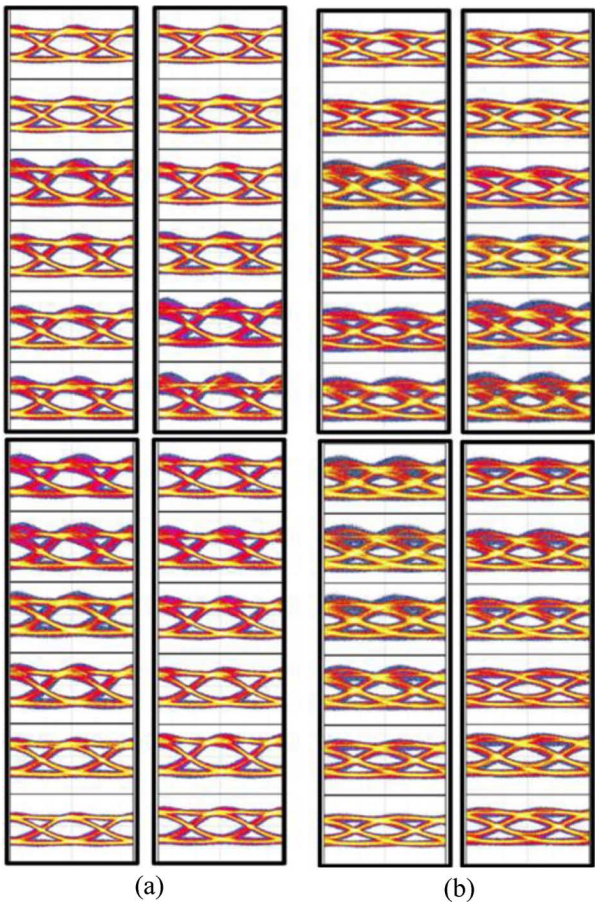

Fig. 6. 24-channel TX Optomodule eye diagrams at (a) 15 and (b) 20 Gb/s. The data is grouped in the 4 banks of 6 channels corresponding to the physical IC layout. The horizontal full scale of the eye diagrams spans 133 ps and 100 ps at 15 Gb/s and 20 Gb/s, respectively.

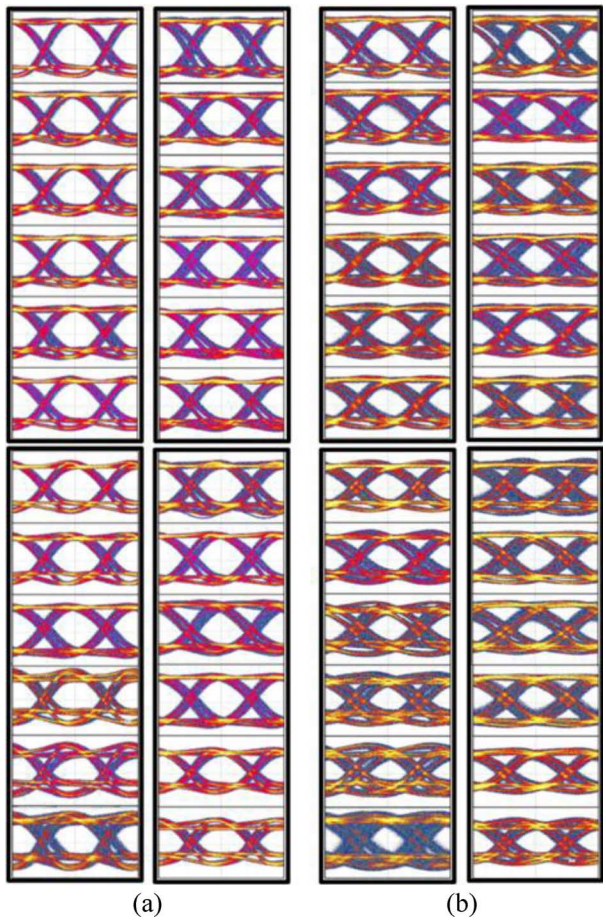

Fig. 7. 24-channel RX Optomodule electrical output eye diagrams at (a) 15 and (b) 20 Gb/s. The data is grouped in the 4 banks of 6 channels corresponding to the physical IC layout. The horizontal full scale of the eye diagrams spans 133 ps and 100 ps at 15 Gb/s and 20 Gb/s, respectively.

scale is the same for all the data in Fig. 6. All 24 channels exhibit open eye diagrams at 15 and 20 Gb/s with measured extinction ratios between 4 and 5 dB.

The TX supply voltages were 1.9 V for the pre-driver stage, and 0.85 V for the output driver stage. The bias voltage for the VCSELs was around 2.55 V, but was adjusted for each bank of six channels to yield a constant current of about 24 mA, or ~ 4 mA per laser. The per-channel power consumption was 30 mW.

2) Receiver High-Speed Characterization: Fig. 7 shows the electrical output eye diagrams for all 24 RX channels at 15 Gb/s and 20 Gb/s. All the eye-diagrams are plotted on the same vertical scale. A single-channel implementation of an Optochip TX channel incorporating the identical VCSEL and CMOS drive circuits was used as a reference source for the RX measurements. The reference TX voltage settings were re-optimized for best full-link performance, resulting in a TX power consumption of 67 mW with an extinction ratio of 4.7 dB.

All 24 RX channels produce open eye diagrams at 15 Gb/s with single-ended ouput amplitudes greater than 150 $\mathrm{mV_{p-p}}$. The eye-diagrams remain open at 20 Gb/s with some degradation due to limited RX bandwidth. The high-speed data of Fig. 7 was obtained with the following RX power supplies: 1.9 V for the transimpedance amplifier stage, 2.0 V for the limiting amplifier stage, 0.9 V for the output stage, and 3.0 V for the photodiode bias. The per-channel power consumption was 79 mW.

Fig. 8 shows an expanded view of the eye-diagrams at various bitrates (10, 15, 17.5, 20 and 22 Gb/s) for one RX channel and one TX channel. Open-eye performance is clearly evident up to 20 Gb/s for both TX and RX, with appreciable eye closure seen at 22 Gb/s.

The sensitivity characteristics of the RX channels were measured at various data rates under the same operating conditions used to obtain the eye diagrams in Figs. 7 and 8 (79 mW/ch power consumption). The results for 12 typical channels are presented in Fig. 9 for data rates of 15, 17.5 and 20 Gb/s. The mean sensitivity for the 12 channels at a BER of 10^{-12} at 15 Gb/s is about -10 dBm. At the higher data rates, the average sensitivity decreases to about -7.5 dBm at 17.5 Gb/s and -4 dBm at 20 Gb/s. The best channels (not shown) achieved sensitivities of -11 dBm, -8.5 dBm and -6 dBm at 15, 17.5 and 20 Gb/s, respectively.

The sensitivity characteristics at 20 Gb/s for all 24 RX channels are shown in Fig. 10. Operation at $\mathrm{BER} < 10^{-12}$ was obtained for all channels. The spread in sensitivity is approximately 3.5 dB, higher than the <1.5 dB spreads exhibited at the lower data rates of 17.5 and 15 Gb/s. With all 24 TX and

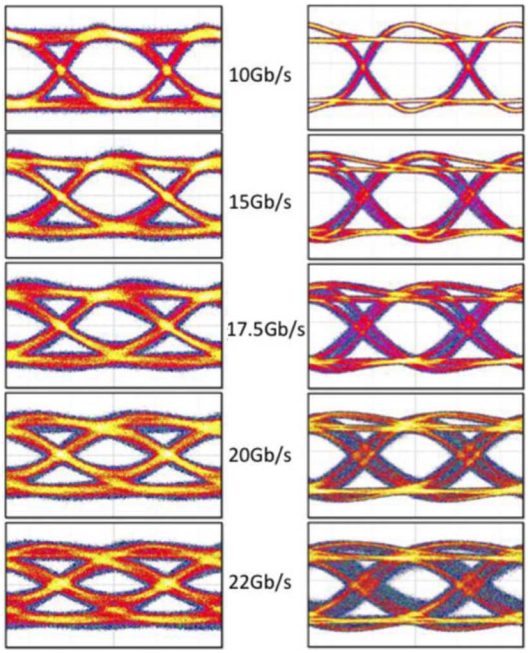

Fig. 8. Transmitter (left) and receiver (right) eye diagrams at varying data rates from 10 Gb/s to 22 Gb/s. The horizontal full scale of the eye diagrams spans two full bit periods: namely, 200, 133, 114, 100, and 91 ps at the five data rates of 10, 15, 17.5, 20, and 22 Gb/s, respectively.

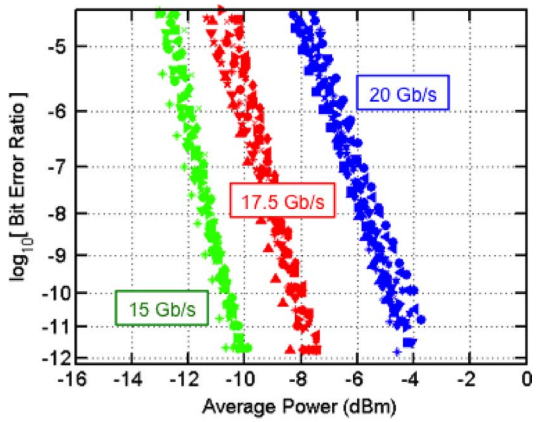

Fig. 9. Sensitivity curves for 12 typical Optomodule receiver channels at 15, 17.5 and 20 Gb/s.

RX channels operating at 20 Gb/s, the holey Optomodules provide an aggregate data rate of 480 Gb/s TX+480 Gb/s RX while consuming only 7.3 pJ/bit.

B. Cross-Talk Measurements

Minimizing inter-channel crosstalk is a significant challenge for single-chip transceivers, which is only exacerbated by the density achieved here. Three types of crosstalk are of primary concern: TX-to-RX, TX-to-TX, and RX-to-RX, since RX-to-TX crosstalk is much less problematic given the larger amplitude of the TX signals compared to the RX signals and the physical separation between the TX and RX circuits. Of these three, only RX-to-RX crosstalk has been observed in previous implementations of our single-chip transceivers [12]. As a result, the RX-to-RX crosstalk within the Optochip was characterized by observing degradation in receiver sensitivity

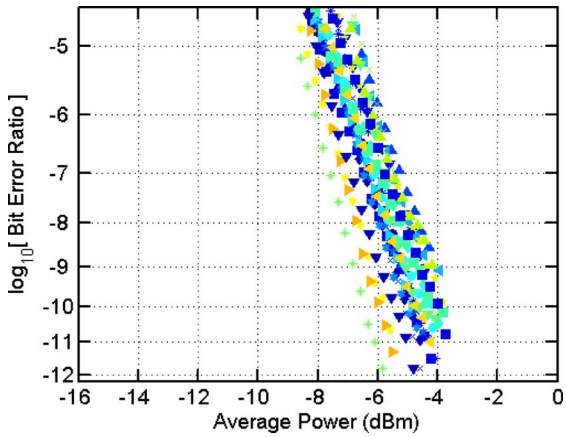

Fig. 10. Sensitivity curves for all 24 Optomodule receiver channels at 20 Gb/s.

and timing margin of one victim (V) channel when nearby aggressor (A) channels are operating at high speed. In this manner, the crosstalk-induced reduction in both vertical and horizontal eye opening is captured, providing a complete accounting of potential eye closures. For these crosstalk measurements, only the RX portion of the Optochip was powered up (all 24 channels) in order to minimize temperature-related effects associated with full $\mathrm{TX} + \mathrm{RX}$ power consumption (see Section III.C). Note that all circuit implementations use analog CMOS circuitry leading to constant power dissipation regardless of high-speed modulation signals.

The setup for performing the crosstalk measurements was identical to the setup used for RX characterization, except that additional asynchronous aggressor channels were provided by a reference 12-channel, 850-nm transmitter with data inputs supplied by the 12-channel test station described in [13]. The aggressor channels were operated at 10.3 Gb/s with a pseudo-random 64 b/66 b-encoded pattern. The lensed multi-channel fiber module described in Section III.D was used to couple the victim and aggressor channels into the RX simultaneously. The optical power present at the input to each aggressor RX channel was set to approximately -5 dBm, which is 5 dB and 2–3 dB above the receiver sensitivity points at 15 Gb/s and 17.5 Gb/s, respectively. This represents a worst-case configuration for parallel point-to-point links, since all channels typically share similar losses. For the amplitude margin curves, the power on the victim channel alone was varied using an optical attenuator, while for the timing margin curves, the victim channel was held at a constant power of -5 dBm.

Fig. 11 shows the resultant measurements comparing operation when receiving the victim channel alone (1 CH) to operation when receiving the victim channel in addition to the eleven aggressor channels (12 CH). The results are shown when the victim channel is operated at both 15 Gb/s and 17.5 Gb/s. At 15 Gb/s minor penalties of 0.3 dB in amplitude and 0.02 UI in timing are observed in the presence of the aggressor channels. At 17.5 Gb/s more significant penalties of 0.8 dB in amplitude and 0.03 UI in timing are observed.

In order to understand the cause of the crosstalk penalties at 17.5 Gb/s, BER curves were taken exciting aggressors in a variety of configurations (Fig. 12). Under investigation was

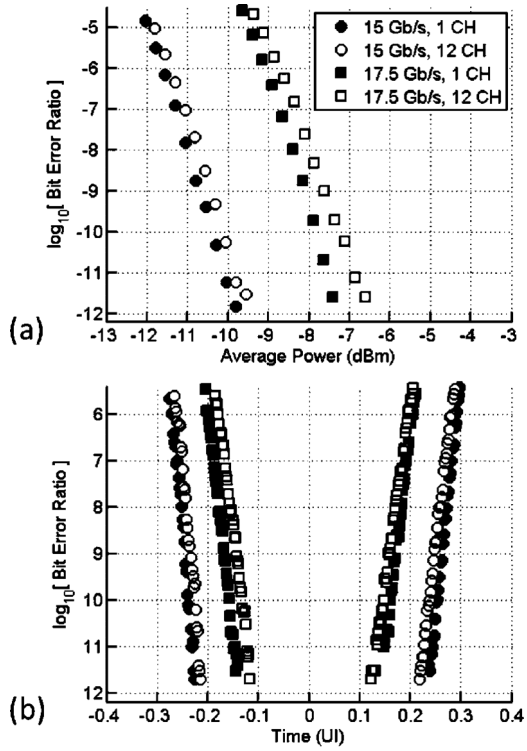

Fig. 11. (a) BER sensitivity curves and (b) bathtub curves showing the effect of RX-to-RX crosstalk on the amplitude and timing margins of one channel when the eleven other channels within the bank are receiving signals. The curves are shown for 15 Gb/s and 17.5 Gb/s operation.

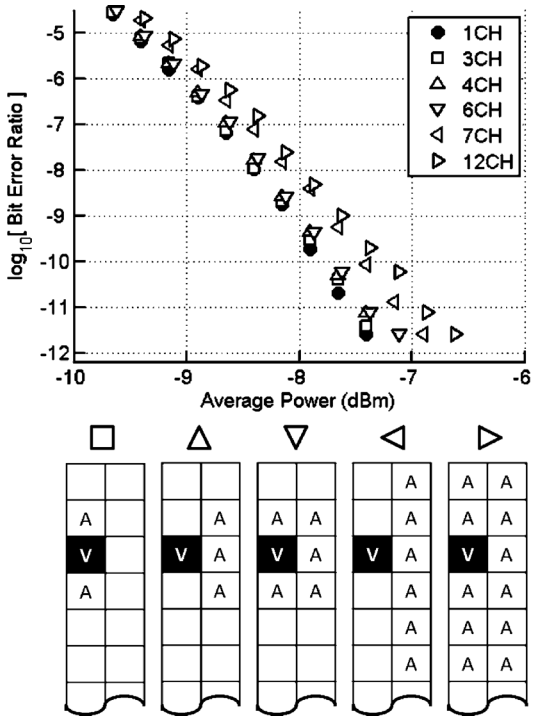

Fig. 12. BER curves showing the crosstalk penalty using different configurations and different numbers of aggressor channels.

whether crosstalk was correlated with the operation of nearest neighbor channels, nearest neighbor channels in the opposing row which routes transmission lines nearest to the victim channel, or only with the amount of aggregated aggressor input power. The results exhibit a negligible penalty compared to the victim-only measurement when operating only a few nearest neighbor channels, regardless of whether those aggressors are in the same row or the opposing row of the victim channel. However, as more aggressor channels are added, the penalty increases proportionately with the amount of aggregate aggressor power, irrespective of the aggressor channel location.

One possible explanation of the observed phenomena would be crosstalk incurred within the chip's power delivery system. The measurements were carried out with power supplied to all 24 RX channels but the experimental apparatus is limited to a maximum of 12 independent high-speed aggressors [13]. Although the remaining 12 channels are in distant banks with independent bias/control signals, they may contribute additional cross-talk penalties when receiving high-speed data. This crosstalk penalty due to switching noise can be readily reduced in future transceiver designs through more robust power delivery networks incorporating additional decoupling capacitors. This result demonstrates that nearest neighbor single-channel crosstalk measurements are insufficient to properly characterize a dense high-channel count transceiver.

C. Thermal Measurements

The thermal environment of the Optochip during operation has an impact on the performance and reliability of the Optomodule and thermal management is required for optimum performance. A 17 mm $\times$ 17 mm $\times$ 6 mm aluminum heat spreader, same area as the module, is used to remove the heat from the Optochip. It includes a 4 mm $\times$ 3.2 mm central opening to allows access to the optical vias while simultaneously providing thermal contact to the peripheral $\sim$1 mm edges of the Optochip. The complete Optomodule packaging includes attachment of a finned heat sink and applying moderate air flow.

The operating temperature of Optochip as a function of electrical power dissipation was measured in order to access Optomodule performance under typical operating conditions. Fig. 13 shows the backside chip temperature versus the electrical power dissipated by the bare Optochip as well as for the fully packaged Optomodule. The Optochip, and therefore Optomodule, consumes about 3 W under nominal operating conditions with all 24 TX and 24 RX channels active. For the Optomodule with a bare Optochip (no thermal management), the backside of the IC rises to a temperature of 90°C. Adding the thermal management solution described above reduces the backside chip temperature by about almost 30°C to an operating temperature of about 60°C.

Earlier studies of single-chip CMOS transceivers with flip-chip attached OE arrays found negligible degradation in TX performance for operation at temperatures as high as 70°C [14]. However, some degradation was evident in RX performance at elevated temperature. The operating temperature of the Optochip was varied by adjusting the power consumption through individual control of the TX and RX banks, as illustrated in Fig. 13, and the performance of the RX Optomodule channels were characterized as a function of temperature. This effect was quantified by measuring the sensitivity of a typical RX channel

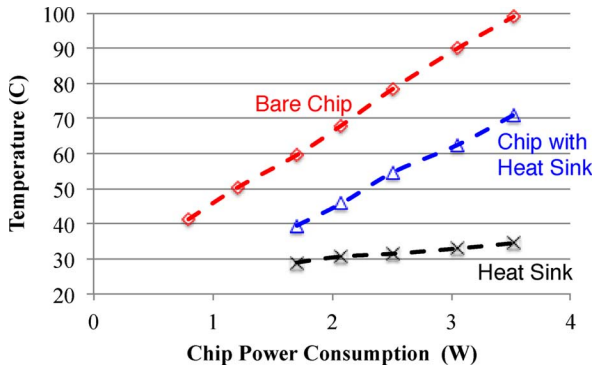

Fig. 13. Optochip temperature vs. power consumption for an Optomodule with bare Optochip and a fully packed module with heat sink and air flow.

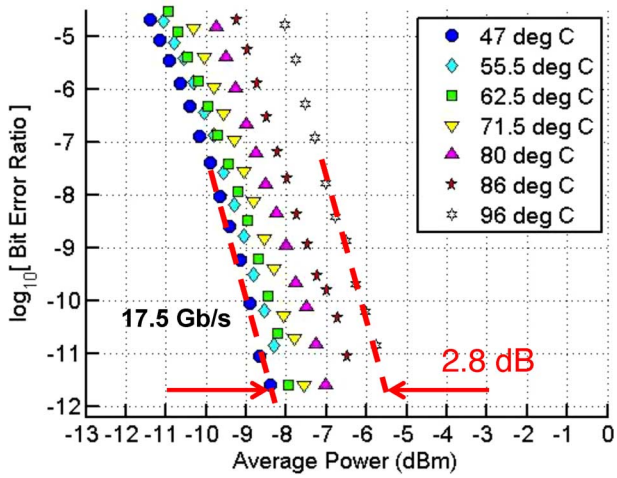

Fig. 14. Sensitivity for typical receiver channel at elevated temperatures.

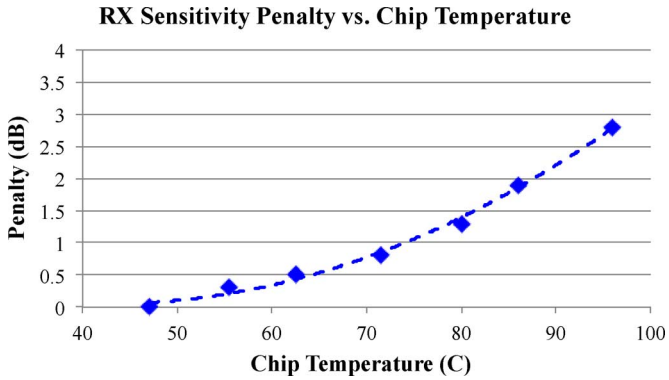

Fig. 15. Sensitivity penalty for typical receiver channel at elevated temperature.

as a function of temperature for data rate of 17.5 Gb/s, and the results are presented in Fig. 14. Compared to operation at 47°C, the RX channel shows a sensitivity degradation of about 2.8 dB when the chip temperature is increased to 96°C.

A summary of the measured penalty as a function of temperature is shown in Fig. 15. Operation at temperatures up to 70°C incurs more modest penalties less than 0.7 dB. A minimal penalty of <0.5 dB can be realized when the IC operating temperature is maintained at <62°C, which can be readily achieved using a heatsink with mild air flow.

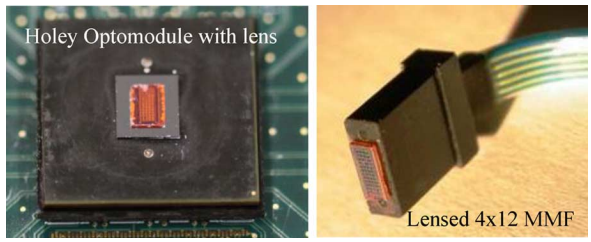

Fig. 16. Optomodule and MMF ferrule with attached lens arrays.

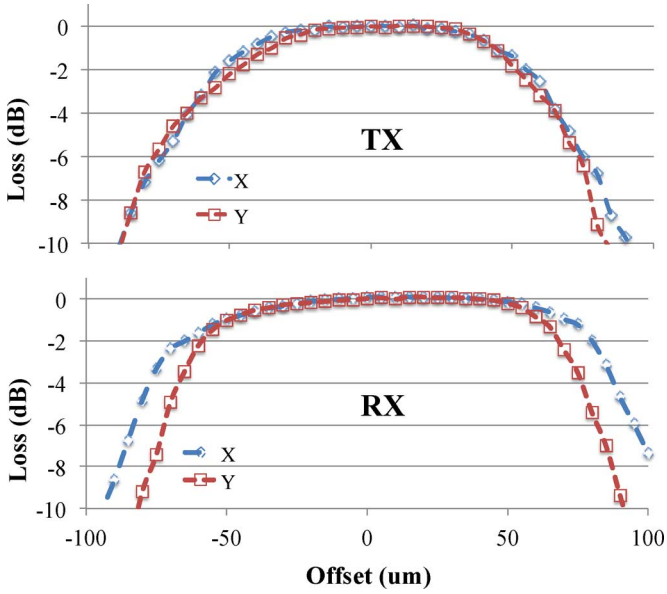

Fig. 17. Measured TX and RX coupling efficiency as a function of MMF array offset relative to Optomodule.

D. Optical Coupling

The OE devices are arranged on a 4×12 array with 250 μm $\times$ 250 μm pitch to match standard MMF arrays. A dual lens optical system is used to couple light to/from the OE devices to the fiber array, and is described in detail elsewhere [6], [7], [12]. Briefly, two 4×12 lens arrays are used, with the first lens array integrated onto the Optochip while the second lens array is attached to the MMF ferrule. The optical system is designed to provide approximately $1.5\times$ magnification form the OE devices to the MMF and to provide nearly collimated light between the two lenses. For the TX, the optical system magnifies the VCSEL image onto the 50-μm core MMF while simultaneously reducing the numerical aperture by $1.5\times$ to provide efficient optical coupling. For the RX path, the fiber core image is reduced by $1.5\times$, allowing more efficient coupling to smaller-diameter high-speed photodiodes.

Two lens arrays were fabricated using high-index GaP substrate and attached to the Optochip and to the ferrule of a 4×12 MMF array, as seen in Fig. 16. A primary advantage of the dual-lens optical system is the relaxed alignment tolerances resulting from the nearly collimated light between the 2 lenses. The measured optical coupling dependence on in-plane x- and y-offsets between the lensed Optomodule and lensed MMF array are shown in Fig. 17.

For the TX, the results show that coupling efficiency better than -1 dB can be achieved for up to ± 40 μm alignment offsets. For the RX Optomodule with 30 μm photodiodes, the dependence on alignment offset shows $>\pm 55$ μm tolerances at -1 dB coupling efficiency. The optical coupling and alignment tolerance measurements demonstrate the high coupling efficiency and relaxed assembly tolerances of the dual-lens optical system.

IV. Conclusion

We have reported on the successful demonstration and characterization of second-generation optical transceiver module based on a holey Optochip. The holey Optochip is a highly-integrated chip-like package with flip-chip attached industry-standard 850-nm VCSEL and PD arrays and incorporating optical vias for optical access through the backside of the Optochip. The 24 TX+24 RX Optochip is packaged into a complete Optomodule by flip-chip soldering to a high-density, high-speed organic carrier that is further attached to pluggable connector.

High-speed characterization of Optomodules plugged into test cards showed good performance for all 24 TX channels and all 24 RX channels up to 20 Gb/s, with select channels operating up to 22 Gb/s. Cross-talk measurements show minor penalties at 15 Gb/s and a measured (12-ch) worst-case receiver penalty of 0.8 dB at 17.5 Gb/s. Analysis of the cross-talk results suggest this penalty can be reduced in future transceiver designs with enhanced power delivery networks. Thermal studies reveal additional receiver penalties at elevated temperatures, although proper thermal management can limit this to <0.5 dB for 48-channel operation. Additionally, efficient optical coupling with relaxed alignment tolerances was demonstrated using a dual-lens optical system, with one lens integrated onto the Optochip and a second onto the MMF ferrule. The Gen2 Optomodule included enhancements in CMOS IC, OE arrays, and packaging which provided 60% improvement in bandwidth, 11% lower energy/bit, and 24% reduction in module area compared to Gen1 module. The Optochip also achieves a record bandwidth density of 31.8 Gb/s/mm^2 for the entire Optochip and 79.5 Gb/s/mm^2 when considering only the area devoted to circuits and OEs (excluding C4 pads). At 20 Gb/s per channel, the holey Optomodule can provide an aggregate data rate of 0.48 Tb/s TX plus 0.48 Tb/s RX with an unprecedented power efficiency of 7.3 pJ/bit (TX+RX). The 1 Tb/s data transfer rate is also a record for parallel optical transceivers.

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