Final Exam, ECE 137A

Thursday March 20, 2025, Noon- 3 p.m.

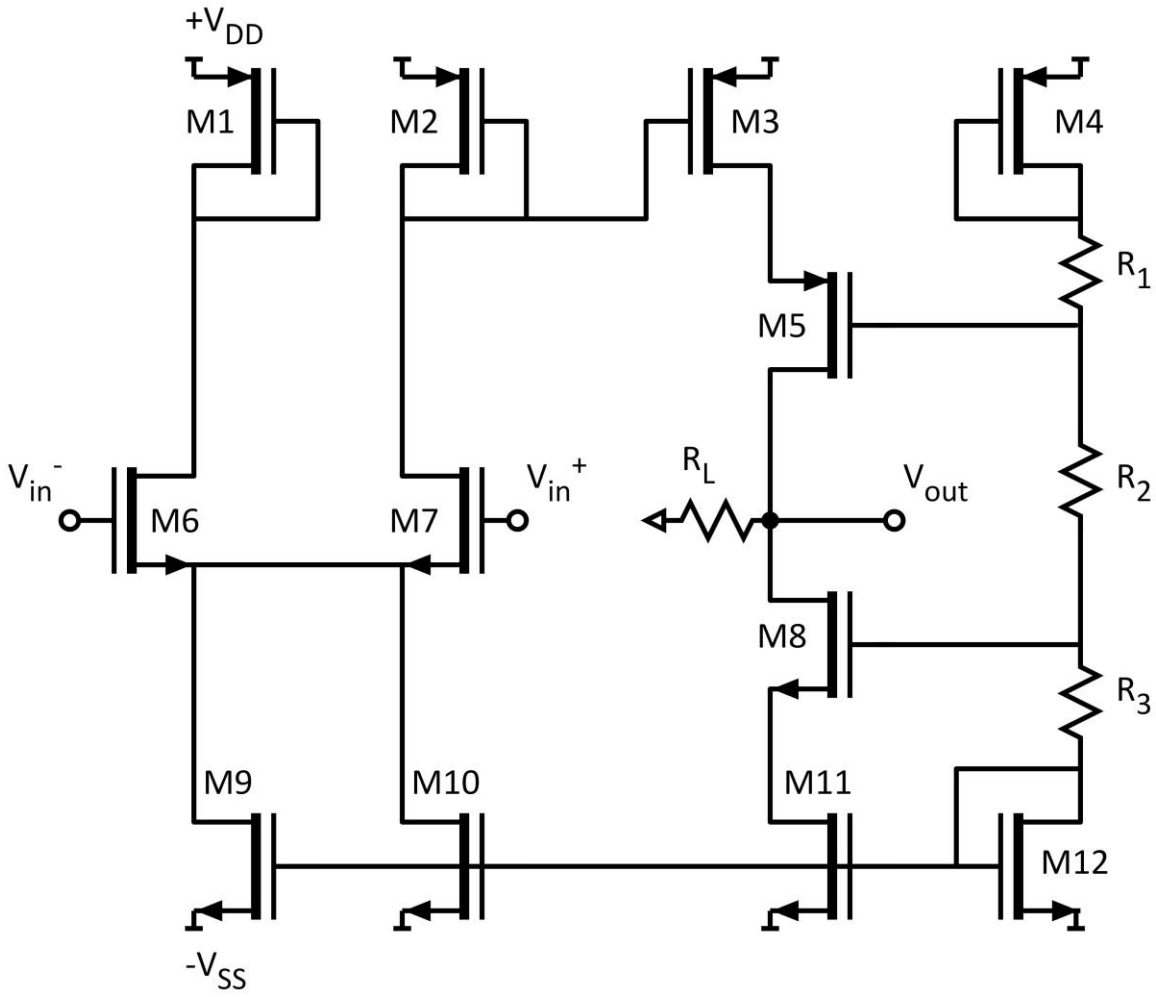
Name: _____

Closed Book Exam:
Class Crib-Sheet and 2 pages (4 surfaces) of student notes permitted
Do not open this exam until instructed to do so. Use any and all reasonable approximations (5% accuracy), ***after stating & justifying them***.
Show your work:
Full credit will not be given for correct answers if supporting work is missing.
Good luck

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		5	2b		5
1b		5	2c		15
1c		5	2d		10
1d		12	3a		5
1e		8	3b		10
1f		10	3c		5
2a		5			
total		100			

Problem 1, 45 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts.



The NMOSFETs have $K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$ $K_v = 2.0\text{mA/V} \cdot (W_g / 1\mu\text{m})$, $\Delta V = 0.10\text{V}$, $V_{th} = 0.2$ V, $1/\lambda = 5$V. The PMOS have identical parameters, except, of course, V_{th} is negative. V_{DD} = +0.8 V, $-V_{SS}$ = -0.8 V

All transistors have |Vgs|=0.3V.
M1,2,6,7,9,10 are biased at I_D=20 μA.
M3,5,8,11,4,12 are biased at I_D =100 μA.
The IR voltage drops across R_1 and R_3 are each 200 mV.
R_L=10 kΩ.

a

Part a, 5 points

DC bias

Find the following:

Gate width of M2 = _____

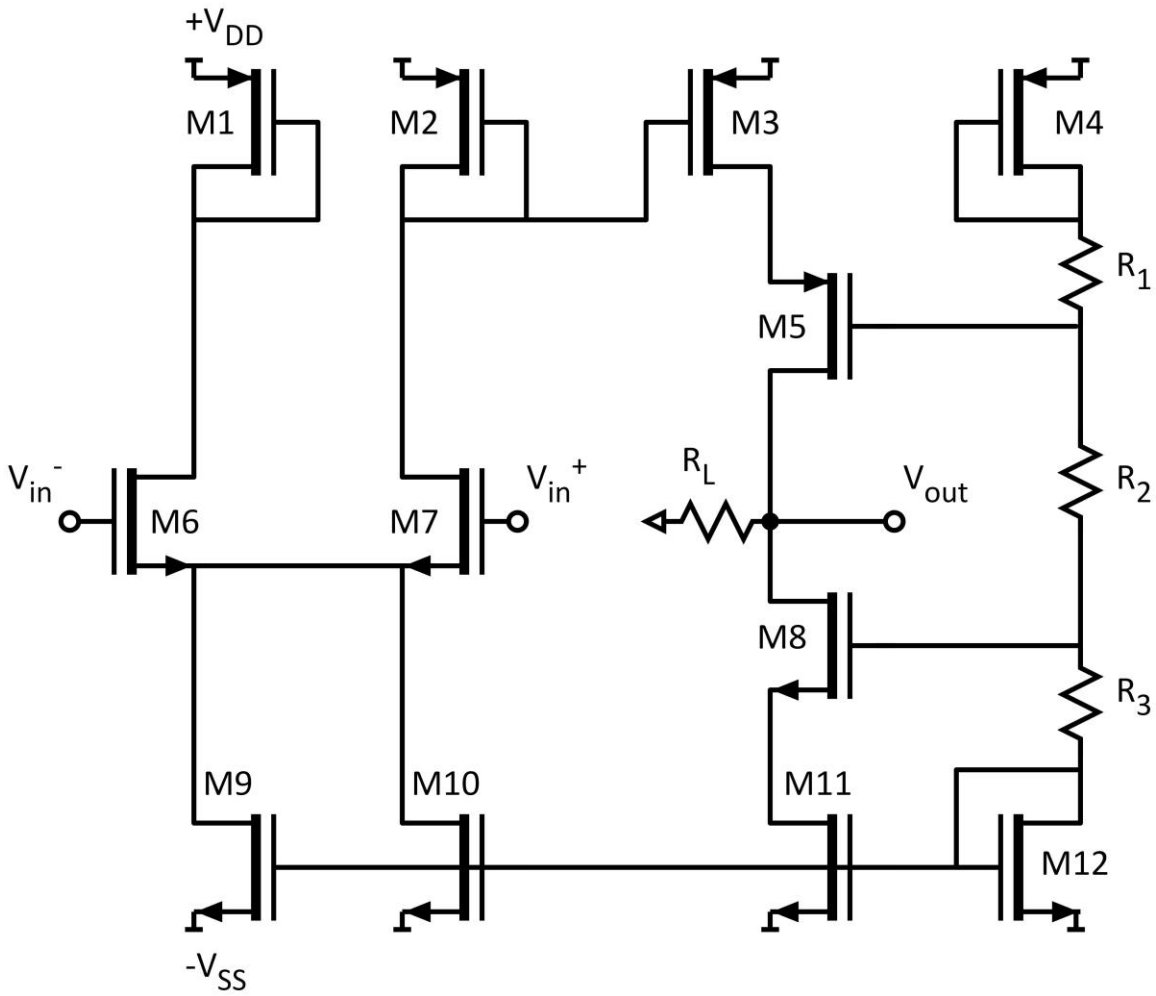
Gate width of M3 =_____

Value of R_1 =_____

Value of R_2 =_____

Part b, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes**.

Part c, 5 points

Find the following

MOSFET M6 g_m =_____ R_{DS} =_____

MOSFET M7 g_m =_____ R_{DS} =_____

MOSFET M2 g_m =_____ R_{DS} =_____

MOSFET M3 g_m =_____ R_{DS} =_____

MOSFET M5 g_m =_____ R_{DS} =_____

MOSFET M8 g_m =_____ R_{DS} =_____

MOSFET M11 g_m =_____ R_{DS} =_____

a

Part d, 12 points.

Find the following

	Voltage Gain	Input impedance
Transistor combination M3,5,8,11		

Note: You can analyze M3 and M5 as separate stages, or as a combined stage using Norton/Thevenin methods. Don't ask for hints as to how to do this.

Part e, 8 points.

Find the following

	Voltage Gain	Input impedance
Transistor combination M1,2,6,7,9,10		
Overall op-amp $V_{out} / (V_{in}^{+} - V_{in}^{-})$		

Hint: although M2 is a diode-connected FET, the small-signal resistance of this 2-terminal element, although mostly determined by the FET transconductance, also has a slightly contribution from the FET R_{DS} .

Part f, 10 points

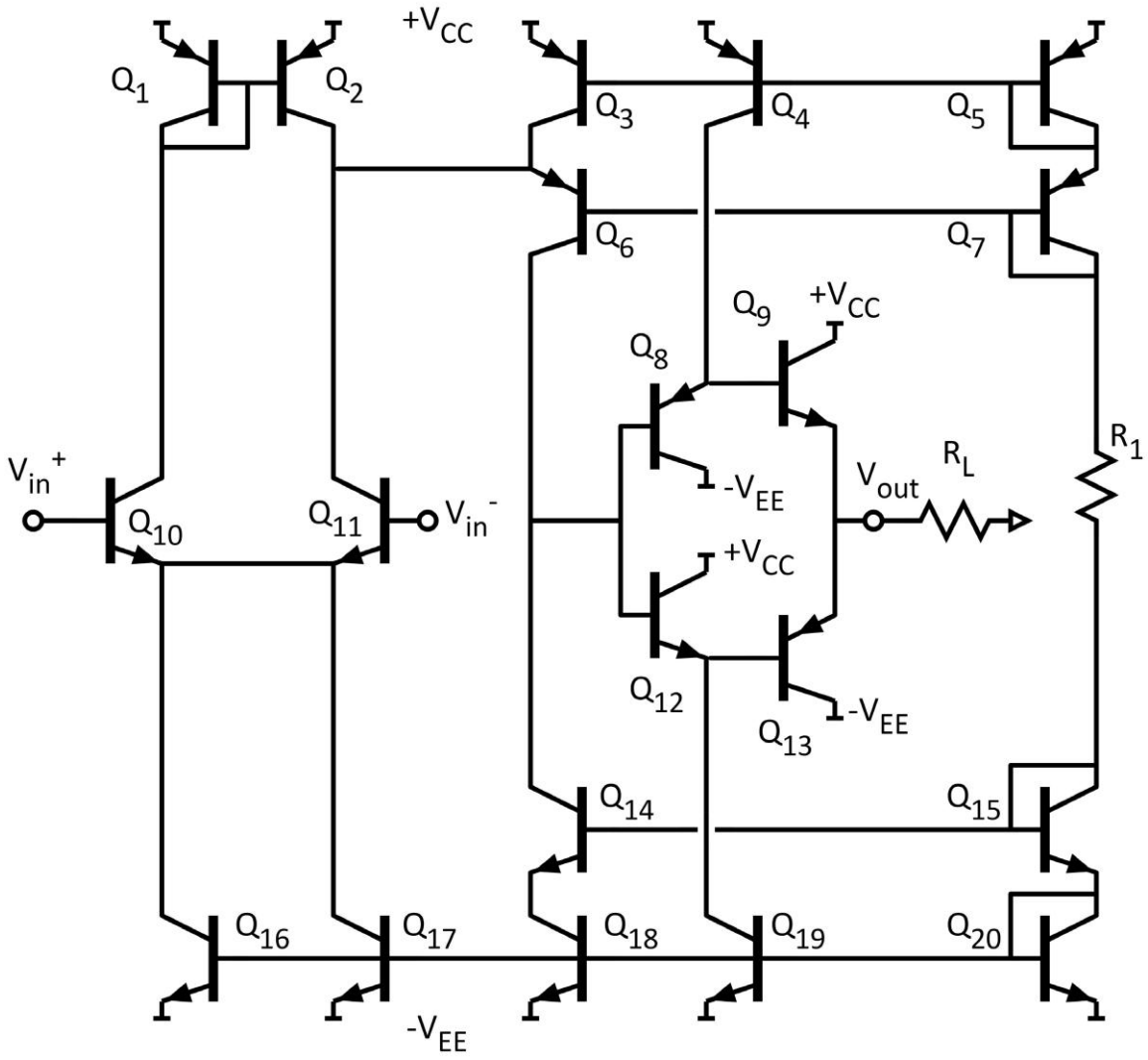
Maximum output voltage swings (***show all your work***).

	magnitude and sign of maximum output signal swing due to ***cutoff***	magnitude and sign of maximum output signal swing due to ***knee voltage***
Transistor M6		Do not calculate
Transistor M7		Do not calculate
Transistor M3		Do not calculate
Transistor M5	Do not calculate	
Transistor M8	Do not calculate	

a

Problem 2, 35 points

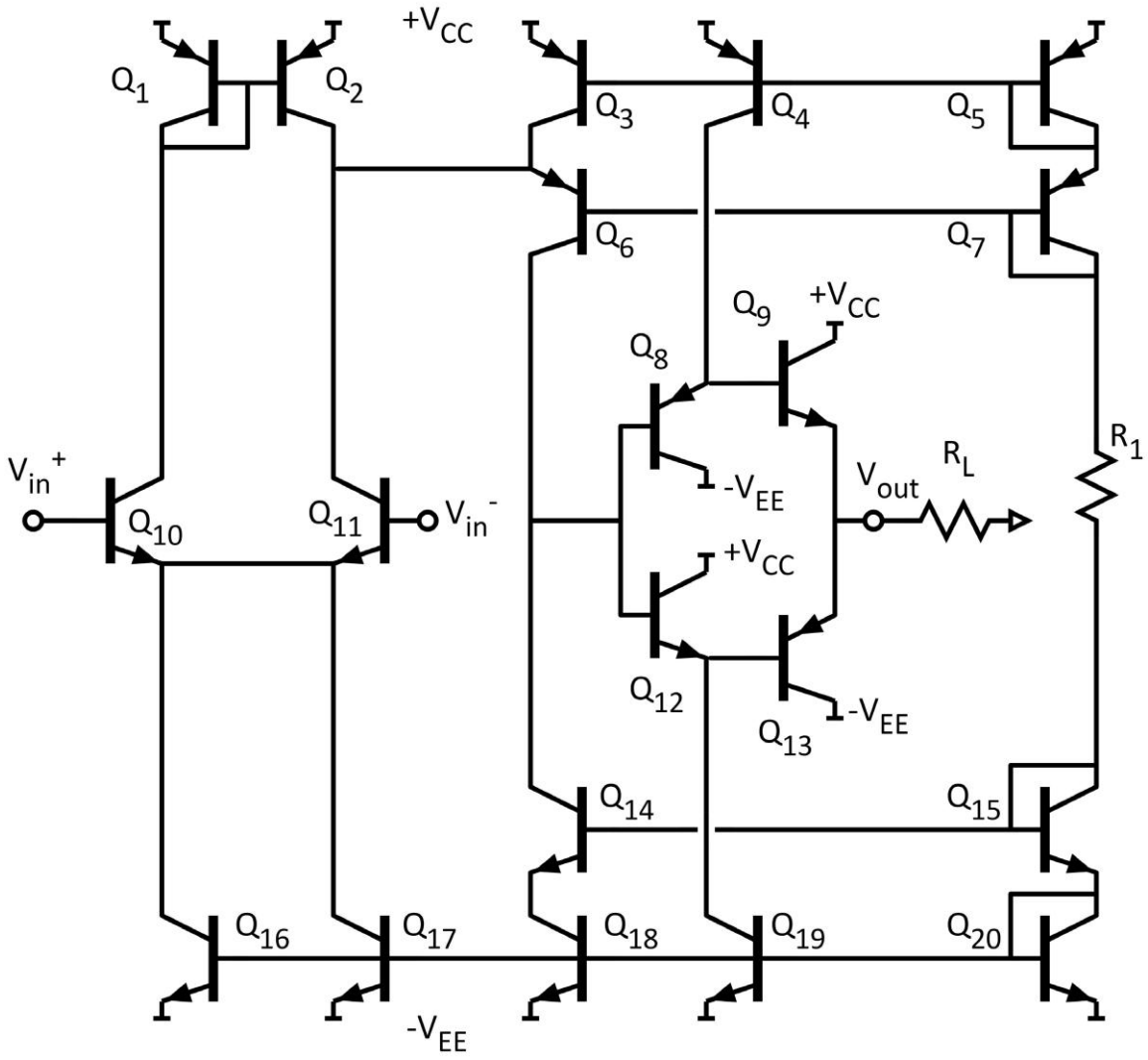
This is an Op-Amp---analyze the bias under the assumption that DC output voltage V_{out} is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.



All the transistors have the same (matched) I_S, have $\beta = \infty$, and $V_A = 100$ Volts.
$V_{CE(sat)} = 0.5\text{V}$. V_{be} is *approximately* 0.7 V, but use the *exact relationship*
$V_{be} = (kT/q)\ln(I_E / I_S)$ when appropriate. The supplies are +5 Volts and -5 Volts. All transistors have the same I_S, and all are biased at 0.1 mA collector current.
R_L=1 kOhm.

Part a, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes.**

a

Part b, 5 points.

Find the following

	Voltage Gain	Input impedance
Transistor combination Q8,9,12,13		

a

Part c, 15 points.

Find the following

	Voltage Gain	Input impedance
Transistor combination Q1,2,10,11,6		
Overall op-amp $V_{out} / (V_{in}^{+} - V_{in}^{-})$		

Note: You can analyze (Q1,2,10,11) and Q6 as separate stages, or as a combined stage using Norton/Thevenin methods. Don't ask for hints as to how to do this.

a

Part d, 10 points

Maximum output voltage swings (***show all your work***).

	magnitude and sign of maximum output signal swing due to ***saturation voltage*** (saturation)
Transistor Q4	
Transistor Q9	

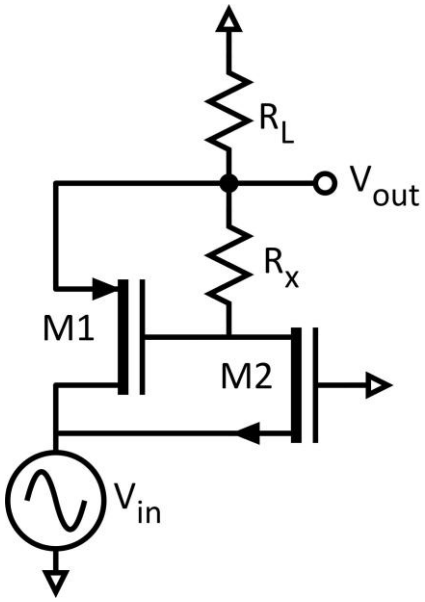
Note that transistors Q13 and Q19, Because of the circuit symmetry, Will give similar answers but with a change in sign.

a

a

a

Problem 3, 20 points



You will be working on the circuit to the left

Ignore DC bias analysis. You don't need it.

M_1 and M_2 have transconductances g_{m1} and g_{m2}.

Both transistors have **infinite** R_{DS} ,
...so you don't need to include these elements in the circuit diagram !

Part a, 5 points

Draw a small-signal equivalent circuit of the circuit.

a

Part b, 10 points

Derive an algebraic expression for V_{out} / V_{in} in terms of g_{m1}, g_{m2}, R_L, and R_X

V_{out} / V_{in} =

a

a

Part c, 5 points

Set g_{m1} =1 mS, g_{m2} =2 mS , R_L =3 kΩ, and R_X = 5 kΩ.
Find the numerical value of V_{out} / V_{in}

V_{out} / V_{in} =

a

a