Problem 1: The supplies are +/- 5 V. The transistors all have beta=100 and Va=100 Volts. The Emitter resistors (Re3 and Re4, Ree8, Ree9) all have 150 mV DC voltage drop. Ri=10 kOhm. RL=2 kOhm. Ree5=Ree6=100 Ohm.

The DC input voltages are 0 V, the DC output voltage is to be 0 V. Q1 and Q2 are biased at 200 uA, Q5 and Q6 at 2 mA, and Q7 at 5 mA. Q9 has a Vce of 0.7 Volts. Find all bias values, all resistor values, the differential and common-mode voltage gains, the CMRR, and the output impedance.

Problem 2:
The NMOS FETS have 0.8 nm equivalent* oxide thickness, 22 nm gate length, and a 0.25 V threshold. Mobility is 400 cm²/(V·s), $v_{inj} = 10^7$ cm/s and $1/\lambda=25$ V. The PMOS FETs are the same. The sign of the PMOS threshold voltage is of course reversed.

The FETs are to all operate at Id1=Id2=50 uA, Id5=Id6 Id8=Id9=500 mA. Ic3=Ic4. Ic10=1mA. Pick the FET widths so that all FETs operate at Vgs corresponding to the boundary between mobility-limited and velocity-limited operation.

The voltage drops across Re3 and Re4 are 150 mV. The supplies are +/- 2 V, and the gates of Q8 and Q9 are at +0.5 V. The load is 5000 Ohms

Ignore the effect of lambda in the DC analysis but not the AC analysis.

Vin- and Vin+ are at zero volts DC, as is Vout. The BJTs have beta=200. RgA is 1 MOhm.

*meaning----we don't know what the actual oxide thickness is, but we will get the correct answer if we assume a thickness of 0.8nm and the 3.8 dielectric constant of SiO2.