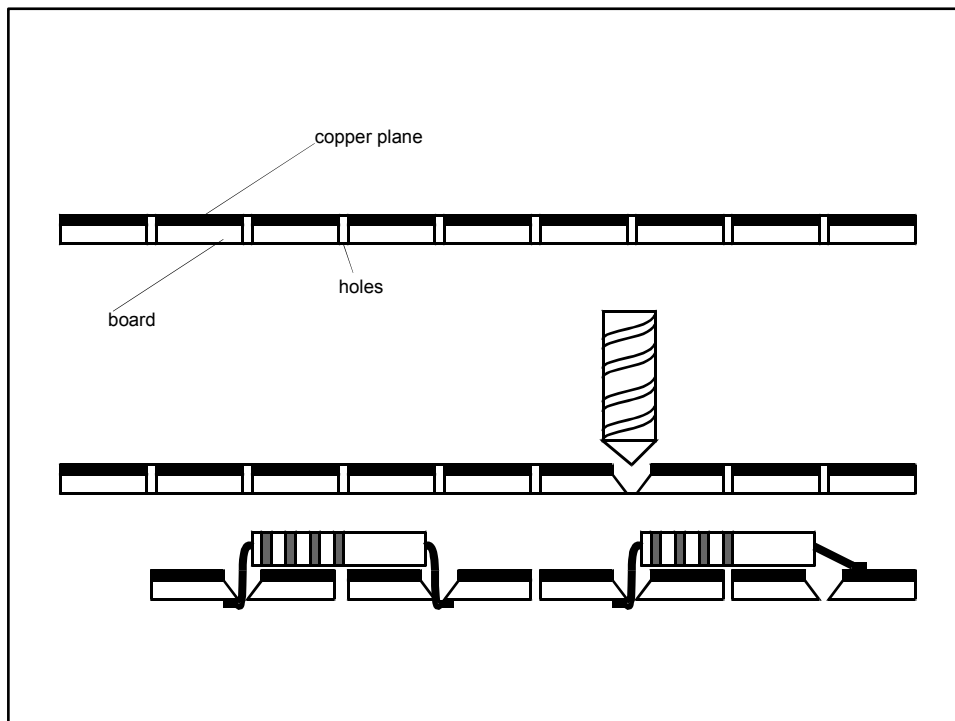


Comments on lab project #2.

Construction:

Copper-clad ground-plane circuit board

build the circuit on the copper-plated "perfboard" (a board with a pre-drilled array of holes at 0.1" spacing, coated one side with copper). Components leads are passed through the board...they will short to the ground plane. To avoid this, grab a small drill bit in your fingers, and use it to bevel the holes, as shown. Wires to ground are soldered directly to the ground plane. Wiring between components can be done by running wires and soldering them to parts. Or, you can run wiring traces on the board using thin strips of sticky copper tape...the shop usually stocks this. The glue on the tape does not conduct, so joints between copper tape strips must be soldered.



Not Copper-clad ground-plane circuit board

If this seems too hard, use the usual unclad board. But, make a ground plane on it by using a WIDE strip of sticky copper tape. Use this for all your ground connections.

Generally

Input and output connections: use solder-to-board coaxial cable connectors from the shop. Use power supply bypass capacitors. Solder wires to the board to connect power. Wrap the +V/Ground/-V power wires together into a single twisted "rope".

Circuit Design.

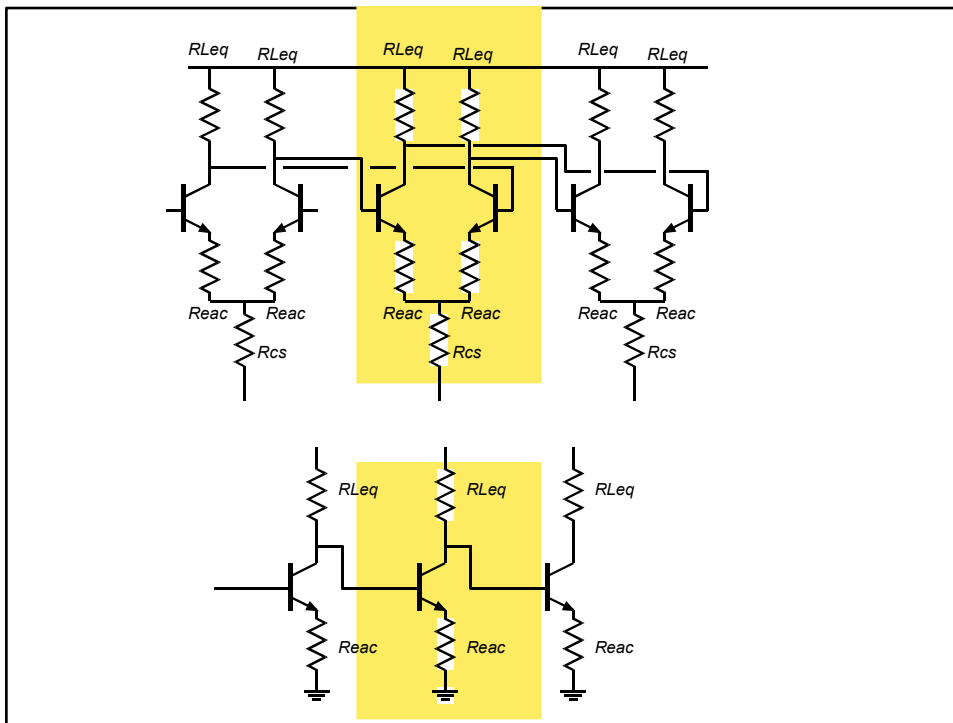
General concepts

We need to have a general idea of the problem.

Your overall bandwidth will be

$$f_{high} = 1/2\pi a_1,$$

where a_1 can be found by the method of first-order time constants. This can be done for a multi-stage circuit, capacitor by capacitor, just like a single stage circuit. Let's start by considering a series of differential stages, and their half-circuit equivalent, below. You are warned that the circuit below has problems with DC biasing. Further, please note that this multistage differential amplifier has *both* outputs driving *both* inputs of the next stage...something which we *don't* have to do.



Note that the degenerated Cpi of a transistor is

$$\tilde{C}_\pi = C_\pi \frac{r_e}{R_{eac} + r_e} \quad \text{but } C_\pi = \frac{0.159}{r_e f_\tau} - C_{cb}, \text{ so } \dots$$

$$\tilde{C}_\pi = \frac{0.159}{(R_{eac} + r_e) f_\tau} - C_{cb} \frac{r_e}{r_e + R_{eac}} \approx \frac{0.159}{(R_{eac} + r_e) f_\tau}$$

So, if we want small values of C_pi, we cant let (Reac+re) be very very small.

If we consider that the gain of a common-emitter stage is

$$\tilde{C}_\pi = \frac{0.159}{(R_{eac} + r_e) f_\tau} - C_{cb} \frac{r_e}{r_e + R_{eac}} \approx \frac{0.159}{(R_{eac} + r_e) f_\tau}$$

Then the dominant time constant arising from Cpi and Ccb of the middle transistor (the one highlighted in yellow) will be:

$$a_1 \sim \tilde{C}_\pi R_{Leq} + C_{cb} \left(1 + \frac{R_{leq}}{r_e + R_{eac}}\right) R_{Leq} = 0.159 \frac{R_{Leq}}{(R_{eac} + r_e) f_\tau} + C_{cb} \left(1 + \frac{R_{leq}}{r_e + R_{eac}}\right) R_{Leq}$$

$$a_1 \sim 0.159 \frac{A_v}{f_\tau} + C_{cb} (1 + A_v) R_{Leq}$$

The above formulas are rough, not exact. Don't use them for exact calculations.

But understand what this means.

If the 3 dB bandwidth is roughly

$$f_{high} \sim 0.159 / a_1 \quad \text{and} \quad a_1 \sim 0.159 \frac{A_v}{f_\tau} + C_{cb} (1 + A_v) R_{Leq}$$

Then

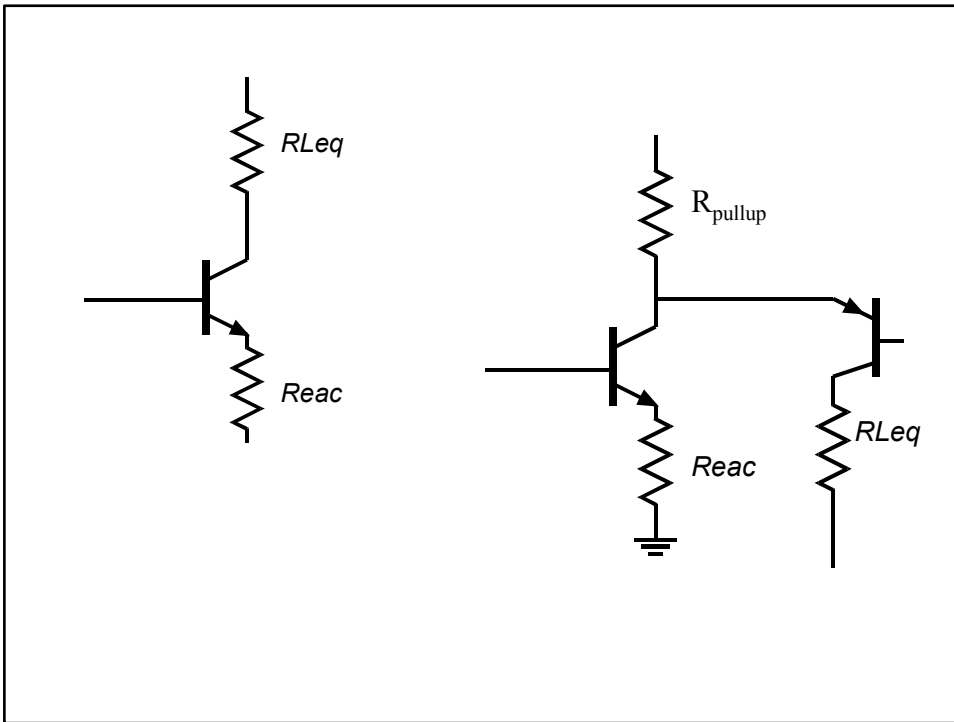
- 1) High gain-per-stage means low bandwidth
- 2) Miller multiplication is bad and should be avoided.

The 2 lessons are:

- 1) If you design for a large gain with one stage, it will probably have low bandwidth. The more stages you use, the lower the gain of each stage, and the higher its bandwidth.
- 2) One should try to avoid having bandwidth further hurt by Miller effect.

Circuit Design Strategies: cascodes.

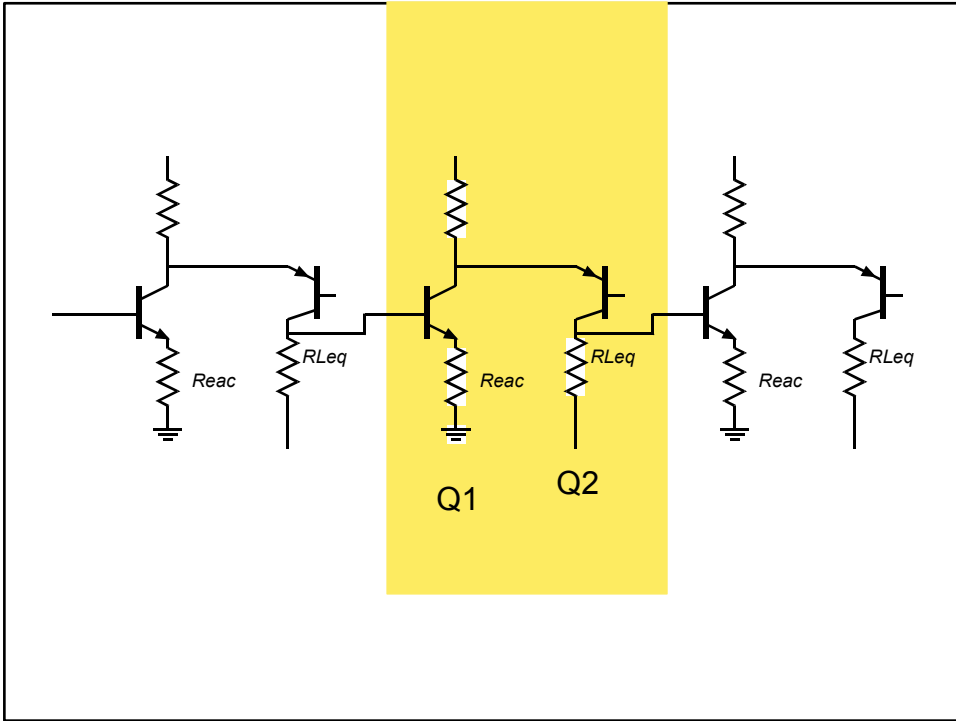
Consider replacing a single common-emitter amplifier with a cascode stage:



The gain of the CE stage is $A_v = R_{leq} / (r_e + R_{eac})$

The gain of the cascode stage is $A_v = \frac{R_{in_cb} \parallel R_{pullup}}{(r_e + R_{eac})} \frac{R_{leq}}{R_{in_cb}} \approx \frac{R_{leq}}{(r_e + R_{eac})}$,

which is the same as the CE stage. But, when you look at the time constants involved:



$$a_1 \sim \tilde{C}_{\pi 1} R_{Leq} + C_{cb1} \left(1 + \frac{R_{in2}}{r_e + R_{eac}}\right) R_{Leq} + C_{cb1} R_{in2} + C_{\pi 2} R_{in2} + C_{cb2} R_{Leq2}$$

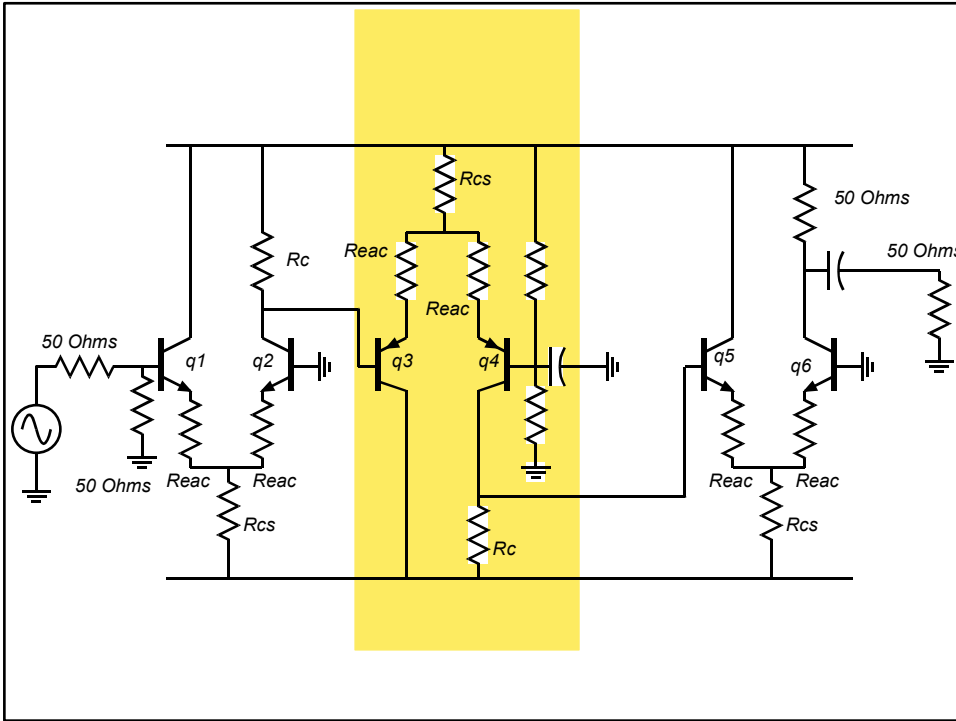
$$a_1 \sim 0.159 \frac{R_{Leq}}{(R_{eac} + r_e) f_{\tau}} + C_{cb1} \left(1 + \frac{R_{in2}}{r_e + R_{eac}}\right) R_{Leq} + C_{cb1} R_{in2} + C_{\pi 2} R_{in2} + C_{cb2} R_{Leq2}$$

Now, note that $(R_{in2})/(r_e + R_{eac})$ is probably much less than 1. And note that $R_{in2} \approx r_{e2} \ll R_{leq}$. So, if we drop the smaller terms:

$$a_1 \sim 0.159 \frac{R_{Leq}}{(R_{eac} + r_e) f_{\tau}} + C_{cb1} R_{Leq} + C_{\pi 2} R_{in2} + C_{cb2} R_{Leq2}$$

If we compare this to the common-emitter stage, we see that Miller multiplication terms have dropped .

Other design strategies: emitter-coupled pairs with single-ended connections



Here, note that that Q1 Q3 and Q5 do not have collector resistors. This is to Avoid miller effect. Q1, Q3, and Q5 operate as common collector stages and Q2, Q4, and Q6 as common-base stages. Considering Q3 and Q4 alone:

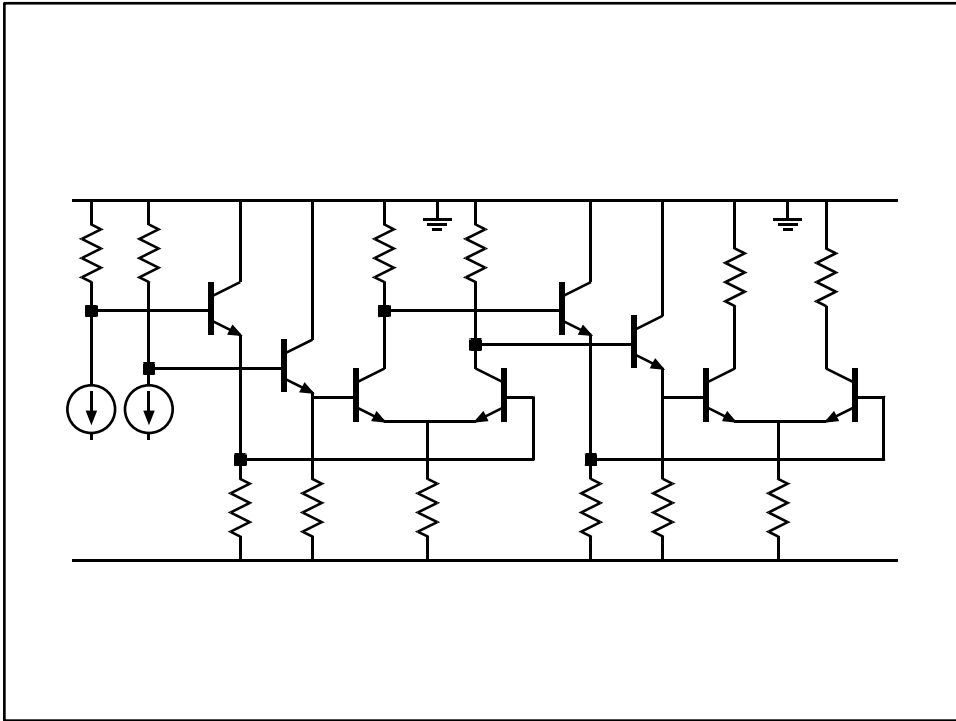
$$a_1 \sim \tilde{C}_{\pi 3}(R_c \parallel R_{in3}) + C_{cb3}(R_c \parallel R_{in3}) + C_{\pi 4}r_{e4} + C_{cb4}(R_c \parallel R_{in5})$$

where, once again,

$$\tilde{C}_{\pi 3} = \frac{0.159}{(R_{eac} + r_e 3)f_{\tau}} - C_{cb} \frac{r_{e3}}{r_{e3} + R_{eac}} \approx \frac{0.159}{(R_{eac} + r_{e3})f_{\tau}}$$

Other design strategies: emitter-coupled pairs with single-ended connections

This circuit I will not recommend for you...too many transistors. But, it is common in industrial practice....Miller multiplication here does occur, but the emitter-followers provide very low resistances through which to charge the miller-multiplied capacitors...so the resulting time constants are not so large.



AC coupling

Input blocking capacitors give low-frequency time constants of

$$\tau = (R_{gen} + R_{in})C$$

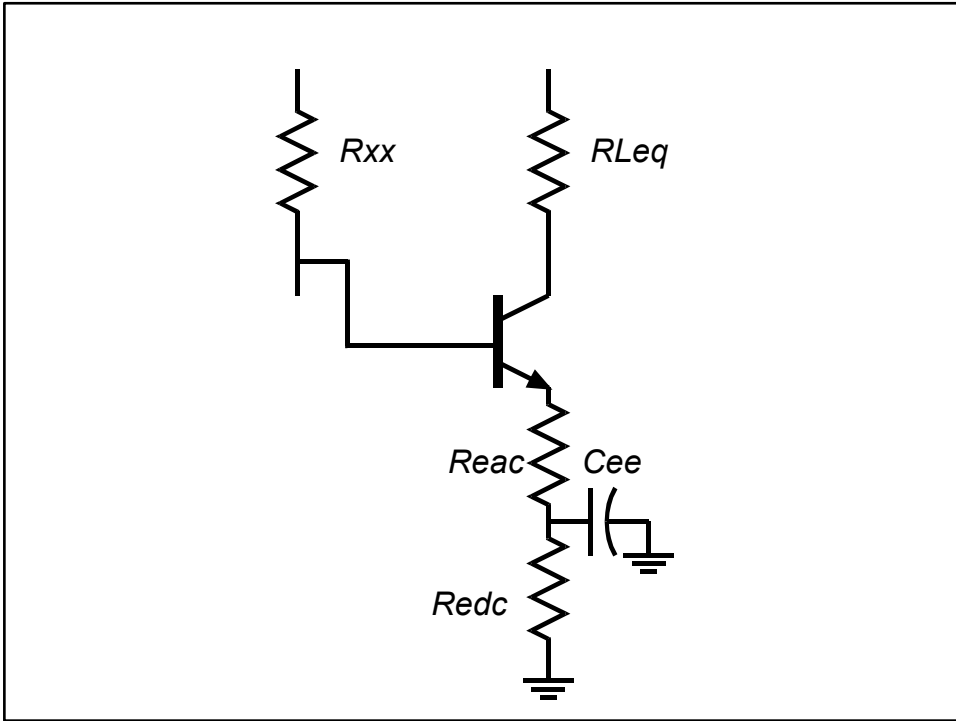
Interstage give time constants of

$$\tau = (R_{out,stage1} + R_{in,stage2})C_{between1and2}$$

and output blocking capacitors give

$$\tau = (R_{out} + R_L)C$$

Capacitors which by pass an emitter to AC ground give a time constant of



$$\tau = C_{ee} \left[R_{edc} \parallel \left\{ R_{eac} + r_e + \frac{R_{xx}}{\beta} \right\} \right] \dots \text{a result you can derive in 2 seconds by MOTC.}$$