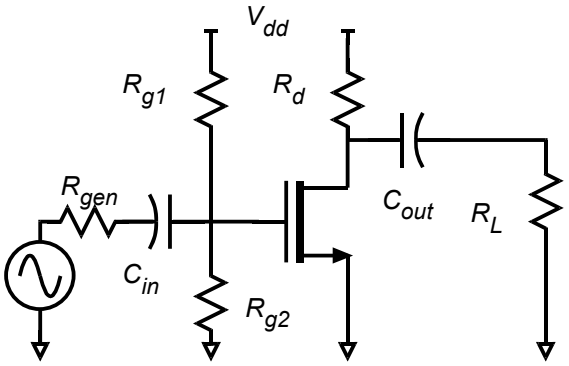
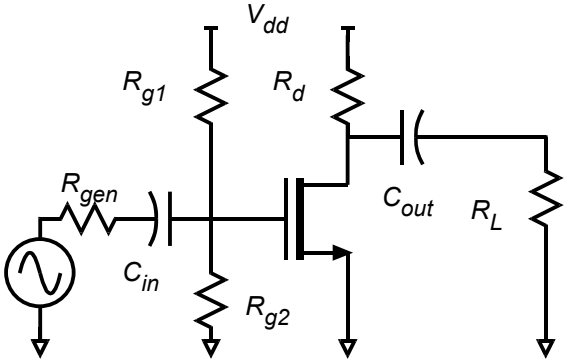


Problem 1: The NMOS FET has $K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$ $K_v = 2.0\text{mA/V} \cdot (W_g / 1\mu\text{m})$ $\Delta V = 0.1\text{V}$, $1/\lambda$ =4 Volts, and a 0.25 V threshold.. The gate-source capacitance C_{gs} is $(20\text{fF}/(\mu\text{m})^2) \cdot L_g W_g + (0.5\text{fF}/\mu\text{m}) \cdot W_g$ while C_{gd} is $(0.5\text{fF}/\mu\text{m}) \cdot W_g$.

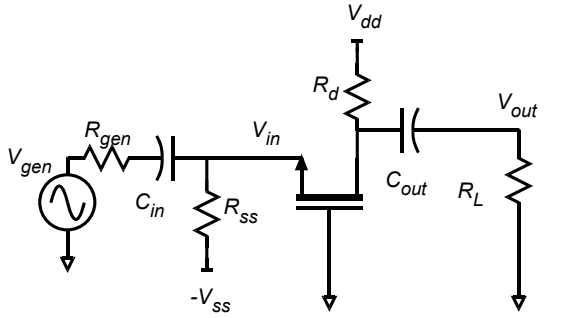
V_{dd} is 1.5 Volts. We will bias device at V_{gs}=0.40 Volts and I_d = 1mA and V_{ds}=0.5 V. From this you can find W_g.

R_{gen}=100 kΩ . The parallel combination of R_{g1} and R_{g2} is 1 MΩ . C_{in} and C_{out} are both infinite. The load resistance is to be twice R_d

(a) Find all resistor values, the values of C_{gs} and C_{gd}. Also find the transistor f_τ (b) Using the results derived by nodal analyis, find the low-frequency gain and the 2 dominant poles of the transfer function and the zero frequency. Is it so high in frequency that it can be neglected? (c)Now suppose that the input signal is a 10 mV step-function occuring at t=0. What will be the output signal voltage waveform (compute it as a function of time)? What is the amplifer's 10%-90% step-response risetime ? (to compute this, if one pole is much higher in frequency that the other, neglect it in the risetime calculation) (d) Draw a Bode plot (on semi-log paper) of the gain-frequency characteristics.



Problem 2: Using the same values as in problem 1, now set C_{gs} and C_{gd} to zero, and C_{in}=1nF, C_{out}=2nF. (a) compute calculate the low-frequency gain-frequency characteristics of the amplifier. (b) Now suppose that the input signal is a 1 mV step-function occuring at t=0. What will be the output signal voltage waveform (compute and graph as a function of time)?



: The NMOS FET has $K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$ $K_v = 2.0\text{mA/V} \cdot (W_g / 1\mu\text{m})$ $\Delta V = 0.1\text{V}$,

Problem 3:
V_{dd} = 1 Volts, $-V_{ss}$ = 1 Volts,
Bias the transistor at V_d= 0.25V, V_{gs}= 0.3V, and select the gate width W_g such that the transistor is carrying 1mA drain current. . The load resistance is to be 10 times Rd. Rgen=100 Ohm.
(a) Find all resistor values, Cgs and Cgd, and transistor ft.
(b) Compute the small signal Vout/Vgen at mid-band. (c) Using the results derived by

$1/\lambda$ =infinity Volts, and a 0.25 V threshold.The gate-source capacitance C_{gs} is $(20\text{fF}/(\mu\text{m})^2)\cdot L_g W_g + (0.5\text{fF}/\mu\text{m})\cdot W_g$ while C_{gd} is $(0.5\text{fF}/\mu\text{m})\cdot W_g$.	nodal analysis, find the first two poles in the transfer function. (d) Draw clean Bode plots on semilog paper of the mangitude and phase of the transfer function.