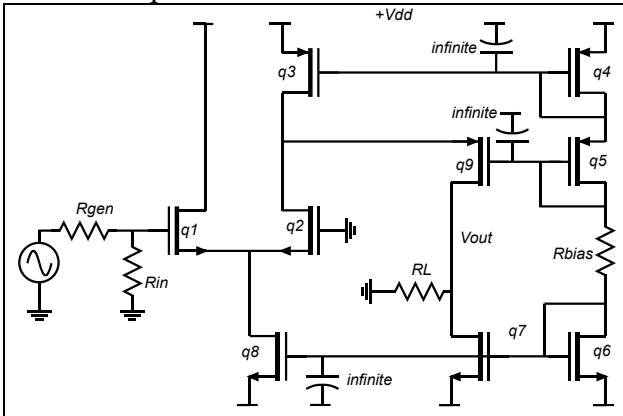
ECE137b problem set 5



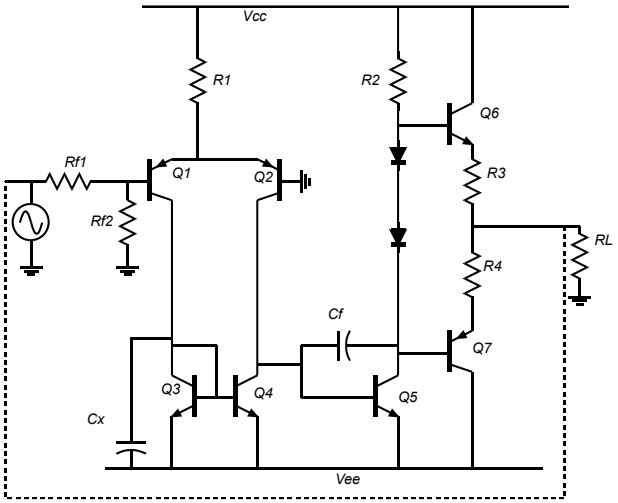
Both the NMOS and PMOS FETs have $K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$ $K_v = 2.0\text{mA/V} \cdot (W_g / 1\mu\text{m})$ $\Delta V = 0.1\text{V}$, $1/\lambda$=4 Volts, and a 0.25 V threshold. L_g=30nm .The gate-source capacitance C_{gs} is $(20\text{fF}/(\mu\text{m})^2) \cdot L_g W_g + (0.5\text{fF}/\mu\text{m}) \cdot W_g$ while C_{gd} is $(0.5\text{fF}/\mu\text{m}) \cdot W_g$.

Problem 1:
We will choose all FET widths such that $|V_{gs}|$=0.35 V.
The supplies are +/- 1.0 volts
Q8,7,6 are to be biased at 100 μA

Find Rbias.
RL=500 kOhm. Rgen=Rin/10=10 kOhm.

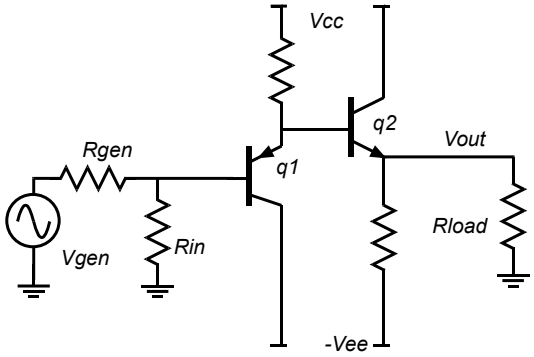
To simplify the problem, the indicated capacitors are AC short circuits (do not treat these as capacitors in an MOTC analysis) (a) Find all DC bias conditions (b) find all device capacitances (c) find the circuit gain and (d) Find the all significant poles in the transfer funtion Vout/Vin

Problem 2
A simple operational amplifier. The power supplies are ±10 volts. Pick R1 so that Q1 and Q2 are biased at 0.25 mA. Pick R2 so that Q5 is biased at 1 mA. Pick R3=R4 so that the ouptut transistors are biased at 0.5 mA.



Assume feedback forces Vout to zero volts DC. All transistors have the same emitter saturation current, have τ_f=0.5 ps, C_{je}=5 fF, C_{cb}=10 fF for the NPN and τ_f=3 ps, C_{je}=20 fF, C_{cb}=50 fF for the PNP. ß=100, V_A=∞. The load resistance is 1 kΩ. C_f is 10 pF. In the circuit connection shown (Rf1=9Kohm and Rf2=1kOhm represent the feedback network), we are calculating the gain around the feedback loop. This is represeented by the dotted line, which you should not treat as a connection. Find the gain Vout/Vgen. Using MOTC, find the 2 dominant poles in the transfer function.

MAJOR COMMENT. There is a difficulty in that the Q1-Q4 stage has 2 paths from input-ouput. To simplify

	this problem, I have added Cx, a Perfect AC short, to kill one of the 2 paths
	Problem 3. Q1 and Q2 have ß=100 and V_A=∞. Cje=100 fF, Ccb=300 fF and the forward transit time is 0.75 pS. Vcc= -Vee=5 Volts. Rload=100 Ohms, Rgen=1000 OHms, Rin=10,000 Ohm. Q2 is to be biased at 50 mA and Q1 is to be biased at 5 mA. a)Find the DC bias conditions and the voltage gain V_{out}/V_{gen}. b)Use the method of time constants to find the 2 dominant pole frequencies of the circuit. d) Draw Bode plots for parts b) and c).