### Problem 1

a) The operational amplifier has infinite input impedance, zero output impedance, infinite common-mode rejection ratio, and a differential gain of $A_{\text{diff}} = 10,000$. $R_1 = 10\,\text{kOhm}$, $R_2 = 1\,\text{kOhm}$.

Find the gain $V_{\text{out}}/V_{\text{in}}$.

b) Now suppose that the op-amp has a differential input impedance of 100 kOhm. Find the closed-loop input impedance.

c) The differential amplifier has an output impedance of 10 Ohm. Find the closed-loop output impedance.

### Problem 2

The operational amplifier shown above has zero output impedance, infinite common-mode rejection ratio, and a differential gain of $A_{\text{diff}} = 10^3$. $R_f = 50\,\text{kOhm}$, $R_1 = 10\,\text{kOhm}$.

The amplifier input impedance, however, is only 100 Ohm. Find the gain $V_{\text{out}}/V_{\text{gen}}$.

### Problem 3

Feedback amplifier stability analysis by the Bode method. The operational amplifier has a differential gain of $10^6$. Its differential gain has three significant poles, one at 10Hz, one at 10MHz, and one at 20 MHz. The amplifier is otherwise ideal. We will consider 2 cases: a) $R_1 = 0$ and $R_2 = 1\,\text{kOhm}$  b) $R_1 = 9\,\text{kOhm}$ and $R_2 = 1\,\text{kOhm}$.

In each of cases a), and b) do the following:

- **Draw Bode plots (Magnitude and phase) of $A_{\text{D}}(f)$ and $\beta(f)$**
- **Find the loop bandwidth and estimate from this the bandwidth of $V_{\text{out}}/V_{\text{gen}}$.**
- **Find the gain margin and the phase margin of the feedback loop. Is the amplifier stable?**
Problem 4
Stability analysis: the Root Locus
The operational amplifier has a differential gain of 1,000,000. Its differential gain has **two** significant poles, one at 10 Hz, and one at 1 MHz. The amplifier is otherwise ideal. $R_{gen}=0$. Consider 2 cases: a) $R_1=0$ and $R_2=1\text{kHz}$ b) $R_1=19\text{kOhm}$ and $R_2=1\text{kOhm}$. In each of cases a), and b) do the following:
Solve mathematically for $V_{out}(s)/V_{gen}(s)$
Find the natural frequency, the damped frequency, and the damping factor
Draw to scale the location of the poles of $V_{out}(s)/V_{gen}(s)$ on the S-plane.
Graph the (amplitude) of $V_{out}(j\omega)/V_{gen}(j\omega)$
Graph the step response of the amplifier $V_{out}(t)$ given $V_{in}(t)=1\text{V}*U(t)$

Problem 5: The transistors are modeled by the small signal model below left, and have 0.8 nm oxide thickness, 22 nm gate length, and a 0.25 V threshold. Mobility is 200 cm$^2/(\text{V-s})$, saturation drift velocity is 1E7 cm/s, and $1/\lambda_{infty}=\text{infinity}$. The gate capacitance $C_{gs}$ is $\varepsilon_r \varepsilon_{ox} L_g W_g / \varepsilon_{ox} + (0.5\text{fF}/\mu\text{m}) \cdot W_g$
while $C_{gd}$ is $(0.5\text{fF}/\mu\text{m}) \cdot W_g$
$\lambda_{infty}=0$.

The supplies are +/- 1 volts..
$Q1,2,4,5,6,7,9$ are to be biased at 0.1 mA and at $V_{gs}=0.3$ Volts. You will need to find the gate width of all FETs. $R_2=100 \text{kOhm}$, $R_1=1 \text{MOhm}$. (a) Find all DC bias conditions
(b) At low frequencies, find the loop gain $T$, $A_{infty}$, and the closed loop gain $A_{cl}=V_{out}/V_{gen}$. (c) Using your preferred method of analysis, find the location of all significant poles in the loop transmission. (d) Draw a Bode plot of the magnitude of $T(j\omega)$. Find the phase margin of the feedback loop.