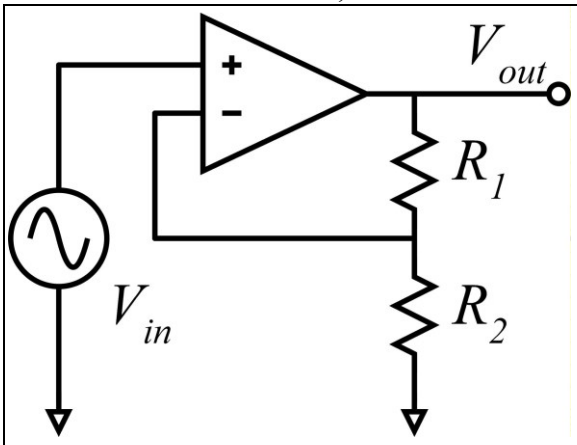
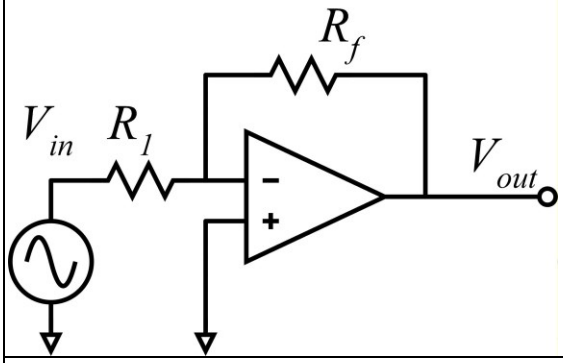
ECE137B Problem set #6,



Problem 1

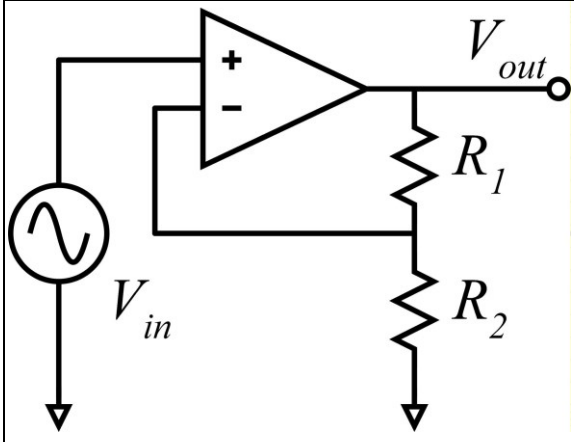
a) The operational amplifier has infinite input impedance, zero output impedance, infinite common-mode rejection ratio, and a differential gain of A_{diff}=10,000. R_1=5kOhm, R_2=1kOhm. Find the gain V_{out}/V_{in}. (b) Now suppose that the op-amp has a differential input impedance of 100 kOhm. Find the closed-loop input impedance

c) the differential amplifier has an output impedance of 10 Ohm. Find the closed-loop output impedance.



Problem 2

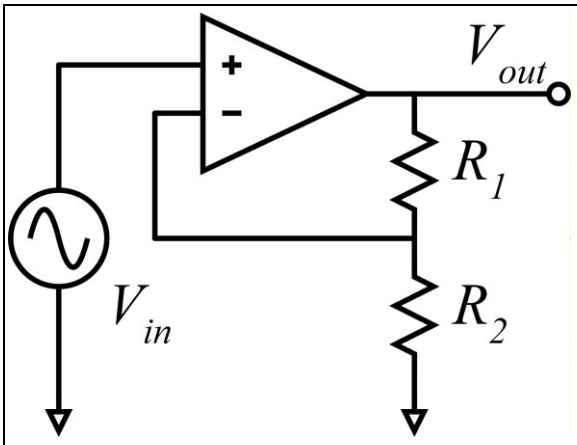
The operational amplifier shown above has zero output impedance, infinite common-mode rejection ratio, and a differential gain of A_{diff}=10^3. R_f =30kOhm, R_1=10 kOhm. The amplifier input impedance, however, is only 100 Ohm. Find the gain V_{out}/V_{gen}.



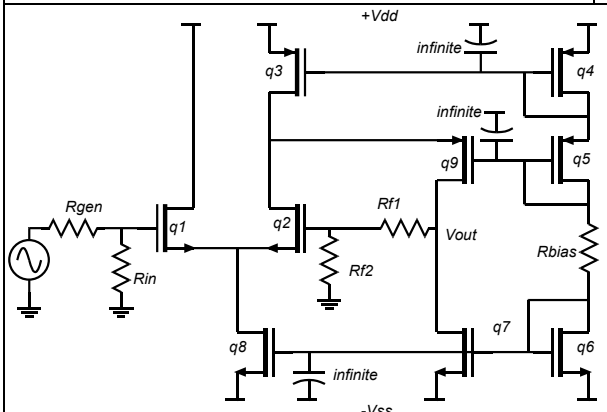
Problem 3. Feedback amplifier stability analysis by the Bode method. The operational amplifier has a differential gain of 10^6. Its differential gain has three significant poles, one at 5Hz, one at 10MHz, and one at 20 MHz. The amplifier is otherwise ideal.. We will consider 2 cases: a) R1=0 and R2=1kOhm b) R1=9kOhm and R2=1kOhm.

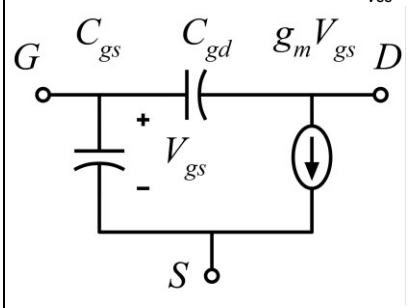
In each of cases a), and b) do the following:

- Draw Bode plots (Magnitude and phase) of Ad(f) and ß(f)
- Find the loop bandwidth and estimate from this the bandwidth of Vout/Vgen.
- Find the gain margin and the phase margin of the feedback loop. Is the amplifier stable ?



Problem 4
Stability analysis: the Root Locus
The operational amplifier has a differential gain of 1,000,000. Its differential gain has **two** significant poles, one at 10 Hz, and one at 1 MHz The amplifier is otherwise ideal. Rgen=0. Consider 2 cases: a) R1=0 and R2=1kOhm b) R1=19kOhm and R2=1kOhm. In each of cases a), and b) do the following:
Solve mathematically for Vout(s)/Vgen(s)
Find the natural frequency, the damped frequency, and the damping factor
Draw to scale the location of the poles of Vout(s)/Vgen(s) on the S-plane.
Graph the (amplitude) of Vout(jf)/Vgen(jf)
Graph the step response of the amplifier Vout(t) given Vin(t)=1V*U(t)





Problem 5 : The transistors are modeled by the small signal model below left, and have 0.8 nm oxide thickness, 22 nm gate length, and a 0.25 V threshold. Mobility is 200 cm^2/(V-s), saturation drift velocity is 1E7 cm/s, and 1/lambda=infinity. The gate capacitance C_{gs} is $\varepsilon_r \varepsilon_{ox} L_g W_g / T_{ox} + (0.5\text{fF}/\mu\text{m}) \cdot W_g$ while C_{gd} is $(0.5\text{fF}/\mu\text{m}) \cdot W_g$
Lambda=0.

The supplies are +/- 1 volts..
Q1,2,4,5,6,7,9 are to be biased at 0.1 mA and at V_{gs}=0.3 Volts. You will need to find the gate width of all FETs. Rf2=100 kOhm, Rf1=1 MOhm. (a) Find all DC bias conditions
(b) At low frequencies, find the loop gain T , A_infinity, and the closed loop gain Acl=Vout/Vgen. (c)Using your preferred method of analysis, find the location of all significant poles in the loop transmission. c) Draw a Bode plot of the magnitude of T(jomega). Find the phase margin of the feedback loop.