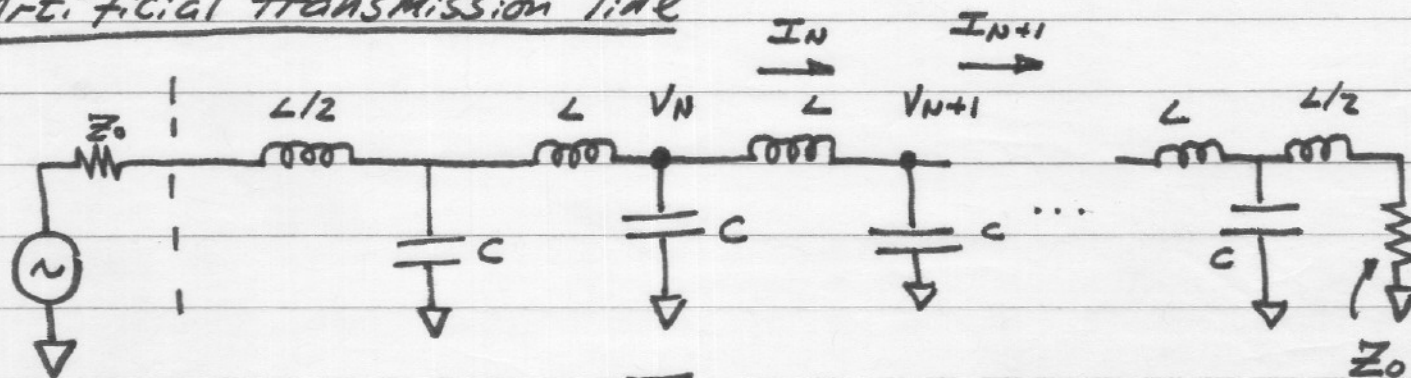


The traveling-wave amplifier

Artificial transmission line



Design: $Z_0 = \sqrt{\frac{L}{C}}$ by choice.

To analyze: $V_{N+1} = e^{-\Gamma} V_N = e^{-A} e^{-jB} V_N$

$$\left. \begin{aligned} V_N (e^{-\Gamma} - 1) &= -j\omega L I_N \\ I_N (e^{-\Gamma} - 1) &= -j\omega C V_{N+1} \end{aligned} \right\} \text{solve for } e^{\Gamma}$$

$$\Rightarrow \cosh \Gamma = 1 - \frac{\omega^2 LC}{2}$$

define a cutoff (or Bragg) Frequency

$$\omega_c = \frac{2}{\sqrt{LC}}$$

Then $\cosh \Gamma = 1 - 2\omega^2 / \omega_c^2$

but $\cosh \Gamma = \cosh(A + jB)$
 $= \cosh(A) \cos(B)$
 $+ j \sinh(A) \sin(B)$

so

$$\left(\cosh(A) \cos(B) + j \sinh(A) \sin(B) = 1 - 2\omega^2 / \omega_c^2 \right)$$

examine how this behaves:

Case 1: $\omega < \omega_c$: then complex term = 0 &
 real term = $1 - 2\omega^2 / \omega_c^2$

$$\Rightarrow A = 0 \text{ and}$$

$$\cos B = 1 - 2\omega^2 / \omega_c^2$$

so wave propagates without attenuation.

Case 2 $\omega > \omega_c$: then we can no longer have

$$\cos B = 1 - 2\omega^2 / \omega_c^2 \leftarrow \text{less than } -1$$

hence $A \neq 0 \Rightarrow$ this means wave attenuates.

(note also $A \neq 0 \Rightarrow \sin B = 0 \Rightarrow B = \pi$)

So: signals propagate only below the Bragg
 frequency $\omega_c = 2 / \sqrt{LC}$

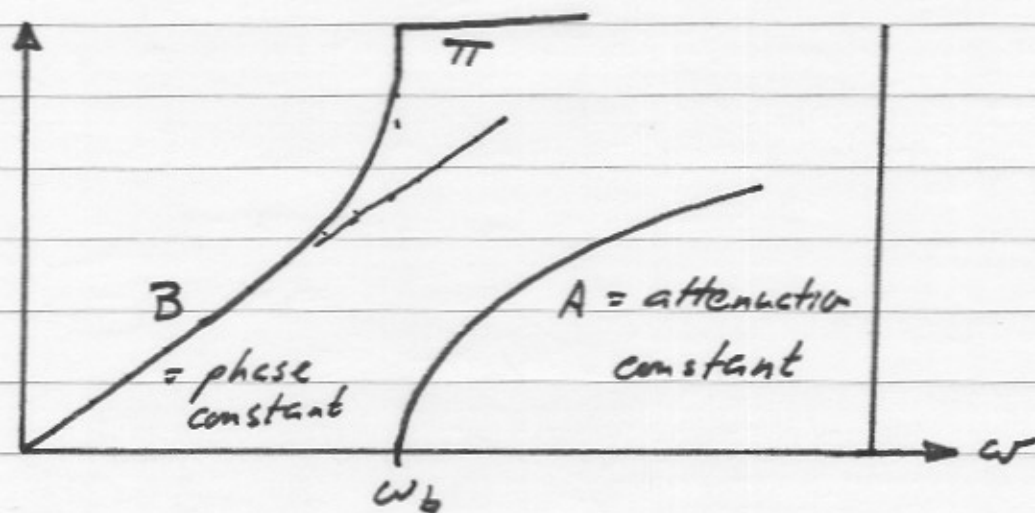
Below cutoff: $A=0$ $\cos B = 1 - 2\omega^2/\omega_c^2$
 $= 1 - \omega^2 LC/2$

Far below cutoff $B \ll 1$, $\cos B \approx 1 - B^2/2 + (\overset{\uparrow}{B^4/24})$
 drop.

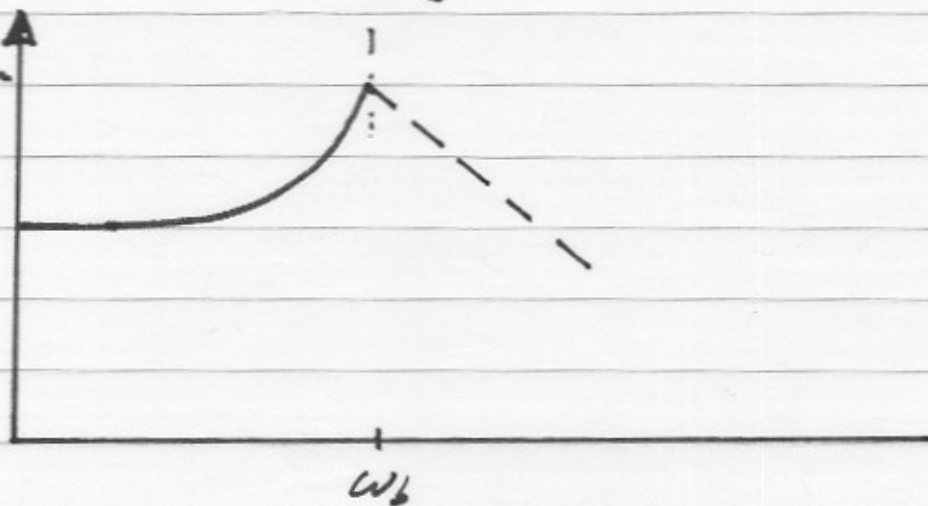
so: $1 - B^2/2 \approx 1 - \omega^2 LC/2$

$\Rightarrow B \approx \omega \sqrt{LC}$

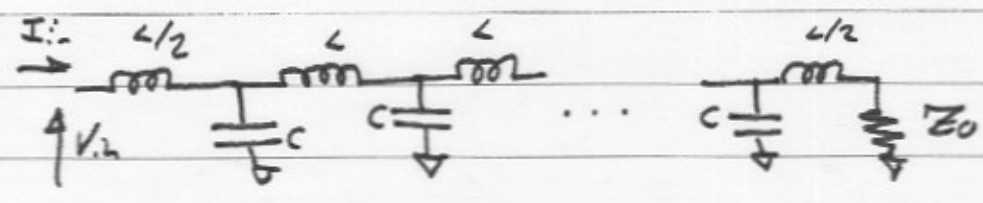
phase delay = $\frac{B}{\omega} \approx \sqrt{LC}$



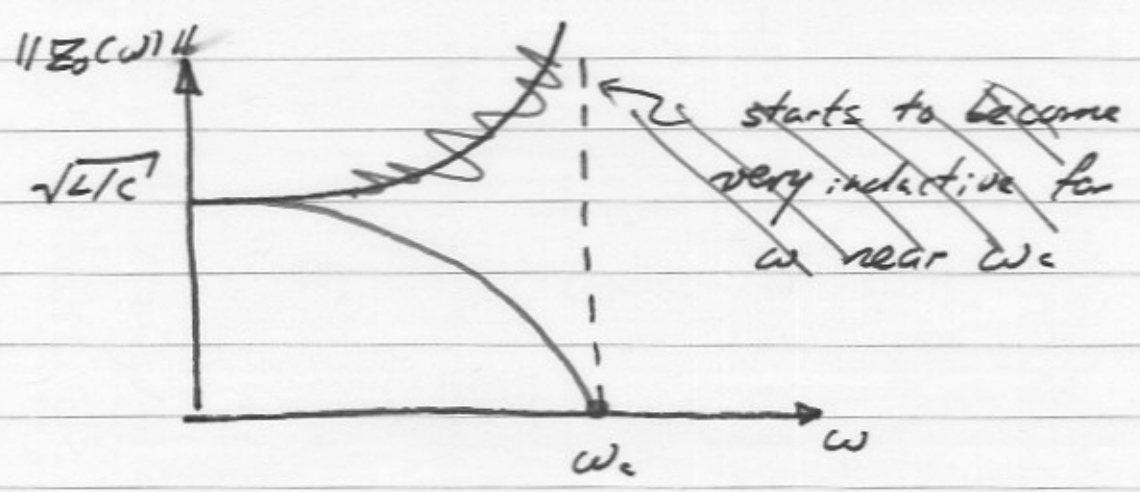
Phase Delay
per section



Characteristic Impedance



Defining $Z_0(\omega) = V_{in}(\omega) / I_{in}(\omega)$ a similar calculation can be made. (won't repeat)



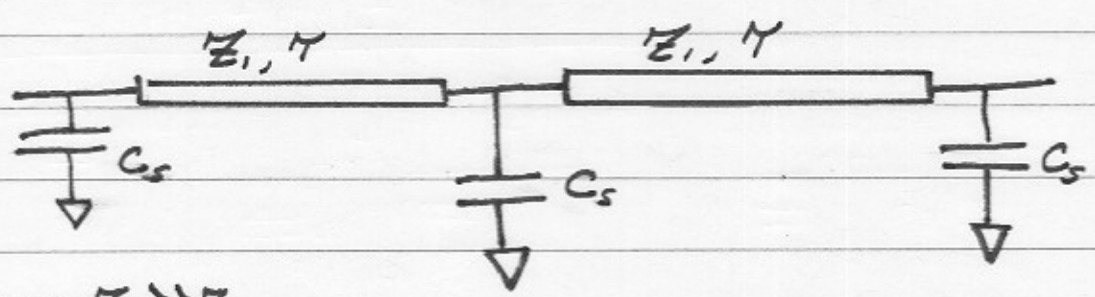
summary of general properties:

$Z_0 \approx \sqrt{LC}$ for $\omega \ll \omega_c$

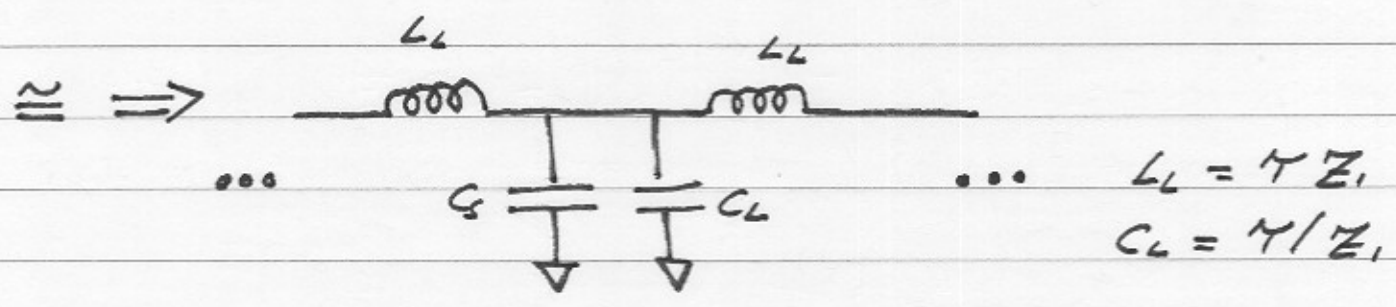
delay per section $\approx \sqrt{LC}$ for $\omega \ll \omega_c$

$\omega_c = \frac{2}{\sqrt{LC}}$ or $f_c = \frac{1}{\pi\sqrt{LC}}$

Realization with distributed elements:



assume $Z_1 \gg Z_0$



$$\Rightarrow Z_0 \approx \sqrt{\frac{L_L}{C_s + C_L}} = \sqrt{\frac{\gamma Z_1}{C_s + \gamma / Z_1}} \quad \leftarrow \omega \ll \omega_c$$

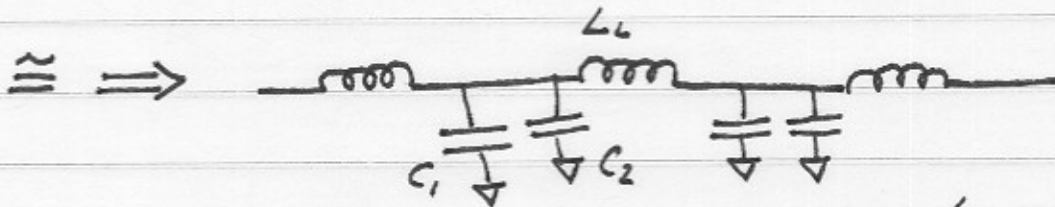
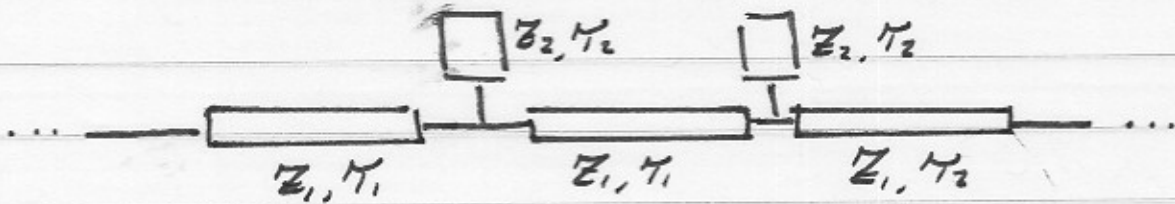
$$T = \text{delay per section} \approx \sqrt{L_L (C_s + C_L)} = \sqrt{\gamma Z_1 \left(C_s + \frac{\gamma}{Z_1} \right)}$$

$$\omega_c \approx \frac{2}{\sqrt{L_L (C_s + C_L)}} = \frac{2}{\sqrt{\gamma Z_1 \left(C_s + \frac{\gamma}{Z_1} \right)}}$$

Can also realize as so:

$$Z_2 \ll Z_0$$

$$Z_1 \gg Z_0$$



$$L_L = \gamma_1 Z_1$$

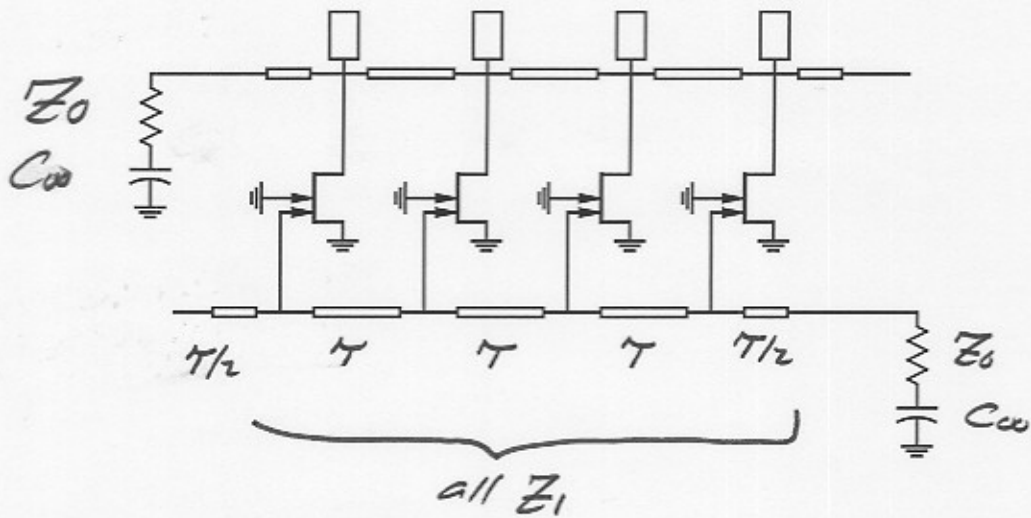
$$C_1 = \gamma_1 / Z_1$$

$$C_2 = \gamma_2 / Z_2$$

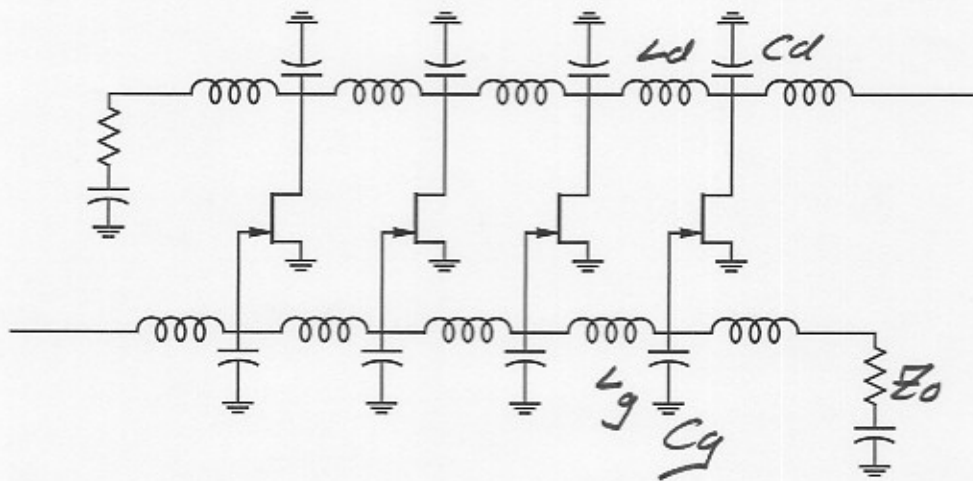
Touchstone will provide exact analysis to

check these design (first-order) relationships.

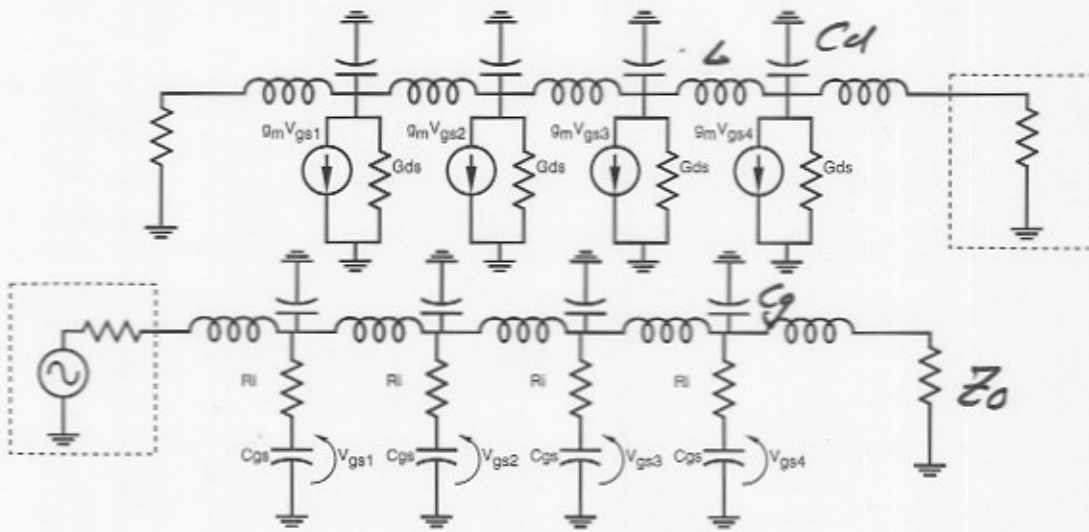
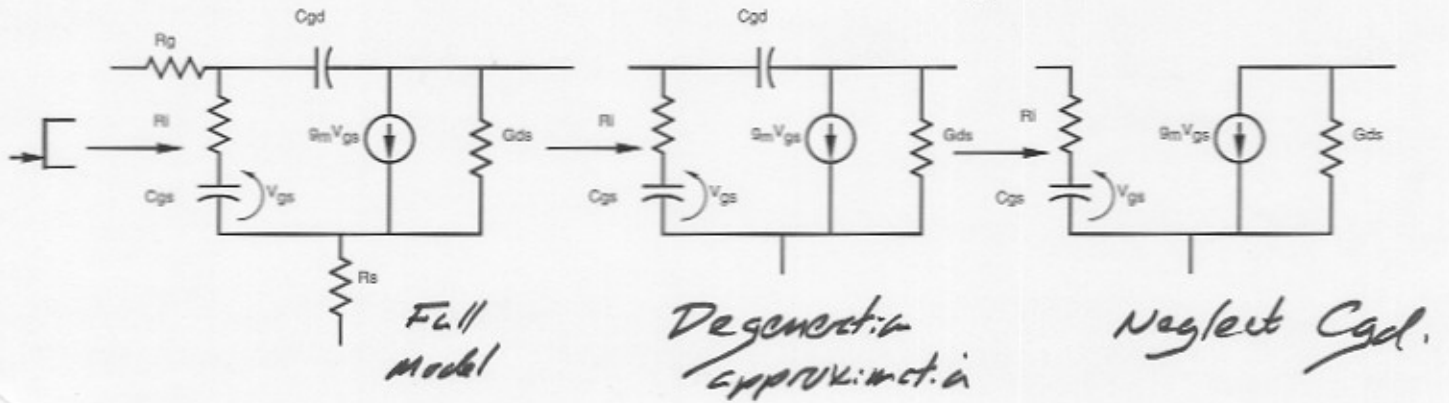
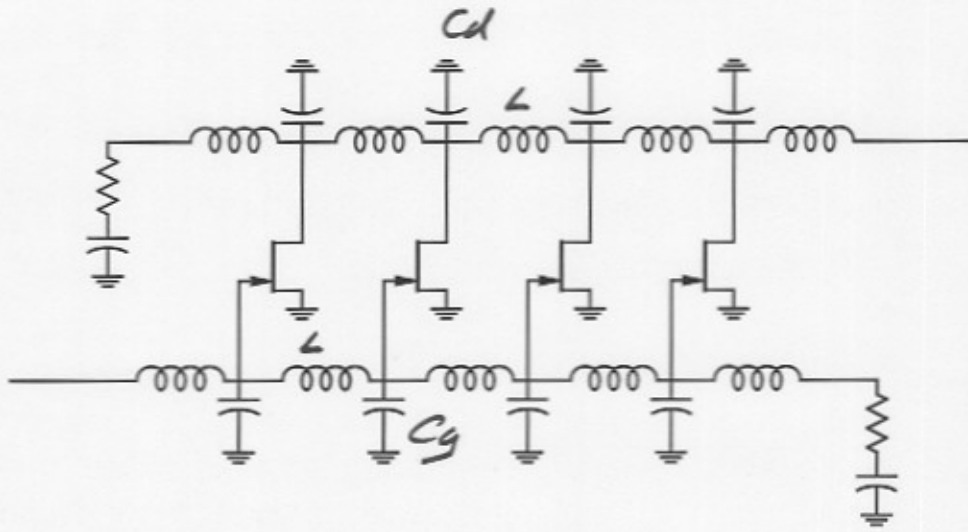
Traveling wave Amplifier



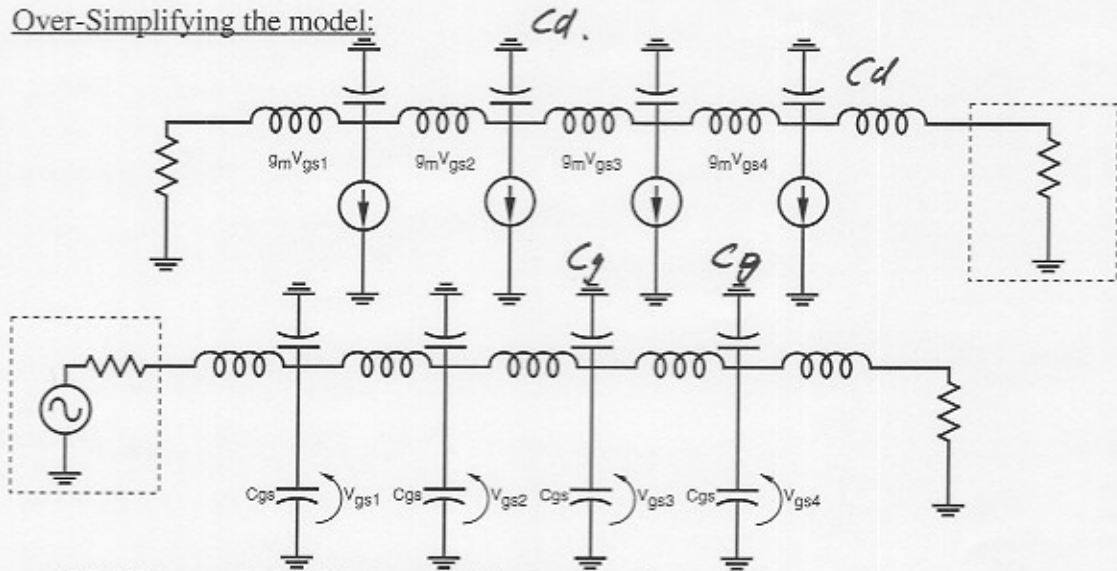
Approximate model



→ is a shorthand for a cascode pair
 cascodes or cs devices can be used..

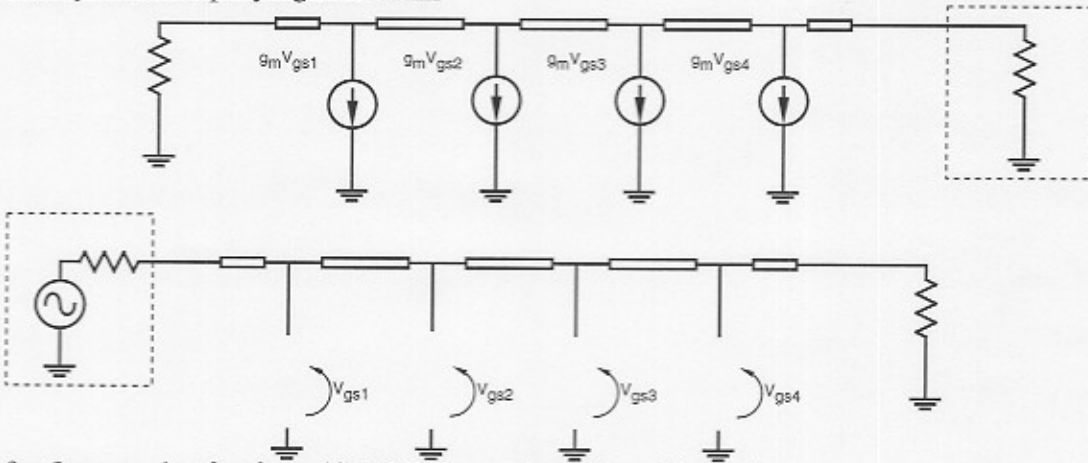


Over-Simplifying the model:



---artificial transmission lines coupled by transconductances

Really-over simplifying the model



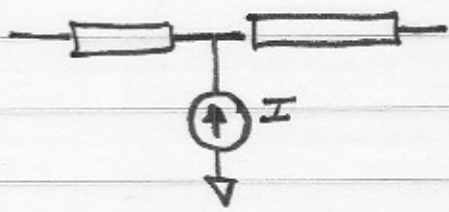
for frequencies $f \ll f_c$, artificial lines can be replaced by real ones,...

$$T_d = \sqrt{L_d C_d} \quad Z_d = \sqrt{L_d / C_d} \quad T_g = \sqrt{L_g (C_g + C_{gs})} \quad Z_g = \sqrt{L_g / (C_g + C_{gs})}$$

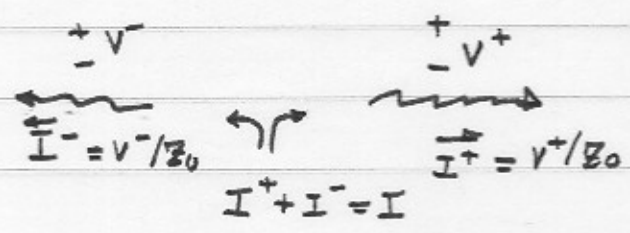
Clearly we want $Z_d = Z_g = 50\Omega$; we also want $T_d = T_g$.
 Above model shows that bandwidth $\approx 1/\pi \sqrt{L_g (C_g + C_{gs})}$ if $T_g = T_d$

Gain

Assuming equal delays:



From symmetry, individual current generator develops equal waves in both directions.



Hence $I^+ = I/2$
 and $V^+ = Z_0 I/2$

each successive device (FET) adds a current $I/2$ to the forward wave.

If they add in phase (I_f !!!)

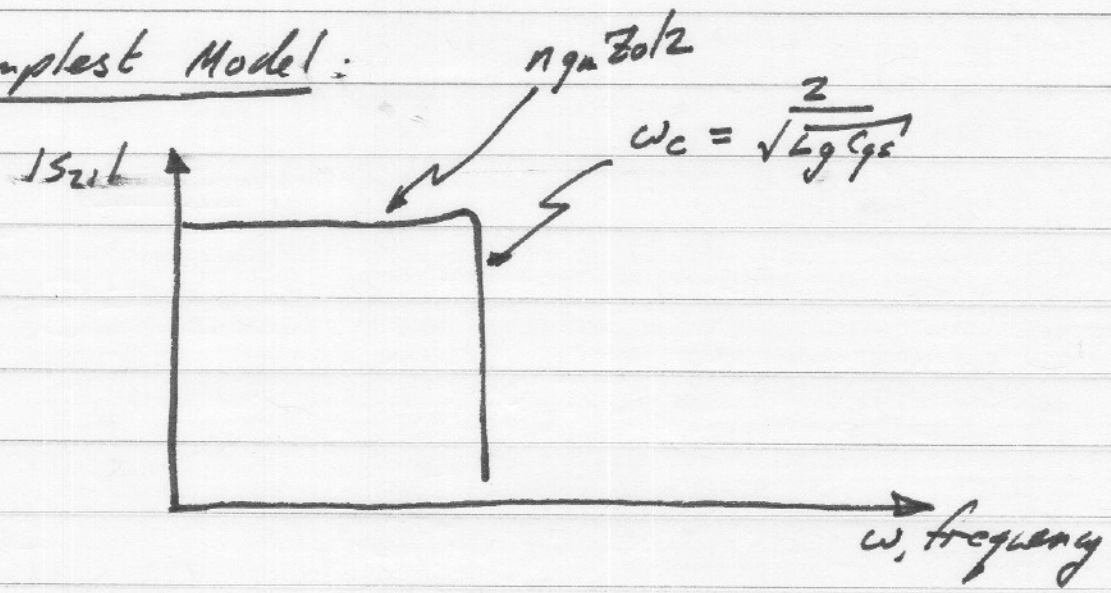
then total voltage after n devices

$$V^+ = n Z_0 I/2 = -n \frac{Z_0 g_m V_{gs}}{2} = -\frac{n Z_0 g_m V_{in}}{2}$$

$$\text{Forward gain} = -n g_m Z_0 / 2$$

Approaching the Bragg Frequency, the line will no longer transmit signals.

So simplest Model:



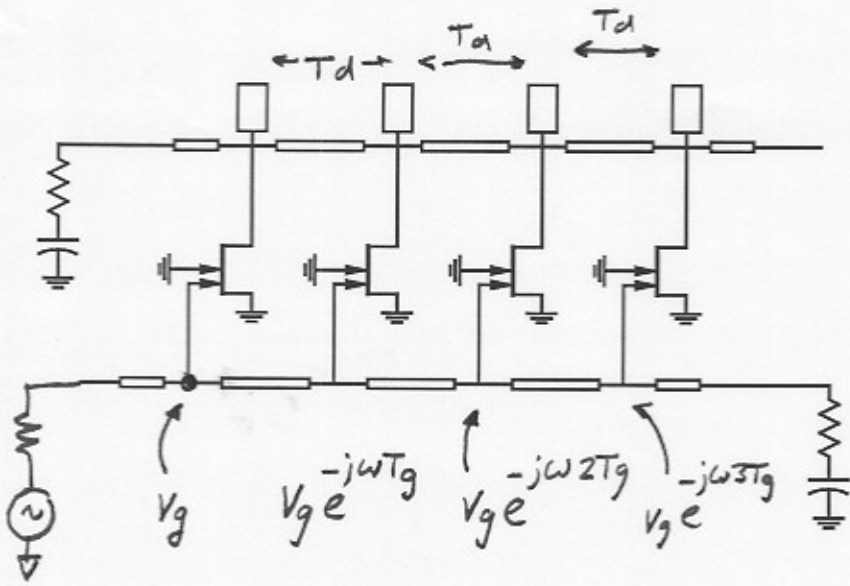
i.e. the periodic lines limit the amplifier bandwidth. This is far from the only effect.

Also:

- Effect of Mismatched delays on gate and drain lines.
- Effect of input & output resistance.

on the issue of delays:

T_d = inter-device delay on drain line
 T_g = " " " " gate "



Neglect the delays of the first gate-line section and the last drain-line section, as these are common to all signals:

FET #1

$$\begin{cases} \text{gate 1} & V_g e^{-j\omega T_g} \\ \text{drain 1} & g_m V_g e^{-j\omega T_g} \\ \text{after reaching output:} & -\frac{Z_0 g_m V_g}{2} e^{-j\omega T_g} e^{-j\omega 3T_d} \end{cases}$$

FET #2

$$\begin{cases} \text{gate 1} & V_g e^{-j\omega T_g} \\ \text{drain 1} & g_m V_g e^{-j\omega T_g} \\ \text{after reaching output:} & -\frac{Z_0 g_m V_g}{2} e^{-j\omega T_g} e^{-j\omega 2T_d} \end{cases}$$

etc.

Total output (4 Fets)

$V_{out} =$

$$-V_g \cdot \frac{Z_0 g_m}{2} \left[\begin{array}{l} e^{-j\omega T_g} e^{-j3\omega T_d} + e^{-j\omega T_g} e^{-j\omega 2T_d} \\ + e^{-j2\omega T_g} e^{-j\omega T_d} + e^{-j3\omega T_g} e^{-j\omega T_d} \end{array} \right]$$

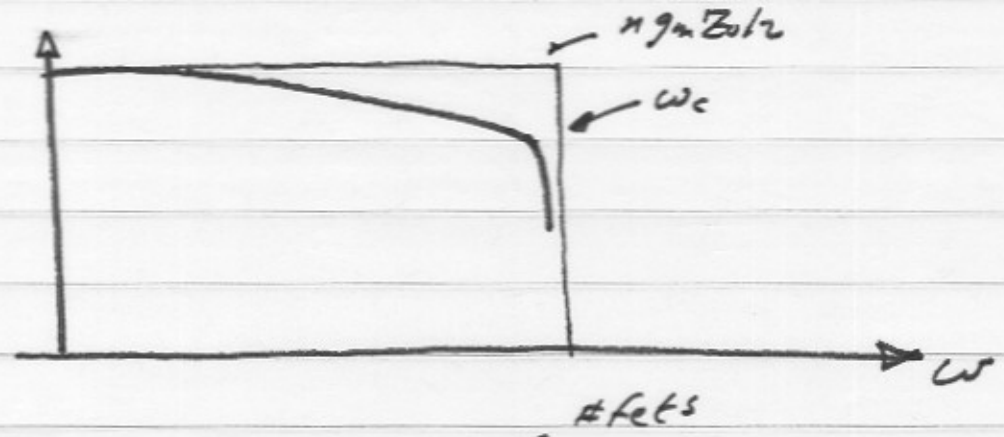
phase factors (or delays) must all be equal for outputs to add in-phase.

Suppose T_g & T_d are mismatched by $\Delta T = T_d - T_g$

$$V_{out} = -V_g \frac{Z_o g_m}{2} e^{-3j\omega T_g} \times \left[e^{-j3\omega\Delta T} + e^{-j2\omega\Delta T} + e^{-j\omega\Delta T} + 1 \right]$$

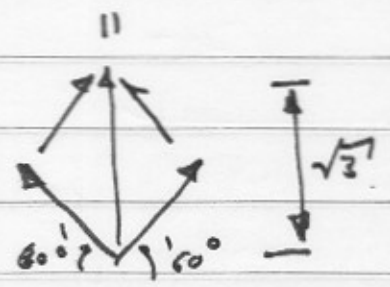
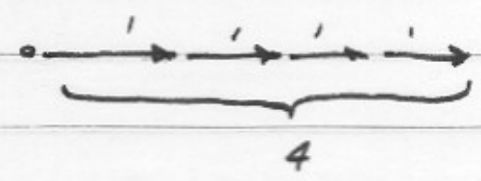
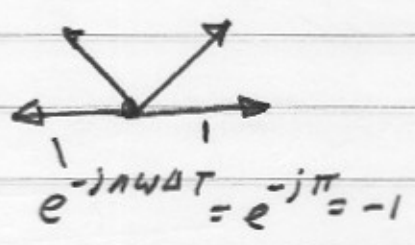
delay T_{read} , so who cares?

This will result in a rolloff in the frequency response:



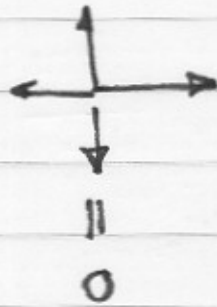
consider when $(n-1)\omega\Delta T = \pi$

vs. dc.

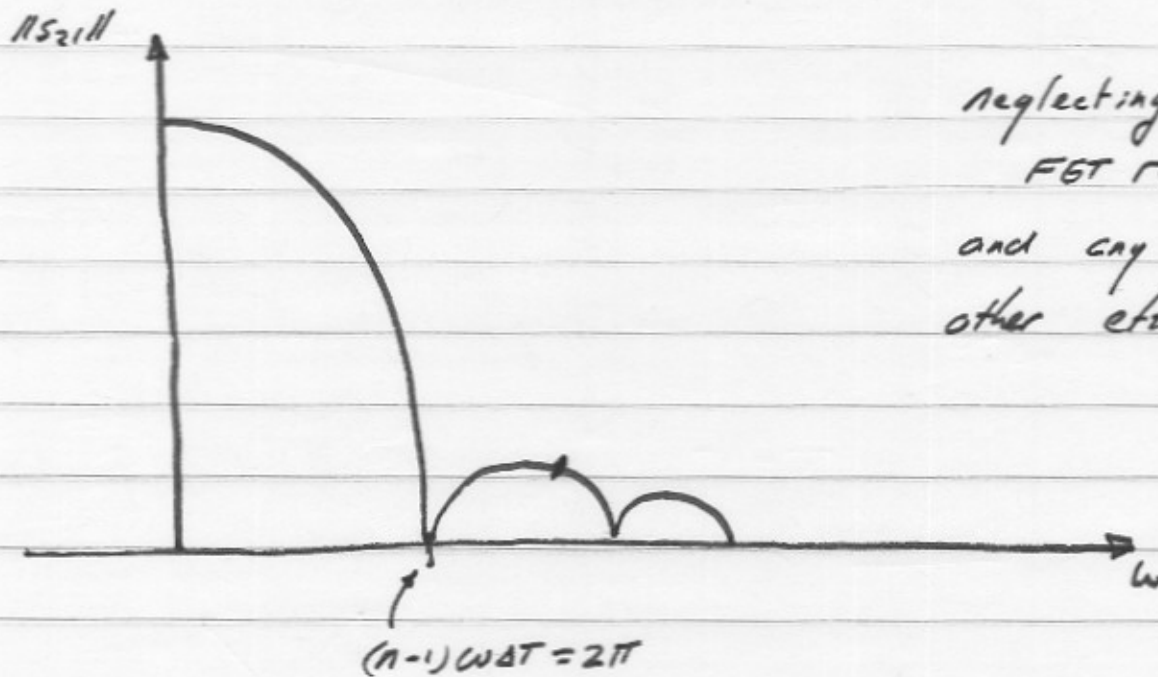


\Rightarrow response down by $\frac{\sqrt{3}}{4} = -7 \text{ dB.}$

also consider when $(n-1)\omega\Delta T = 2\pi$



Null in response.



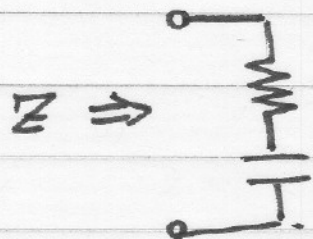
neglecting ω_c ,
FET resistances,
and any and all
other effects.

Design relationship: $(n-1)\omega_c\Delta T \leq \pi/2$

If we desire negligible rolloff in gain due to delay mis-match.

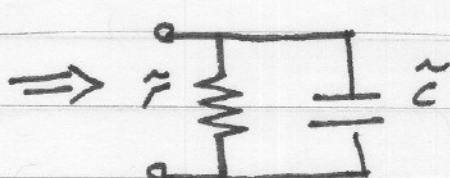
These concepts should be very familiar to physicists; basically the same phenomena as phase matching (or interaction length).

With gate and drain conductance (resistance)
(see illustrations, page 17)

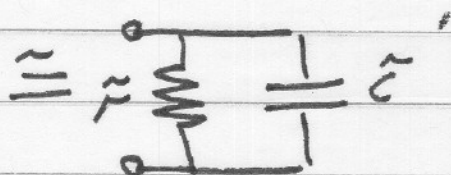


$$Z = r + 1/sC$$

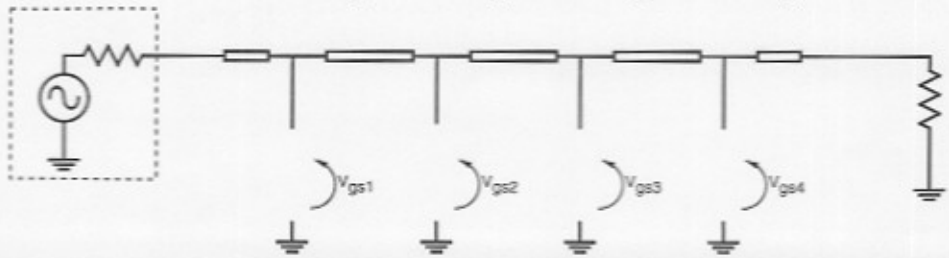
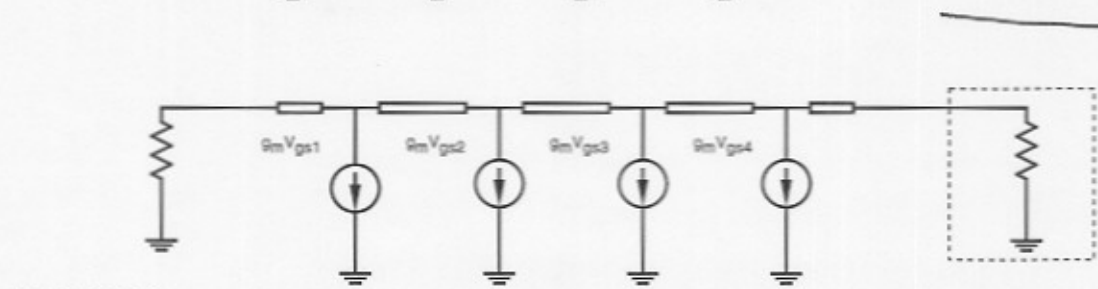
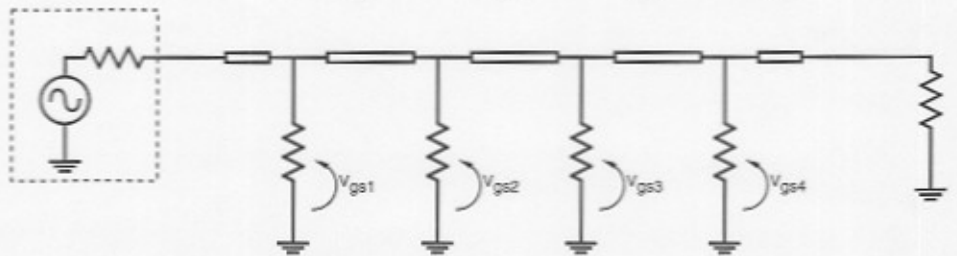
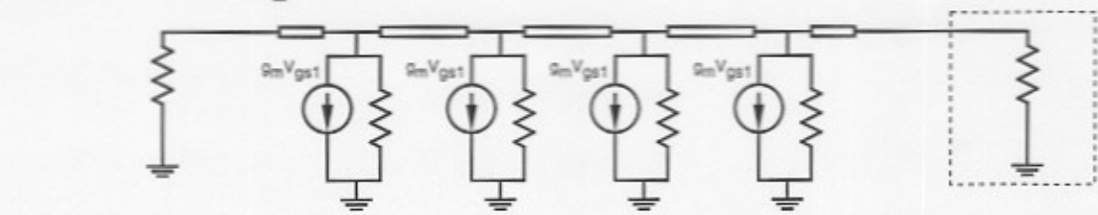
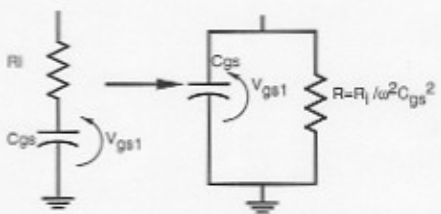
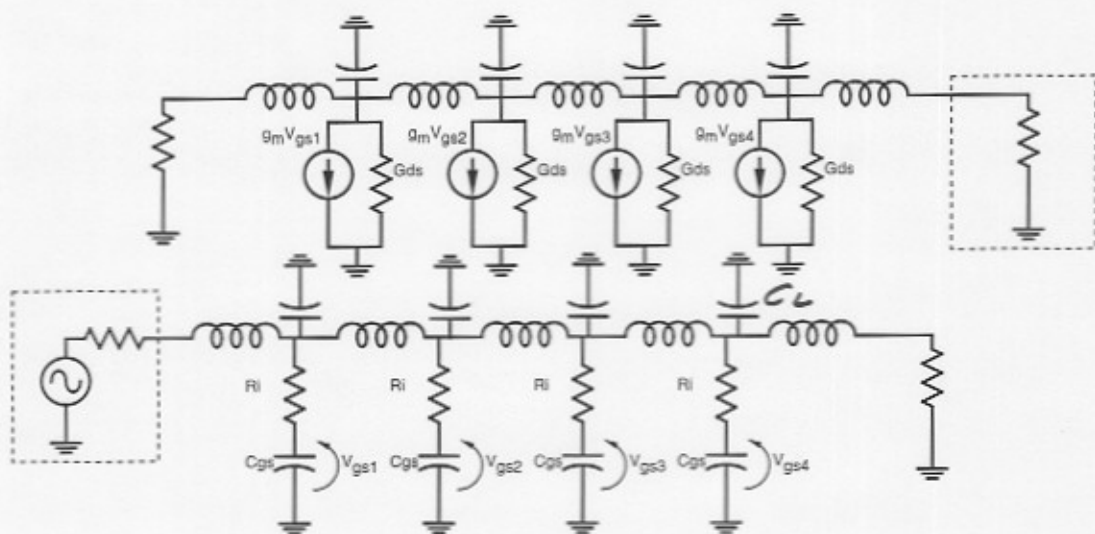
$$\begin{aligned}
 Y = \frac{1}{Z} &= \frac{1}{r + 1/sC} = \frac{sC}{1 + r s C} = \frac{j\omega C}{1 + j\omega r C} \\
 &= \frac{j\omega C (1 - j\omega r C)}{(1 + \omega^2 r^2 C^2)} = \frac{j\omega C}{1 + \omega^2 r^2 C^2} + \frac{\omega^2 C^2 r}{1 + \omega^2 r^2 C^2} \\
 &= jb + g
 \end{aligned}$$



$$\begin{aligned}
 \tilde{r} &= \frac{1}{\omega^2 C^2 r} (1 + \omega^2 C^2 r^2) \\
 \tilde{c} &= C / (1 + \omega^2 C^2 r^2)
 \end{aligned}$$



$$\left. \begin{aligned}
 \tilde{r} &\approx \frac{1}{\omega^2 C^2 r} \\
 \tilde{c} &\approx C
 \end{aligned} \right\} \begin{array}{l} \text{for} \\ \omega \ll 1/rC \\ \text{(good approx)} \end{array}$$



gate and drain lines with attenuation.

Hence we can model both the drain and gate ~~at~~ resistances as resistive parallel loads to ground on the gate and drain lines.

Attenuation per section on gate line:

$$A_g \cong \frac{Z_0}{2r} \quad \text{for } r \gg Z_0$$

$$= \omega^2 C_{gp}^2 r_i Z_g / 2$$

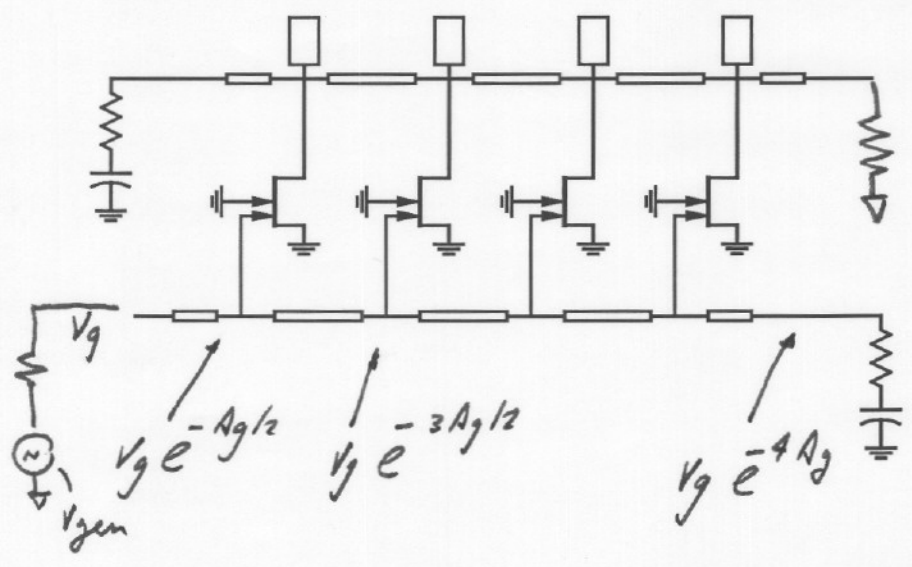
Attenuation per section on drain line

$$A_d \cong \frac{Z_0}{2r_{ds}} = Z_d G_{ds} / 2 \quad \text{for } G_{ds} \ll 1/Z_0$$

Gate line attenuation generally dominates, particularly when dual-gate FETs are used (very low G_{ds})

(Refer to drawing:)

Note that A_d is frequency-independent (gain limit) while $A_g \propto \omega^2$ (bandwidth limit)



Again, lets analyze, neglecting all other effects:

Fet #1

$$\begin{aligned} \text{gate 1: } & V_g e^{-A_g/2} \leftarrow \text{1/2 line section} \\ \text{drain 1: } & g_m V_g e^{-A_g/2} \\ \text{after reaching output:} & \\ & -g_m \frac{Z_0}{2} V_g e^{-A_g/2} e^{-A_d(3/2)} \end{aligned}$$

Fet #2

$$\begin{aligned} \text{gate 2} & V_g e^{-A_g(1/2)} \\ \text{drain 2} & g_m V_g e^{-A_g/2} \\ \text{after reaching output:} & \\ & -g_m \frac{Z_0}{2} V_g e^{-A_g/2} e^{-A_d(2/2)} \end{aligned}$$

etc

Total Output (4 fets)

$$V_{out} = -(V_g Z_0 g_m/2) \times e^{-A_g/2} e^{-A_d/2} \times$$

$$\left[e^{-3A_d} + e^{-A_d} + e^{-2A_d} + e^{-2A_d} + e^{-A_d} + e^{-3A_d} \right]$$

$$A_g = \omega^2 C_{gs}^2 r_i Z_g/2 \quad A_d = Z_d G_d/2$$

Look at Nyasi Paper for graphs: you will see that gain does not increase linearly with # of FETS.

Typically, 3-5 devices is optimal (depends on ratio of f_{max}/f_T)

It is hard to take this much further without getting lost in the math (and there are some very ugly papers on TWA's in the literature)

General observations:

Total Drain-Line attenuation = $\exp(n Z_d G_{ds} / 2)$


Total Gate-line attenuation = $\exp(-n \omega^2 C_{gs}^2 r_i Z_g / 2)$

clearly do not want to have more than ≈ 3 dB ($\approx \exp(-1/2)$) loss on either line

limits: * $n Z_d G_{ds} \leq 1$

i.e. $r_{ds1} || r_{ds2} || \dots || r_{dsn} \geq Z_d$

* $n \omega^2 C_{gs}^2 r_i Z_g \leq 1$

 this sets another frequency limit.

To summarize:

- Analyze input & output structures as synthetic lines, determine $Z_g, Z_d, T_g, T_d, \omega_c$
- D.C. Gain is $-g_m \pi Z_o / 2$
- Bandwidth limits are ω_c , delay mismatch on the 2 lines, and gate-line attenuation $\propto \omega^2$
- Design requirements of $Z_g = Z_d = Z_o$ and $T_g = T_d$ force $L_g = L_d$ and $C_d = C_{gs}$
- As $C_{gs} \gg C_{out}$ for Fets, drain line must have the added capacitors to equalize delays

within the bandwidth, we have:

$$\omega < \omega_c$$

$$n \omega^2 C_{gs}^2 r_i Z_g \leq 1$$

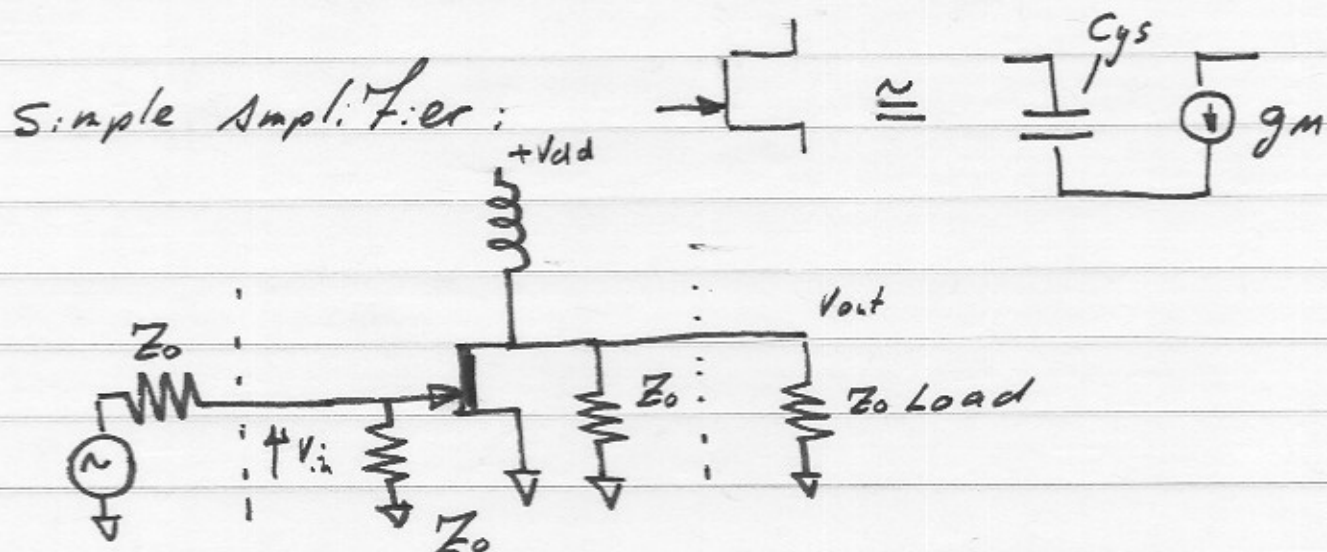
$$(n-1) \omega \Delta T \leq \pi / 2$$

$$A_o \approx -n g_m Z_o / 2$$

$$\text{also } n Z_d G_{ds} \leq 1$$

Ok, so why did we do all of this?

Answer: Increased gain-bandwidth product without the use of matching (resonant) networks



$$A_0 = \text{DC gain} = g_m Z_{0L/2}$$

$$\omega_m = \text{bandwidth} = \frac{1}{C_{gs} Z_{0L/2}}$$

$$\text{gain-bandwidth product} = A_0 \frac{\omega_m}{2\pi} = \frac{g_m}{C_{gs} 2\pi} = f_T !$$

As we scale transistor size (equivalently; put several transistors in parallel) gain will scale in proportion, and bandwidth in inverse proportion, and the product is always f_T . (neglecting C_{gd}, τ_g, \dots)

The TWA beats the f_T limit !!!

use same transistor. Note with highly idealized model that gate & drain line attenuations are zero.

Then only limit is ω_c

$$\omega_c = 2\sqrt{L_g C_{gs}} \quad \text{but} \quad Z_g = Z_o = \sqrt{L_g / C_{gs}}$$

so: $\omega_c = 1 / (C_{gs} Z_o / 2)$ same as before

$$A_0 = \text{DC gain} = N g_m Z_o / 2$$

$$\text{Gain-bandwidth product} = A_0 \frac{\omega_c}{2\pi} = \frac{N g_m}{2\pi C_{gs}} = N f_T$$

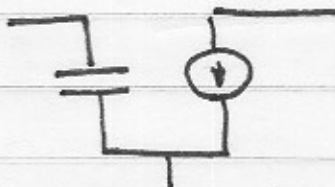
I can beat the f_T limit arbitrarily by using large N .
For More gain, just use more N

For more bandwidth, use smaller devices (C_{gs} & g_m scale proportional to device size) and then increase N as needed to attain desired gain

\Rightarrow infinite gain over infinite bandwidth.

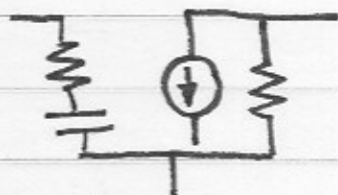
Whoa, this looks wrong. I can never get more than the Maximum available gain of the device at any frequency.

This simple model:



has finite $f_T = g_m / 2\pi C_{gs}$ but infinite f_{max} and infinite maximum available gain (MAG)

use more reasonable device model;



with the addition of r_i and G_{ds} , f_{max} is no longer infinite.

The addition of r_i and G_{ds} introduces gate and drain-line attenuation with resulting limits on Gain and Bandwidth

\Rightarrow with the use of a device of finite f_{max} , only a finite gain-bandwidth product is attainable (not surprising)

Ultimate Gain-Bandwidth Limits

25

Ok, lets examine this:

Remember that the ΔT & ω_c limits on bandwidth are entirely under the control of the circuit designer (use small devices \rightarrow small $C_{gs} \rightarrow$ high ω_c ; get design right to make $\Delta T = 0$)

device-imposed limits:

$$|A_o| \approx n g_m Z_o / 2$$
$$n Z_o G_{ds} \leq 1 \quad n \omega^2 C_{gs}^2 r_i Z_o \leq 1$$

$f_{max} \approx f_T / 2 \sqrt{r_i G_{ds}}$ for the simple model

Hence:

$$\omega_m^2 = (n C_{gs}^2 r_i Z_o)^{-1}$$

$$A_o^2 \omega_m^2 = (n C_{gs}^2 r_i Z_o)^{-1} \cdot n^2 g_m^2 Z_o^2 / 4 = n g_m^2 Z_o / 4 C_{gs}^2 r_i$$

but $n Z_o G_{ds} = 1$

$$A_o^2 \omega_m^2 = g_m^2 / 4 C_{gs}^2 G_{ds} r_i = (2\pi f_{max})^2$$

$$\boxed{A_o \cdot f_m = f_{max} \quad !!!}$$

The reader, however, is cautioned that proving that

$$A_0 f_m = f_{max}$$

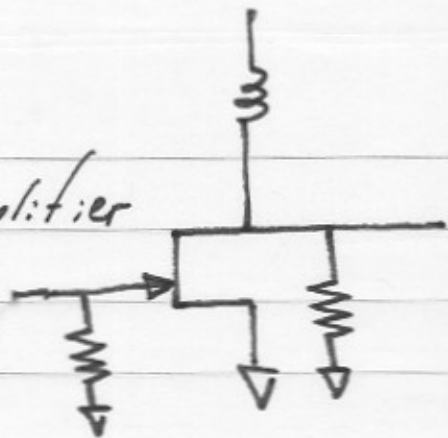
required freedom to choose both the gate & drain line impedances to values imposed by circuit design (e.g. not 50Ω) - or it required, if $Z_g = Z_d = 50\Omega$ that to be some fixed number (e.g.

I can design for a particular gain which will give me to $f_m = f_{max}$, but if I design for other gains, I will not obtain this.

The situation is particularly severe if cascade cells are used, in which case the output impedances are very high and the "optimum" drain line impedance ridiculously and impossibly high.

We have just published a solution for this, called Capacitive division. The description follows in a few pages.

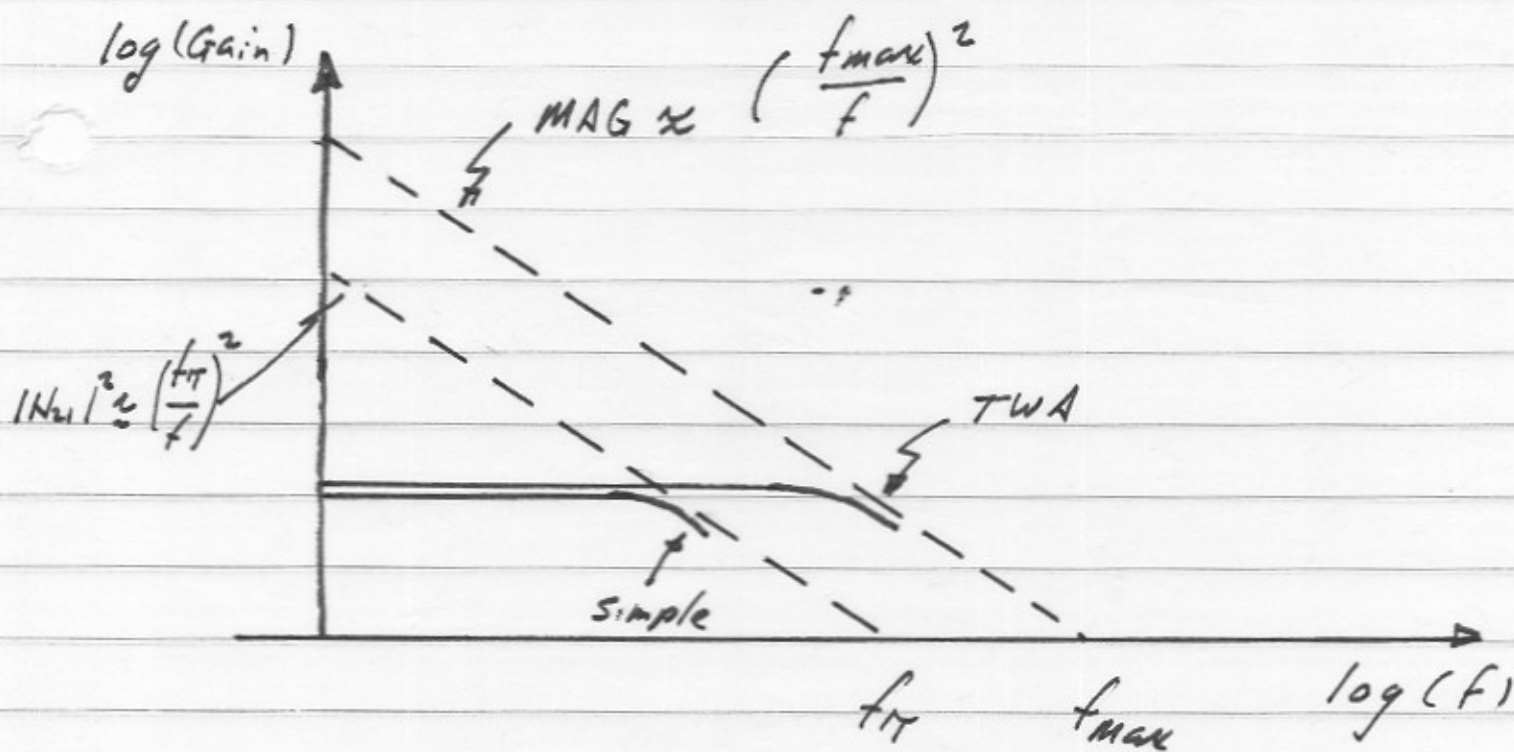
Simple Amplifier



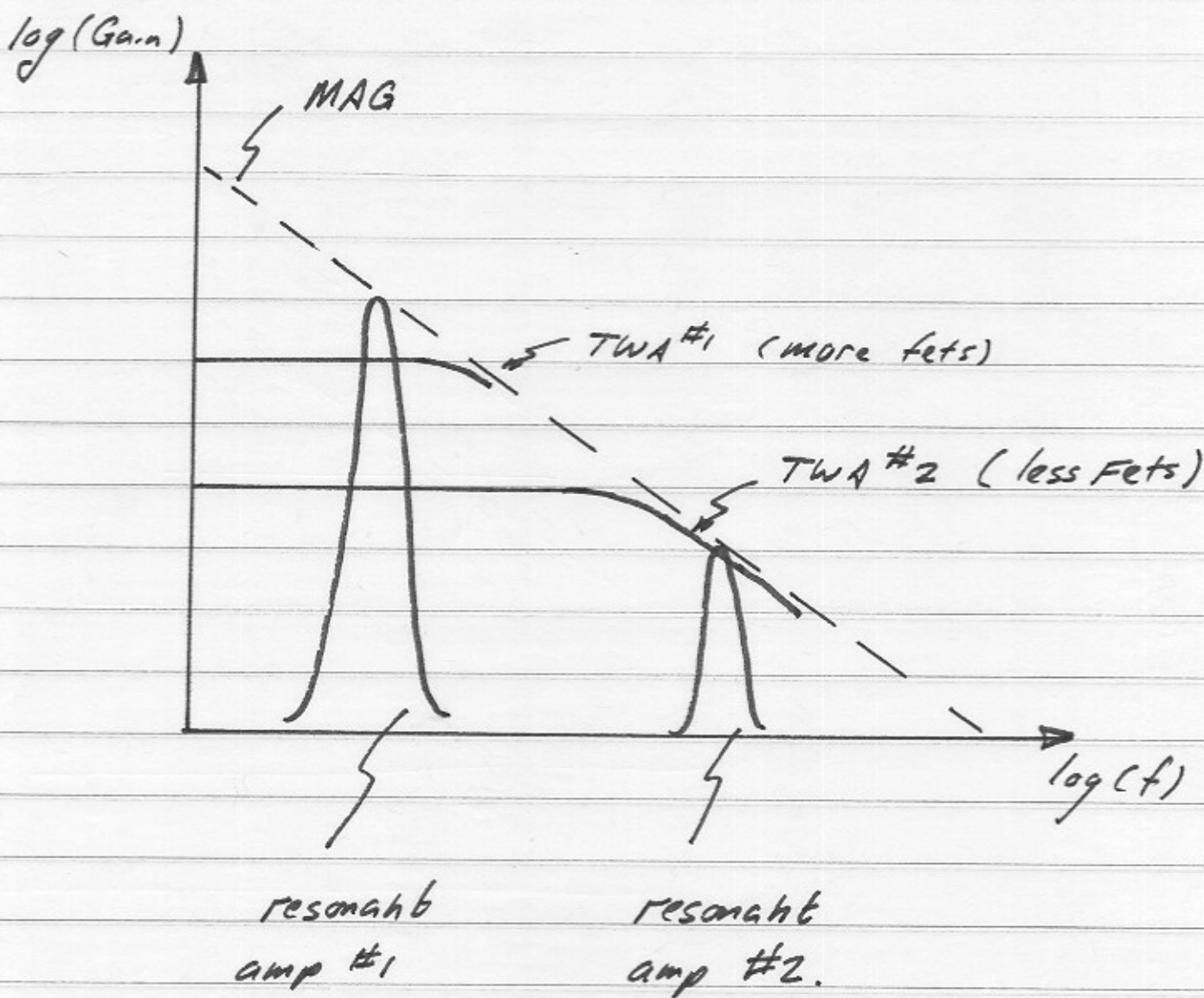
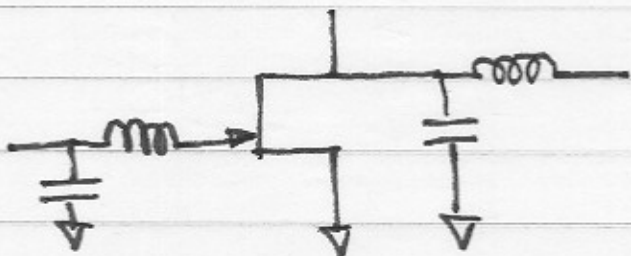
$$A_0 f_m = GBWP \cong \frac{1}{f_H}$$

TWA:

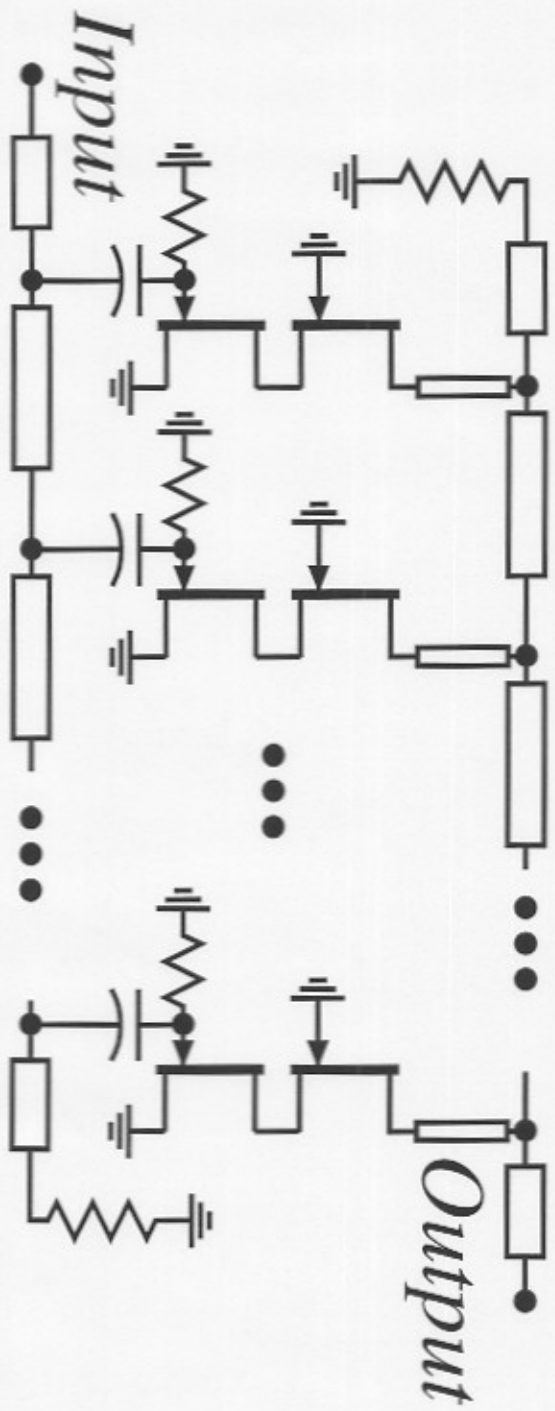
$$A_0 f_m = GBWP \cong f_{max}$$



Compare this to a resonated amplifier:



A description of Capacitive
Division follows.



... Allows obtaining gain-bandwidths
close to device limits for very good
strain impedances.

112-GHz, 157-GHz, and 180-GHz InP HEMT Traveling-Wave Amplifiers

Bipul Agarwal, Adele E. Schmitz, J. J. Brown, Mehran Matloubian,
Michael G. Case, *Senior Member, IEEE*, M. Le, M. Lui,
and Mark J. W. Rodwell

Abstract— We report traveling-wave amplifiers having 1–112 GHz bandwidth with 7 dB gain, and 1–157 GHz bandwidth with 5 dB gain. A third amplifier exhibited 5 dB gain and a 180-GHz high-frequency cutoff. The amplifiers were fabricated in a 0.1- μm gate length InGaAs/InAlAs HEMT MIMIC technology. The use of gate-line capacitive-division, cascode gain cells and low-loss elevated coplanar waveguide lines have yielded record bandwidth broad-band amplifiers.

Index Terms— Distributed amplifier, MMIC, traveling-wave amplifier, TWA.

I. INTRODUCTION

BROAD-BAND amplifiers find applications as gain blocks in multigigabit fiber-optic receivers and as preamplifiers in broad-band instrumentation. Future 100- and 160-Gbit/s optical transmission systems will require amplifiers with very high bandwidths. High-electron mobility transfer (HEMT) traveling-wave amplifiers (TWA's) with ≈ 100 GHz bandwidths have been demonstrated [1]–[3]. Puhl *et al.* [2] used capacitive voltage division [4] on the gate synthetic line to obtain 11 dB gain over a 1–96-GHz bandwidth. Capacitive division decreases the frequency-dependent losses on the gate synthetic transmission line. With these losses reduced, the number of TWA cells can be increased to increase TWA gain. In this manner, the feasible gain for a given design bandwidth is increased. With very small capacitive division ratios, losses associated with the HEMT input resistance are reduced to the point where other loss mechanisms are significant. If the dominant loss mechanisms are the HEMT series input resistance and shunt output conductance, the capacitive-division TWA can obtain gain–bandwidth products limited by the transistor power gain cutoff frequency f_{max} . If a cascode cell is used as the transconductance element with the TWA, the gain–bandwidth product can be increased well beyond the transistor f_{max} .

For design bandwidths above 100 GHz, TWA design is strongly impacted by both the losses and physical dimensions of the synthetic transmission lines. With small capacitive division ratios and design bandwidths above 100 GHz,

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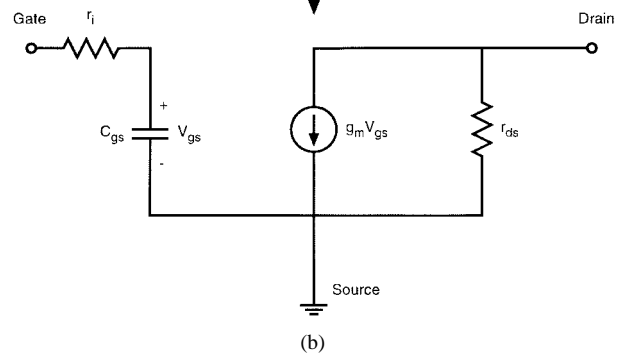
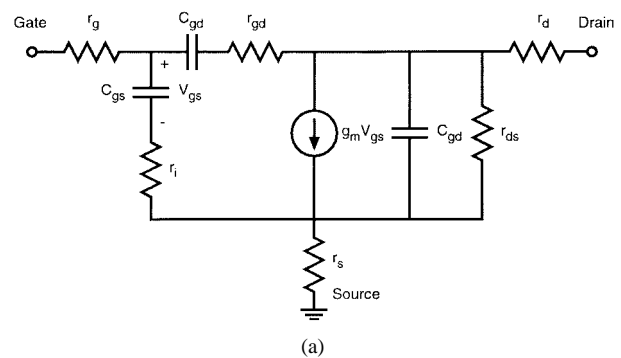


Fig. 1. Small-signal equivalent circuit of (a) a HEMT and (b) a simplified model.

transmission-line skin-effect losses impact the feasible amplifier bandwidth, and the required transmission-line lengths become shorter than the physical dimensions of the HEMT's, making the physical layout unrealizable. By using coplanar waveguide (CPW) transmission-lines with the center conductor raised $\sim 2 \mu\text{m}$ above the substrate [5], [6], the CPW effective dielectric constant is reduced, reducing the line skin-effect losses and increasing the wave velocity. Bandwidth is improved, and the physical layout becomes realizable.

Using gate line capacitive division and elevated CPW, we have fabricated TWA's with 1–112 GHz bandwidth at 7–10 dB gain and 1–157 GHz bandwidth at 5 dB gain. A third amplifier, processed on a wafer with a higher HEMT f_T , exhibited 5 dB gain and a 180-GHz high-frequency cutoff.

II. THEORY

Traveling-wave amplifiers are broad-band circuits whose gain–bandwidth product substantially exceeds the transistor

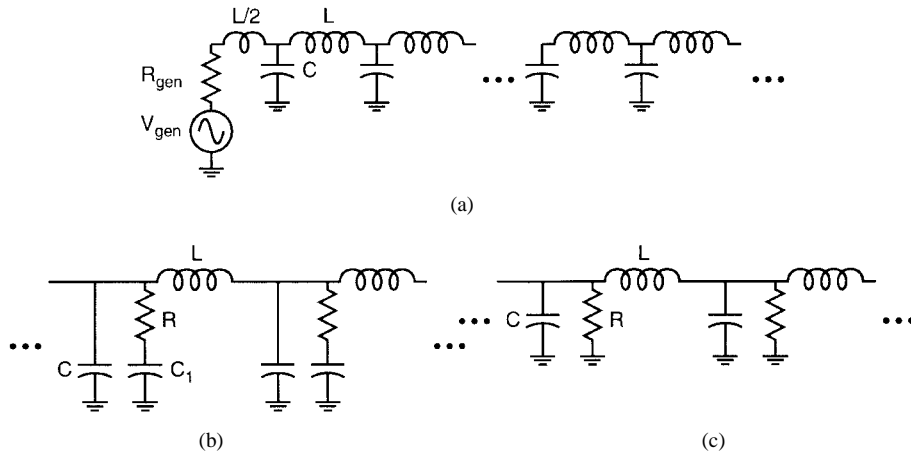


Fig. 2. Periodic synthetic transmission lines (a) without loss, (b) with frequency-dependent loss, and (c) with frequency-independent loss.

current-gain cutoff frequency f_τ . In TWA's, transistor input and output capacitances are absorbed into synthetic transmission lines (LC ladder networks). Amplifier bandwidth is then limited by the synthetic-line (Bragg) cutoff frequency, by frequency-dependent losses associated with the transistor input and output resistances, and by transmission-line losses. TWA design theory is described clearly in [7]. In the analysis below we show [2], [8] that with gate-line capacitive division, the gain-bandwidth product of a common-source TWA approaches the transistor f_{max} . With cascode gain cells and capacitive division, feasible gain at a given design bandwidth is, in principle, constrained by the cascode cells' maximum available gain, although circuit size, power consumption, and line loss considerations will set feasible gains well below this limit.

Fig. 1 shows complete and simplified HEMT small-signal equivalent circuit models. Because of feedback through C_{gd} , TWA analysis with the full HEMT model is complex, and the simplified model of Fig. 1(b) will instead be used. Fig. 1(b) models only the dominant parasitics, e.g., the gate-source capacitance C_{gs} , the input resistance r_i , the transconductance g_m , and the output resistance r_{ds} . These elements scale with HEMT gate width (device area) W_g , with g_m and C_{gs} proportional to W_g and r_i , and r_{ds} proportional to W_g^{-1} . $f_\tau = g_m/2\pi C_{gs}$ and $f_{max} = f_\tau \sqrt{r_{ds}/4r_i}$ are independent of W_g .

Design relationships for synthetic lines are now required. The synthetic line of Fig. 2(a) is lossless for frequencies below the Bragg cutoff frequency $f_B = 1/\pi\sqrt{LC}$, but has very high attenuation for $f > f_B$. For frequencies well below the Bragg frequency, the synthetic line has characteristic impedance $Z_0 = \sqrt{L/C}$ and per-section delay $T = \sqrt{LC}$. If a small series resistance R is added with a portion C_1 of the shunt capacitance as in Fig. 2(b), the line becomes lossy. The frequency-dependent loss per section is given by $e^{-\alpha}$, where

$$\alpha \simeq 4\pi^2 f^2 C_1^2 R Z / 2. \tag{1}$$

Adding a large shunt loading resistance R as in Fig. 2(c) introduces a frequency-independent loss per section $e^{-\alpha}$,

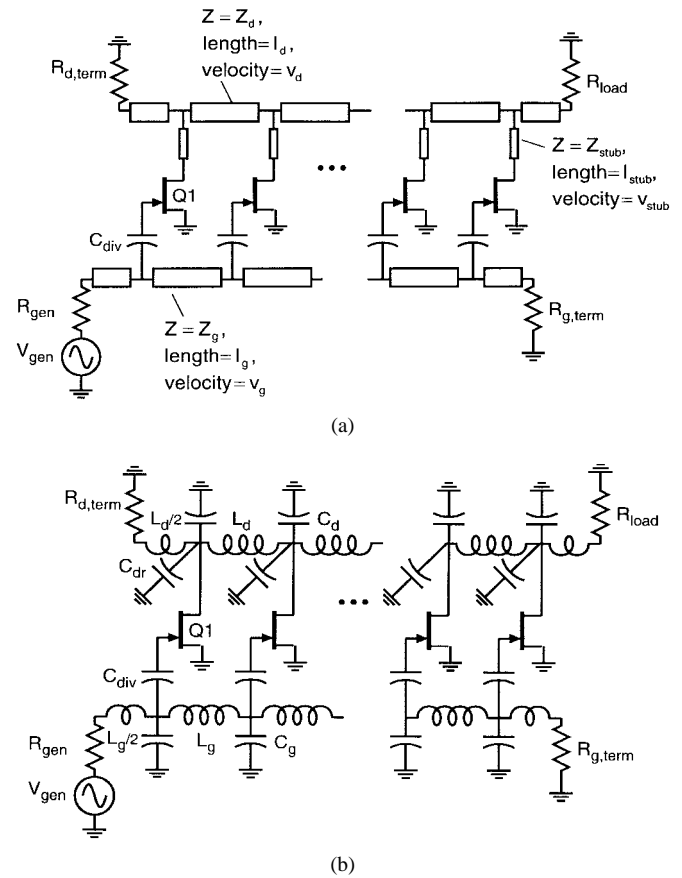


Fig. 3. Circuit diagram of the capacitive-division traveling-wave amplifier with (a) transmission-line tuning sections and (b) approximate equivalent LC model.

where

$$\alpha \simeq Z/2R. \tag{2}$$

Fig. 3(a) shows a HEMT capacitive-division traveling-wave amplifier. In this circuit, inductive and capacitive reactances are implemented through transmission line sections. In both the gate and drain circuits, inductors are approximated with high-impedance line sections (Z_g and Z_d), while shunt capacitors are implemented with series stubs (Z_{stub}). These line sections

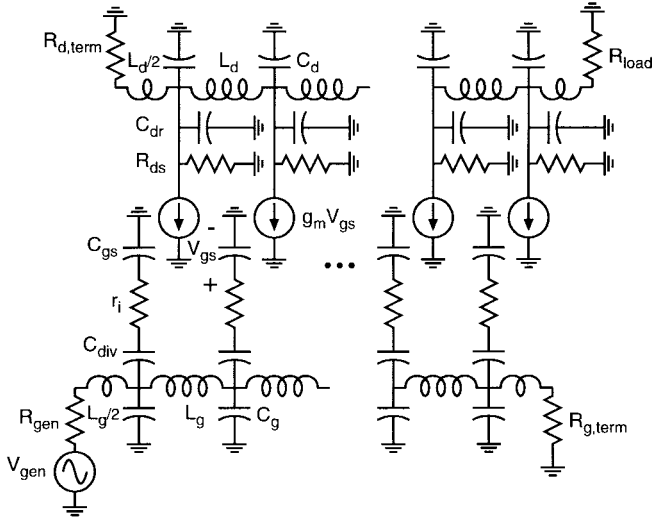


Fig. 4. Small-signal model of the amplifier.

are short in comparison with a wavelength and can be modeled with LC π -sections, resulting in the circuit model of Fig. 3(b). The gate-circuit series lines of characteristic impedance Z_g , phase velocity v_g , and length l_g are modeled in Fig. 3(b) as the inductances $L_g = Z_g l_g / v_g$ and the capacitances $C_g = l_g / v_g Z_g$. Similarly, the drain-circuit series lines of characteristic impedance Z_d , phase velocity v_d , and length l_d are modeled as $L_d = Z_d l_d / v_d$ and $C_d = l_d / v_d Z_d$, while the drain series stubs are modeled as capacitances $C_{dr} = l_{\text{stub}} / v_{\text{stub}} Z_{\text{stub}}$.

Using the simplified LC representation, Fig. 4 shows the TWA small-signal equivalent circuit. Both the gate and drain synthetic lines will be designed for characteristic impedance Z_0 , e.g., $Z_{0,g} = Z_{0,d} = Z_0$. The gate (input) and drain (output) transmission lines are terminated with the synthetic-line characteristic impedance $R_{g,\text{term}} = R_{d,\text{term}} = Z_0$, and the generator and load impedances are both equal to Z_0 . C_{div} is the gate-line division capacitor and M is the capacitive-division ratio

$$M = C_{\text{div}} / (C_{\text{div}} + C_{gs}). \quad (3)$$

The case $M = 1$ corresponds to a TWA without capacitive division. C_{dr} , the stub capacitance, is introduced to adjust the drain-line per-section delay T_d . In design, T_d is made equal to the gate-line per-section delay T_g , e.g., $T_g = T_d = T$. This results in the drain currents of the N HEMT's collectively adding in-phase at the amplifier output.

For the gate line, the loaded characteristic impedance, per-section delay, Bragg cutoff frequency, and per-section attenuation are

$$\begin{aligned} Z_{0,g} &= Z_0 = \sqrt{L_g / (C_g + MC_{gs})} \\ T_g &= T = \sqrt{L_g (C_g + MC_{gs})} \\ f_{B,g} &= 1 / \pi \sqrt{L_g (C_g + MC_{gs})} \\ \alpha_b &\simeq 4\pi^2 f^2 M^2 C_{gs}^2 r_i Z_0 / 2. \end{aligned} \quad (4)$$

Similarly for the drain line, the loaded characteristic impedance, per-section delay, Bragg cutoff frequency, and

per-section attenuation are

$$\begin{aligned} Z_{0,d} &= Z_0 = \sqrt{L_d / (C_d + C_{dr})} \\ T_d &= T = \sqrt{L_d (C_d + C_{dr})} \\ f_{B,d} &= 1 / \pi \sqrt{L_d (C_d + C_{dr})} \\ \alpha_d &\simeq Z_0 / 2r_{ds}. \end{aligned} \quad (5)$$

Equalizing $Z_{0,g} = Z_{0,d}$ and $T_g = T_d$ simply requires that $L_g = L_d$, $C_g = C_d$, and $C_{dr} = MC_{gs}$.

Gain-bandwidth limits can now be derived. For each transistor, the input signal propagates through a section of the gate line before driving that transistor's input and producing a drain current $Mg_m V_{gs}$. The drain current generates a forward wave on the drain line of amplitude $Mg_m V_{gs} Z_0 / 2$. Given that we have set $T_g = T_d$, all HEMT outputs add in phase. The overall amplifier gain is

$$A_v = -NMg_m Z_0 / 2. \quad (6)$$

The number of HEMT sections is limited by line losses. The input voltage to the N th stage is attenuated by $e^{-(N-1/2)\alpha_g}$. Setting the total gate line losses to $e^{-1/2} \simeq -4$ dB, the maximum number of transistors N_{max} for a given desired bandwidth f_{BW} is given by

$$4\pi^2 f_{BW}^2 N_{\text{max}} M^2 C_{gs}^2 r_i Z_0 \simeq 1. \quad (7)$$

Beyond N_{max} , the transistors do not contribute to the output voltage as the driving gate voltage is small. From the drain line losses, the voltage due to the first stage is attenuated by $e^{-(N-1/2)\alpha_d}$ at the output. Setting the total drain line losses to $e^{-1/2} \simeq -4$ dB, the maximum number of transistors N_{max} is thus given by

$$N_{\text{max}} Z_0 / 2r_{ds} \simeq 1. \quad (8)$$

If there are more stages than N_{max} , the output of the first transistor is severely attenuated and does not contribute significantly to the output voltage. Using (6)–(8), the gain-bandwidth product is given by

$$A_v f_{BW} = g_m / 2\pi C_{gs} \sqrt{r_{ds} / 4r_i} = f_{\text{max}}. \quad (9)$$

The maximum TWA gain-bandwidth product is equal to the transistor f_{max} . In this analysis, transmission line skin-effect and radiation losses have been neglected. It is important to note that (7) and (8) can only be simultaneously satisfied if capacitive-division is used. Consequently, without capacitive division, the TWA gain-bandwidth product falls below f_{max} .

Higher TWA gains at a given design bandwidth are obtained using cascode cells. As a consequence of its high output impedance, the power gain of a cascode pair is considerably higher than for a common-source stage. Fig. 5 compares the maximum available gain (MAG) and maximum stable gain (MSG) of cascode and common-source gains for the specific HEMT's used in this work. The output impedance of the cascode pair is very high ($r_{ds}[1 + g_m r_{ds}]$ at moderate frequencies), and in a first analysis drain-line losses can then

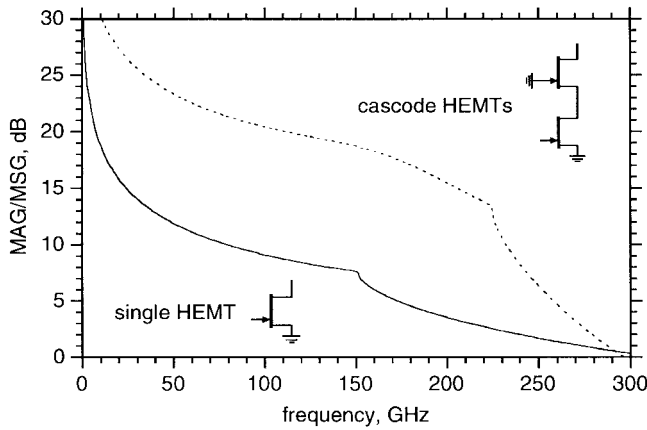


Fig. 5. Maximum available gain of a single transistor and cascode-connected transistors.

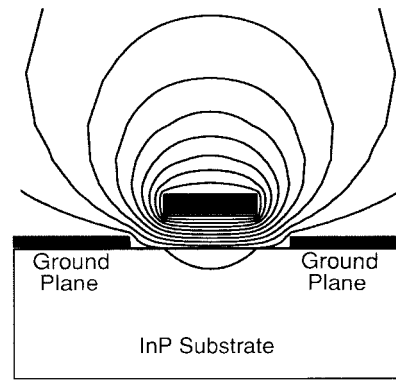


Fig. 7. Cross section and constant-potential profiles of elevated coplanar waveguide. With the center conductor raised 2 μm above the substrate, losses are reduced and wave velocity increased.

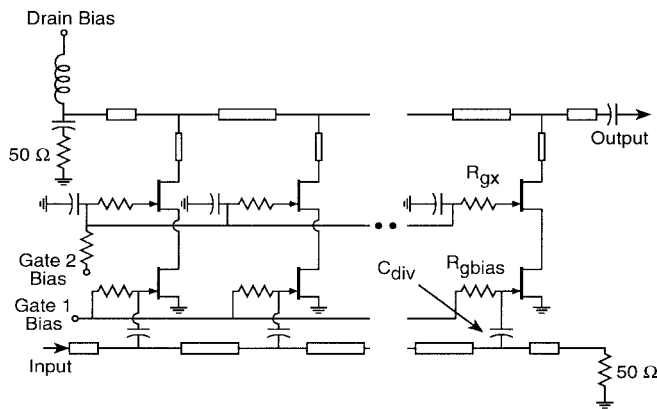


Fig. 6. Schematic circuit diagram of the cascode capacitive-division traveling-wave amplifier.

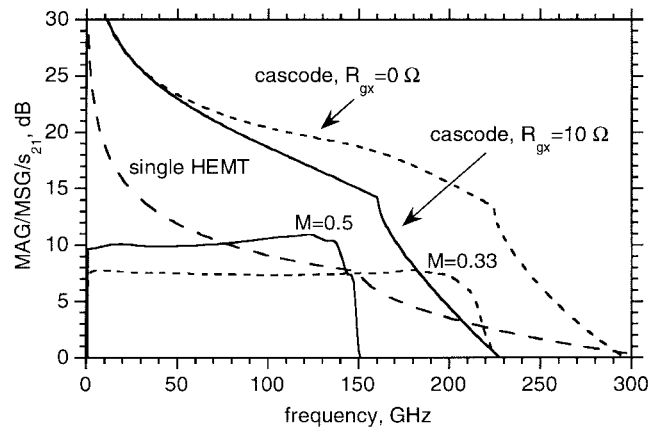


Fig. 8. Simulated gain-frequency characteristics of the two traveling-wave amplifiers.

be neglected. With this assumption, the following design equations can be derived:

$$\begin{aligned} \alpha_g &\simeq 4\pi^2 f^2 M^2 C_{gs}^2 r_i Z_o / 2 \\ \alpha_d &\simeq 0 \\ A_v &= -NMg_m Z_o / 2 \\ 4\pi^2 f_{BW}^2 N_{\max} M^2 C_{gs}^2 r_i Z_o &\simeq 1. \end{aligned} \quad (10)$$

Examining the gain-bandwidth product for this amplifier we obtain

$$A_v f_{BW}^2 = f_\tau / 4\pi M C_{gs} r_i. \quad (11)$$

From (11) it appears that the gain-bandwidth product can be increased arbitrarily to very high values by using aggressive capacitive-division (smaller M). This conclusion results from neglecting the cascode output conductance and is misleading. The amplifier gain is ultimately limited by the maximum available power gain of the cascode cell at any given frequency. This is not evident from the above analysis because the output impedance of a cascode cell is $\simeq r_{ds}(1 + g_m r_{ds})$ only at low frequencies, and an accurate drain line loss analysis is quite complex. The frequency dependent output impedance of the cascode can be derived by nodal analysis using the model of

Fig. 1(b) and is given approximately by

$$Z_{\text{out}} = \begin{cases} r_{ds}(1 + g_m r_{ds}), & \text{for } \omega \ll 1/C_{gs} r_{ds} \\ r_{ds} + g_m r_{ds} / j\omega C_{gs}, & \text{for } \omega \gg 1/C_{gs} r_{ds}. \end{cases} \quad (12)$$

This Z_{out} contributes to drain-line losses, with $\alpha_d \simeq (f/f_\tau)^2 (Z_o/2r_{ds})$, as per earlier analysis. In the idealized case where drain-line transistor Z_{out} losses dominate, a detailed analysis shows that the TWA gain can approach the maximum available gain of the cascode cell. However, generally Z_{out} for the cascode is sufficiently high that drain-line losses due to the cascode output impedance are much smaller than the drain-line skin-effect losses and can therefore be neglected. The TWA gain is then smaller than the cascode MAG.

For high bandwidths and high capacitive-division ratios (lower M), the transistor area becomes larger, the per-section length of transmission lines decreases, and the number of cells increases. This causes two difficulties. First, there may be a physical layout problem because of the increased transistor sizes and reduced transmission line lengths. Second, as the number of cells increases, transmission-line skin-effect losses may limit the attainable gain from the amplifier. The skin-effect losses also need to be reduced. If a coplanar waveguide with a raised center conductor [5], [6] is used, both these difficulties are addressed.

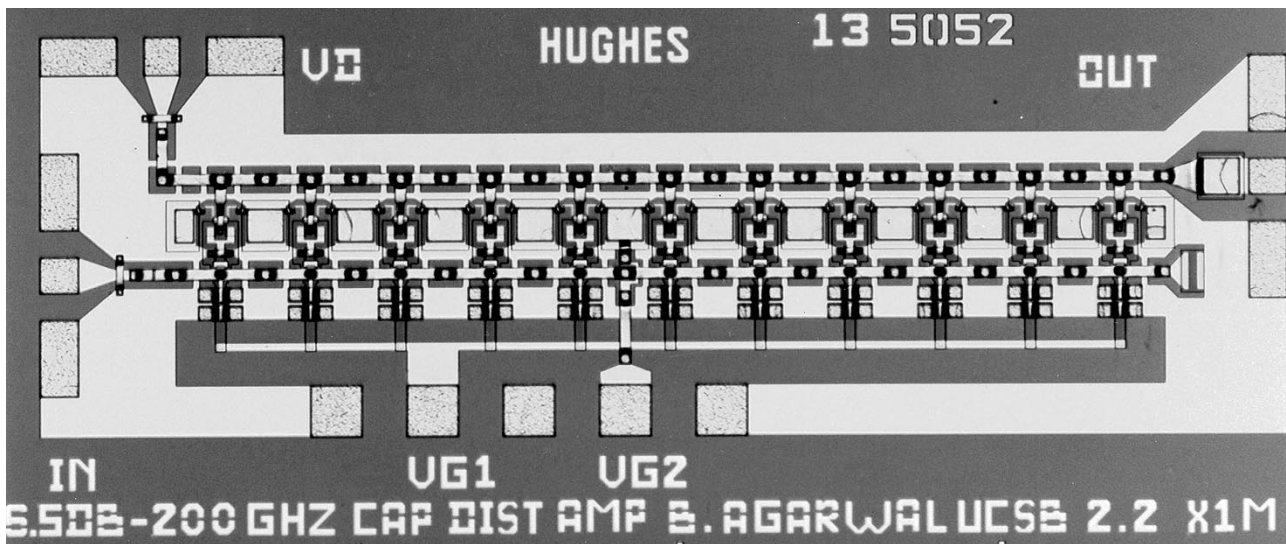


Fig. 9. Photomicrograph of the amplifier IC with 11 cells.

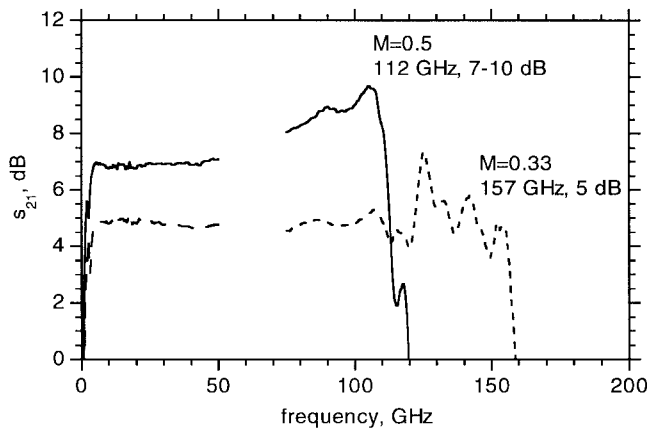


Fig. 10. Measured forward gain s_{21} of the two amplifiers.

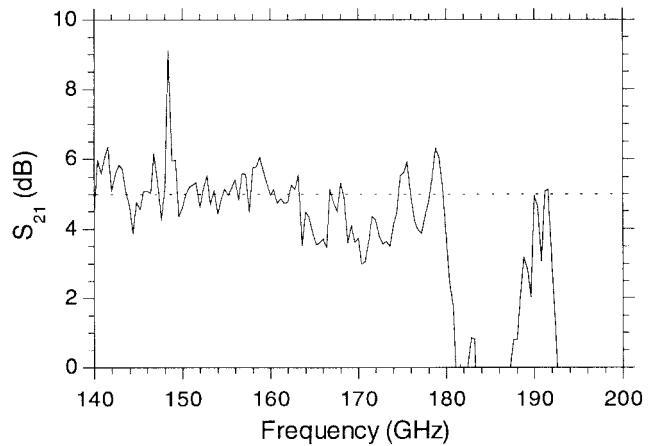


Fig. 12. Measured forward gain s_{21} for a TWA with 0.33:1 capacitive division and increased HEMT f_T .

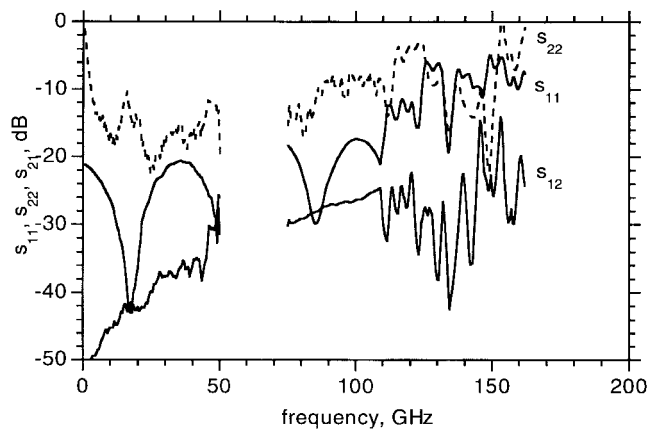


Fig. 11. Measured input return loss s_{11} , output return loss s_{22} , and reverse isolation s_{12} of the amplifier with 11 cells.

III. CIRCUIT DESIGN AND FABRICATION

Using capacitive-division, cascode HEMT cells and coplanar waveguides with raised center conductors, two amplifiers were designed. Fig. 6 shows the circuit diagram. Cascode HEMT's $Q1$ and $Q2$ are used to reduce drain line losses

and obtain high gain-bandwidth products. The gate and drain transmission lines are comprised of 75- Ω coplanar waveguide sections with center conductors raised 2 μm off the substrate (Fig. 7). These lines have a measured velocity of 1.78×10^8 m/s and a measured attenuation of 0.22 dB/mm at 20 GHz, increasing as the square root of frequency [6]. The drain line has a short 90- Ω transmission line section for delay matching between the gate and drain lines. C_{div} is the division capacitor at the input of the common-source transistor. R_{gx} , a small damping resistor in the gate of the common-gate transistor, is inserted to provide unconditional amplifier stability. $R_{g,\text{term}}$ is the 50- Ω gate termination resistor. $R_{d,\text{term}}$, the drain termination resistor, and the drain bias are connected through an off-chip bias tee. This was done because an on-chip resistor did not have enough current capacity to withstand the drain bias current. The two gate bias connections are also shown.

Two amplifiers were designed. The first amplifier had 11 cascode cells with a capacitive division ratio of 0.33:1. The simulated gain and bandwidth were 7 dB and 210 GHz, respectively. The second amplifier had eight cells and a capacitive-division ratio of 0.5:1. For this amplifier, the simu-

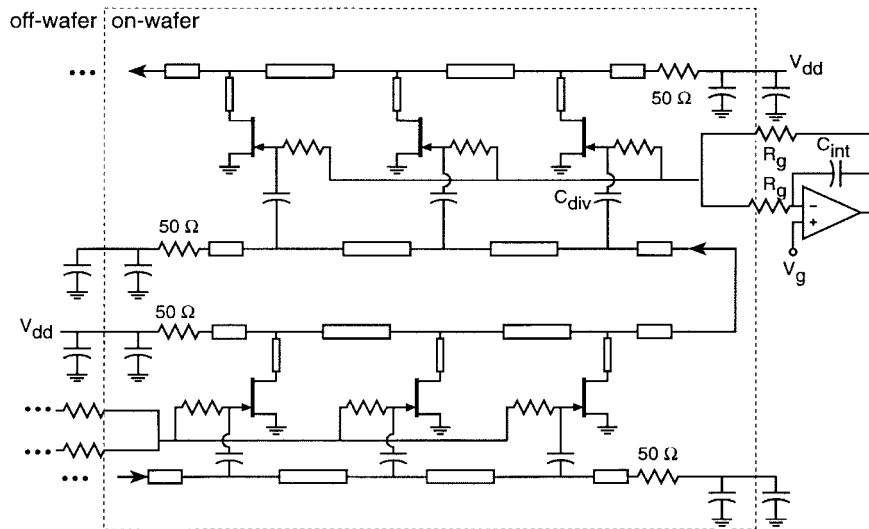


Fig. 13. Interstage ac coupling networks for extended low-frequency response.

lated gain and bandwidth are 10 dB and 140 GHz, respectively. Fig. 8 shows the two simulations together with the cascode-cell MAG/MSG. The MAG/MSG of a single transistor is also shown for comparison. As the figure indicates, the gate damping resistor reduces the maximum cascode cell gain.

The designs were implemented in a 0.1- μm gate length In-GaAs/InAlAs HEMT MMIC technology [9]. Typically, these HEMT's have $f_{\text{max}} = 300$ GHz and $f_{\tau} = 160$ GHz. Fig. 9 shows a photomicrograph of the fabricated chip with 11 cells. The die size is about 2.2 mm \times 1 mm.

IV. RESULTS

The amplifiers were tested on-wafer using commercial network analyzers from 0.045–50 GHz and 75–110 GHz. Beyond 110 GHz, we used in-house on-wafer network analysis based upon active probes [10]. Fig. 10 shows the measured forward gain s_{21} of the amplifiers. For the amplifier with 11 cells, the 3-dB bandwidth is 157 GHz and the gain is ≈ 5 dB. The eight-cell amplifier has 112 GHz bandwidth and 7–10 dB gain with a positive gain slope. The positive gain slope indicates that additional cells could have been added to this amplifier to obtain higher gain with a flatter response. The low frequency cutoff is about 1 GHz and is determined by the gate bias networks and by the output capacitor. Fig. 11 shows the input return loss s_{11} , the output return loss s_{22} , and the reverse isolation s_{12} of the amplifier. The amplifier output return loss s_{22} shows many resonances because of the off-chip drain-line termination.

The measured amplifier gains and bandwidths shown in Fig. 10 are lower than the design values because of low values of HEMT f_{τ} (≈ 110 GHz) on the tested wafer. Recently, a second process lot of amplifiers has been fabricated and tested. In this second process lot, using a modified HEMT design, the HEMT f_{τ} and f_{max} exceed the design values, and amplifier bandwidth is increased. These amplifiers were tested at NASA/JPL using a 140–220-GHz on-wafer vector network analysis system based upon harmonic mixers and waveguide-coupled micro-coaxial wafer probes. Measured over the 140–220 GHz band, the 11-stage amplifier exhibits 5 dB

gain and a 180-GHz high-frequency cutoff. As amplifier bias is varied, there is evidence of potential instability at 190 GHz.

We close with a comment on TWA's applications. If TWA's are to be used in optical fiber links with standard nonreturn to zero (NRZ) line coding, the low frequency response must extend to a frequency $\sim 10^5 : 1$ smaller than the bit rate. Despite capacitive coupling, extended low-frequency response can be obtained in capacitive-division TWA's using the bias network of Fig. 13. Here, interstage dc blocking is provided by the (small) division capacitor C_{div} . A low-frequency cutoff of ~ 1 MHz ($f_{\text{low}} \approx 1/\pi R_g N C_{gs}$) can be obtained using a large dc bias resistor $R_g \approx 1$ M Ω . With large values of R_g , dc bias errors will arise due to the HEMT gate leakage current. This can be suppressed by a closed-loop source/sense arrangement using an op amp integrator.

V. CONCLUSIONS

We have designed and fabricated TWA's having 1–112 GHz bandwidth with 7-dB gain and 1–157 GHz bandwidth with 5 dB gain. A third amplifier exhibited a 180-GHz high frequency cutoff with a 5-dB gain. Applications are in wideband instruments and in very high bit-rate fiber-optic systems.

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M. Le, photograph and biography not available at the time of publication.

M. Lui, photograph and biography not available at the time of publication.

Mark J. W. Rodwell, for photograph and biography, see this issue, p. 2307.