ECE202A Mid-Term Exam.

Nov. 10, 1992

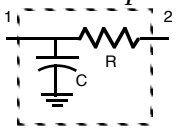
This is a 2-hour exam. There are 4 questions. Please don't turn the cover page until the exam is distributed to everyone.

Use any and all reasonable approximations in circuit analysis, after stating them.

Name: _____

Problem 1, 15 points:

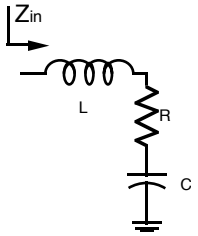
Basic Properties of S-Parameters



In the 2-port at right, C=0.2 pF and R=50Ω. Find S_{21} and S_{11}. The system impedance is 50Ω.

Problem 2, 20 points

Impedance matching and the Smith Chart



Over a limited frequency range, the input impedance of a packaged FET can be approximated as a 0.5 nH inductance in series with C=2.5 pF and R=25Ω

A. 10 points

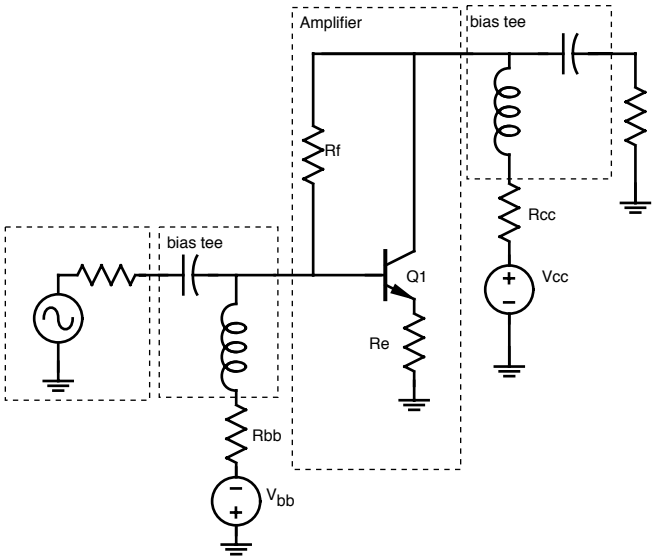
Using the supplied impedance/admittance chart, design a lumped-element matching network to match the input to 50Ω at 3.18 GHz. *Note that there may be several solutions: only give one, but make sure it does not use a series capacitor.*

B. 10 points

Using the solution of part A as a prototypes, give 2 approximate designs of matching networks using high impedance (1-0Ω) and low impedance (10Ω) lines. Both lines have effective dielectric constants of 2. Give line lengths in units of distance.

Problem 3, 30 points

When operating at a collector current of 15 mA and a 5 volt *collector-base* voltage, the transistor below has f_τ=100 GHz and C_{cb}=10 fF, and a 0.8 volt base-emitter voltage. r_{bb}=0 Ω and its parasitic series emitter resistance is also zero, ß=∞, and r_{ce}=∞. Vcc is +15 volts and Vbb is -15 volts.



A. 7 points

With the transistor biased as above, the amplifier is to have an input and output impedance of 50 ohms and a forward gain (S_{21}) of 12 dB at mid-band. Find R_f and R_e.

B. 7 points.

Given the stated bias conditions, find R_{bb} and R_{cc}.

C. 8 points.

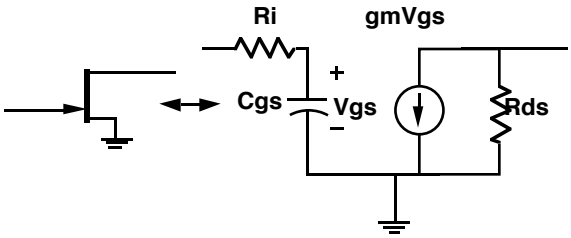
Calculate the 3-dB bandwidth of the forward gain S_{21}

D. 8 points

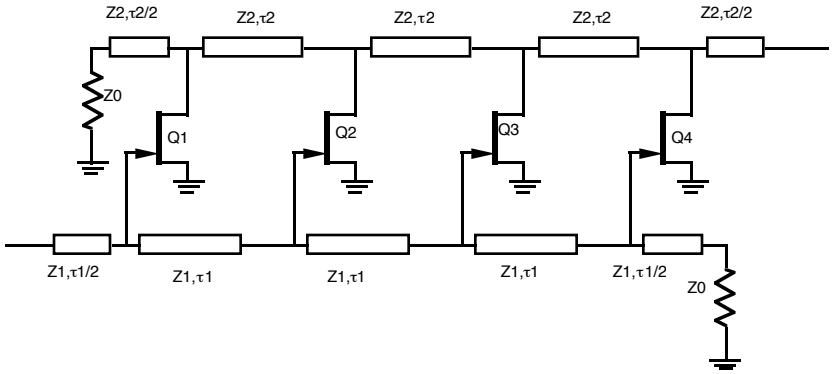
At the frequency which S21 is down 3 dB from the low-frequency value (part C) compute the magnitude of S11 in dB.

4. 35 points

Traveling-Wave Amplifiers, FET models



A GaAs Field-effect transistor has the equivalent circuit model on the left. gm=1/100Ω and Rds=2000Ω. The device has f_t=50 GHz and f_{max}=150 GHz. You will design a 4-FET TWA with the *modified* drain line design shown below. Z0=50Ω



A. 7 points

First, give the values for Cgs and Ri

B. 7 points

Assume that the characteristic impedance of the gate line sections is 100Ω. What is the electrical lenght τ1 of these line sections? What is the Bragg frequency on the gate line? Including the effects of the FET input capacitances, what is the delay between successive gates on the TWA?

C. 7 points

Now think carefully: what criteria must we place upon the drain line to have both the flattest possible frequency response and a 50Ω output impedance? Answer in words. Given these criteria, give values for Z2 and τ2.

D. 7 points

What is the low-frequency gain with drain line losses present? What would it be with zero drain line losses?

E. 7 points

Now neglect the drain line losses. What are the gate line losses per section at a frequency just below the gate-line Bragg frequency? Based upon this, what is the amplifier gain at that frequency?