ECE202A Mid-Term Exam.

Nov. 22, 1994

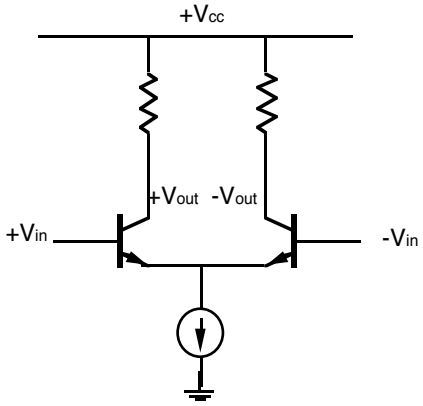
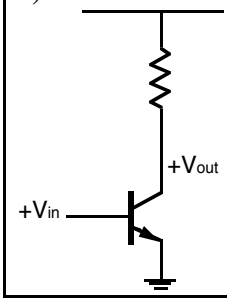
This is a 1 hour, 50 minute exam. There are 4 questions. Please don't turn the cover page until the exam is distributed to everyone.

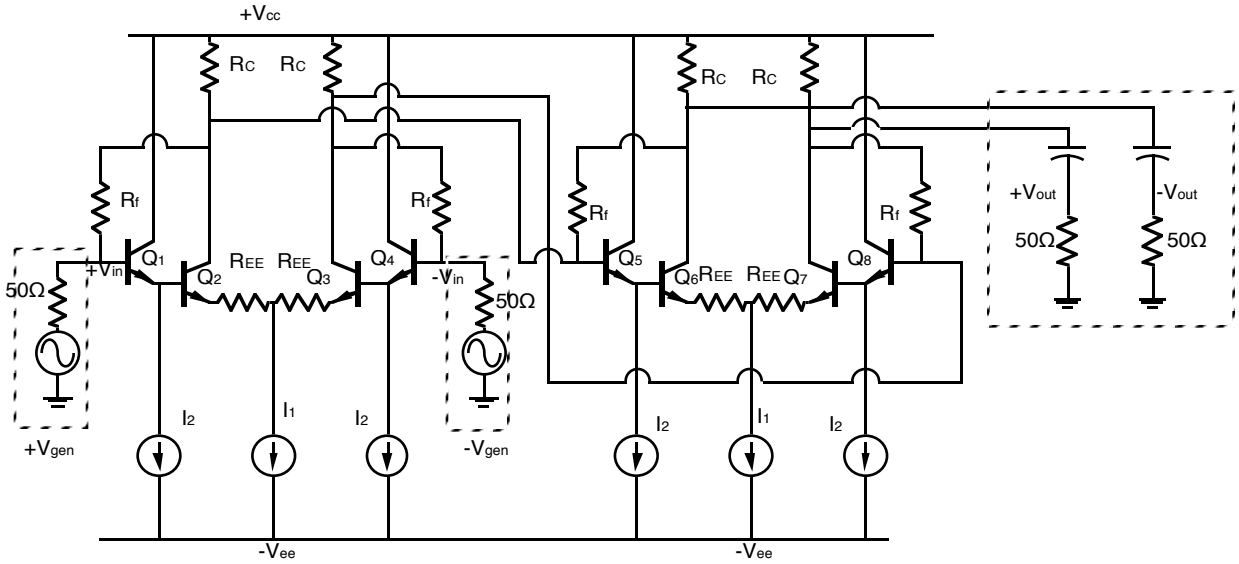
Use any and all reasonable approximations in circuit analysis, after stating them.

Name: _____

Problem 1, 25 points

General high-frequency circuit design

a)  	To give a reminder about differential amplifiers: with a differential circuit as shown on the left (a), with anti-symmetric input signals (+Vin and -Vin, as shown), the ac voltage at the emitter **is zero**, and the circuit can therefore be replaced in *ac small signal analysis* by the simpler circuit shown below (b) . The principle: at the point of symmetry, the AC voltage is zero, and hence is a virtual ground.
b)  	AC analysis is much easier (but note that the DC bias must be found from the full circuit) You will now use this method to solve a differential amplifier problem



The following values are given: +Vcc=+10V, -Vee=-10V, Vbe(on)=0.7V, $I_1=2I_2=10$ mA. Rc=2kΩ.

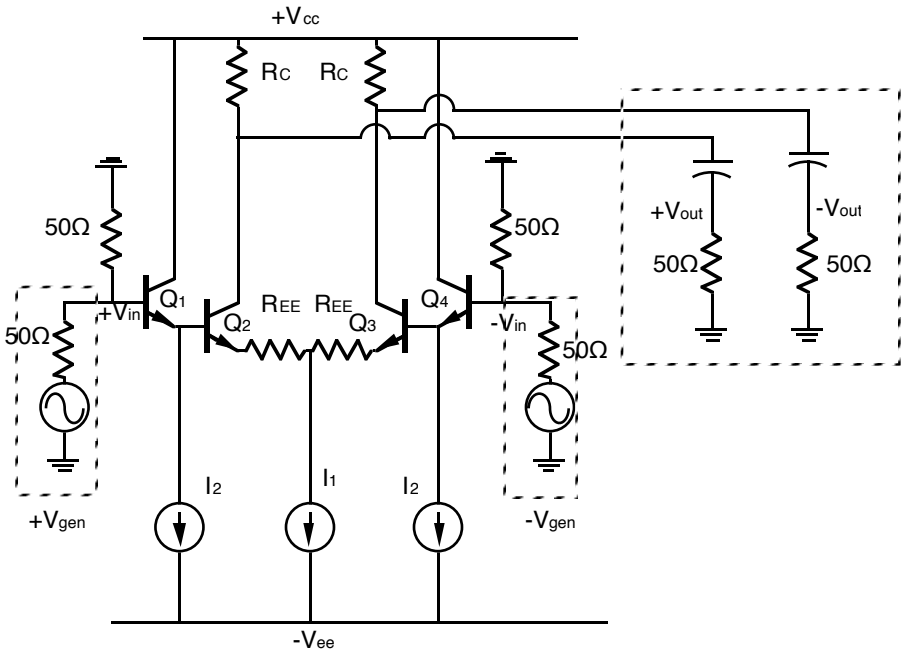
Hint as to a bias solution: the bases of Q1/Q4/Q5/Q8 will be at zero volts, and the collectors of Q2/Q3/Q6/Q7 will be at zero volts. When operating at a collector current of 5 mA, the transistors have f_τ=100 GHz and C_{cb}=10 fF, and a 0.7 volt base-emitter voltage. r_{bb}=0 Ω and its parasitic series emitter resistance is also zero, ß=∞, and r_{ce}=∞.

Part A, 10 points

Elementary feedback amplifier properties

It is desired that Vout/Vin=100 and that the amplifier have 50Ω input and output impedances. What are the required values of the feedback resistor R_f and R_{EE}?

Part C, 15 points
Bandwidth analysis

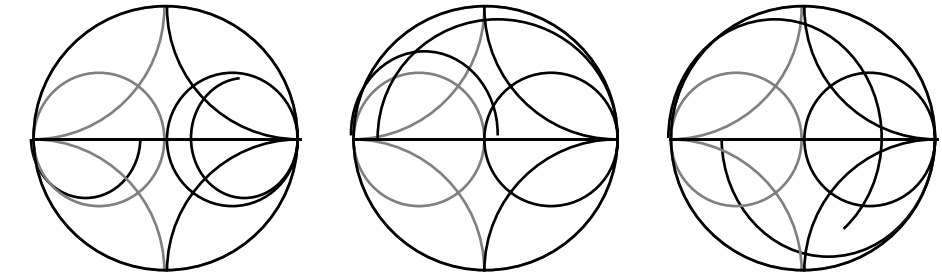


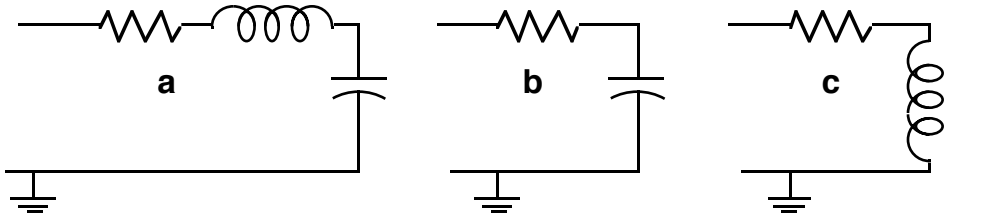
To simplify the problem for the exam, two changes have been made:
• There is only a single stage
• There is no longer a feedback connection

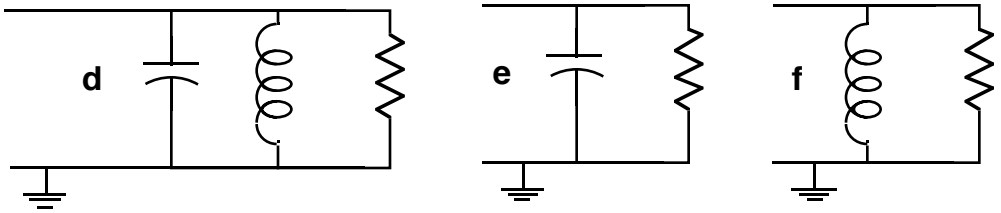
Using the method of time constants, find the dominant and the second-order poles

Problem 2, 15 points
Smith chart and S-parameters

Part xx, 10 points
Familiarity with the Smith Chart



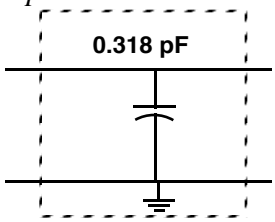




Above are plotted the input reflection coefficients of six networks as a function of frequency. Label each curve with the letter corresponding to the appropriate network.

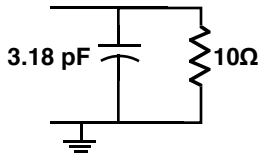
Part xx, 5 points

S-parameter Calculation



Calculate the magnitude and phase of S21 at f=10 GHz for a 50Ω system impedance definition.

Problem 3, 20 points
mpedance--matching



This is a rough model of a the impedance of a semiconductor laser under bias. We will be working at 10 GHz.

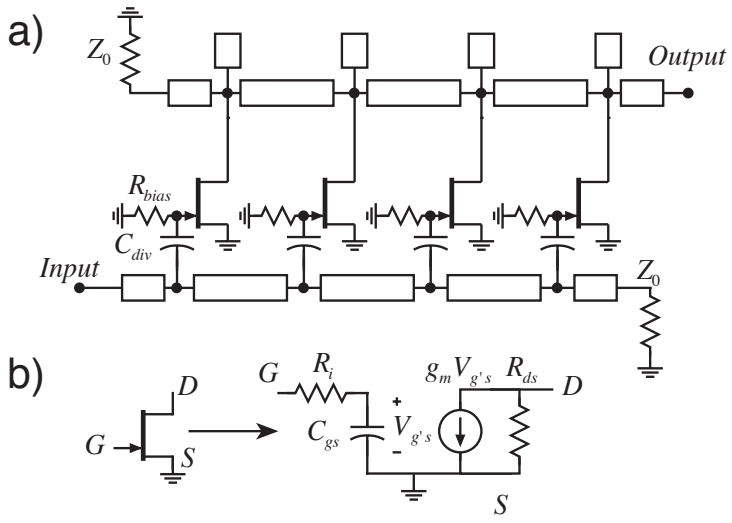
Part a, 10 points
Using the attached Smith Chart, design lumped-element (LC) impedance-matching networks to match the laser to 50Ω. There are several possible solutions; make sure that the solution chosen use shunt capacitors and series inductors.

Part b, 10 points

lumped-element equivalents

Lumped elements are not available to you. Instead, the matching network must be implemented using lines of 10Ω or 100Ω characteristic impedance. All lines have an effective dielectric constant of 4. Draw the circuit diagrams of the resulting approximate distributed realization of the lumped--element prototype, giving the physical lengths in mm and the characteristic impedances.

Problem 4, 40 points
Traveling--wave amplifiers



A capacitive-division traveling-wave amplifier and the FET model are shown at left. Each of the 4 FETs has gm=100 mS, Rds=500Ω, f_t=100 GHz, Ri=10Ω, f_{max}=200 GHz.

Although the circuit diagram shows 4 TWA cells, the Amplifier has 8 cells.

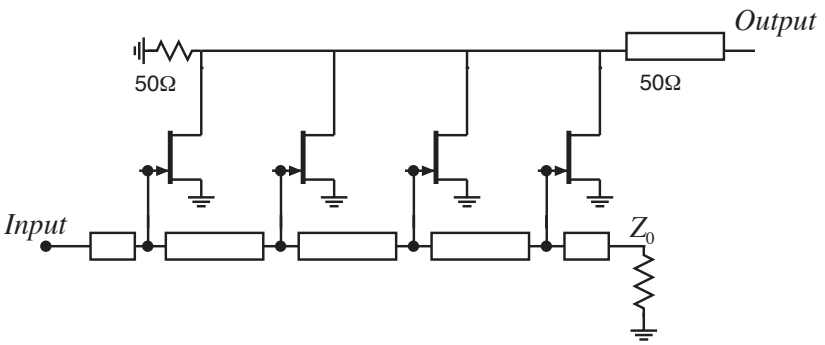
Part A, 10 points
Synthetic Line Principles
The amplifier is to have 50Ω synthetic gate and drain lines. All series line sections are to be 100Ω, all shunt line sections are to be 20Ω.

Find the length of the series and shunt drain lines, and find the Bragg frequency.

Part B, 5 points
Find the low--frequency gain

Part C, 10 points
Losses
Find the per-section attenuation (nepers/section) on the gate line and drain line at 75% of the Bragg frequency. Comment as to what effect (if any) these will have on the amplifier performance

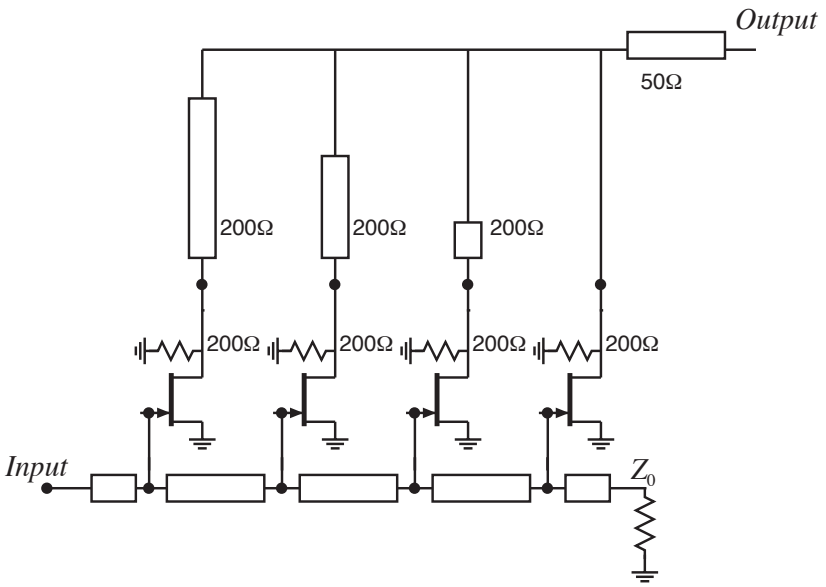
Part D, 10 points



Here is another traveling-wave amplifier. **There are 4 cells**. The FET parameters are as before. There is no capacitive division.

•Quickly work out the required lengths of lines on the gate circuit and the gate line bragg frequency (hint: you can use **scaling** from your answer of part a, so this should take no time at all).
•If we ignore gate-line and drain-line losses give **an estimate** of the amplifier bandwidth. Why is this a bad design?

Part E, 5 points



Here is yet another traveling-wave amplifier. **There are 4 cells**. The FET parameters are as before. There is no capacitive division. The gate line parameters are as in the previous section.

•What are the 200Ω lines for?
•What are the correct lengths (in units of time delay) of the 200Ω lines?
• Why don't we build TWAs like this?