ECE202a final exam

Tuesday, November 09, 1999

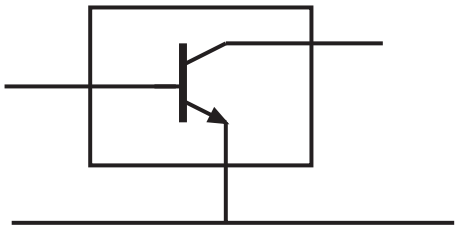
There are 3 problems, and you have 3 hours

Please do not start until the exams have been all distributed.

Use any and all reasonable approximations

Name: _____

Problem 1, 30 points



At a design frequency of 10 GHz, a transistor has

S11=0.5, S21=4 S22=0.8 S12=0

All defined for a reference 50Ω system impedance.

Part 1, 5 points

Find the transistor's maximum available gain at this frequency.

Part 2, 10 points

The generator impedance is 10Ω, while the load impedance is 100Ω.

Find the following:

the transducer power gain Gt=_____

the available power gain Ga=_____

the operating power gain Gp=_____

Part 3, 10 points

The generator impedance is 10Ω, while the load impedance is 100Ω.

If the power available from the generator is 1 mW, what is the load power?

Load Power=_____

If we placed an impedance-matching network between the generator and the transistor, but not between the transistor and the load, what would the load power be?

Load Power=_____

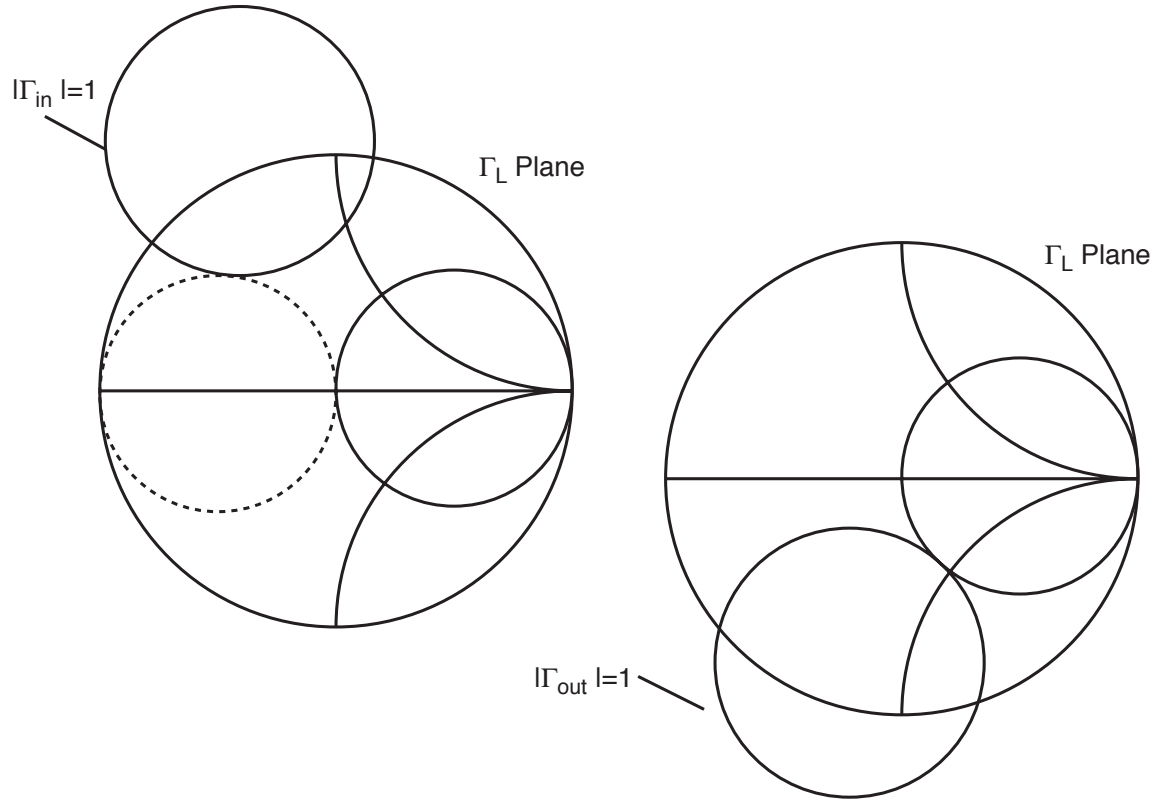
Part 4, 5 points

If the generator and load were instead both 50 Ohms, there were no matching networks, and there was 1 mW available from the generator, what would the load power be?

Load Power=_____

Problem 2, 30 points

Part 1, 10 points



|S11|<1, |S22|<1

Above are shown the stability circles for a common-source-connected FET at 10 GHz. The transistor can be stabilized by either shunt or series stabilization at either the Input or the output.

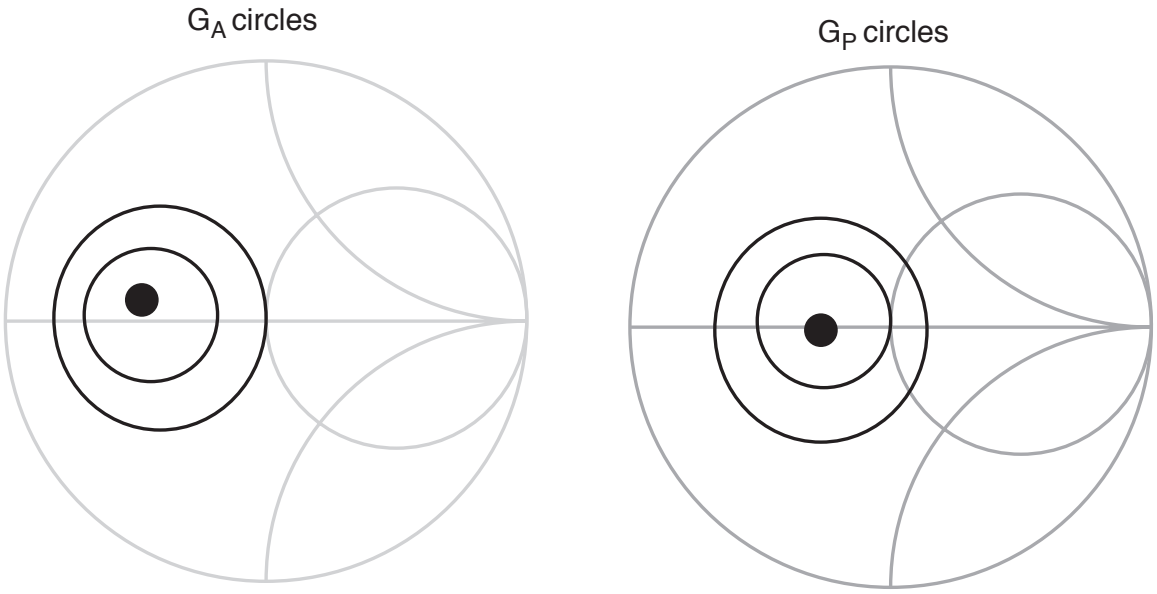
Draw circuit diagrams, with exact component values given, for 2 stabilization methods.

Part 2, 10 points

It so happens that the transistor itself has S21=3+j4, and S12=0.7+j0.7. The transistor S11 and S22 are not given, but the transistor is potentially unstable. After stabilization, and impedance matching on input and output, what is the transducer power gain obtained from the (stabilized and matched) transistor?

G_t=_____

Part 3, 10 points

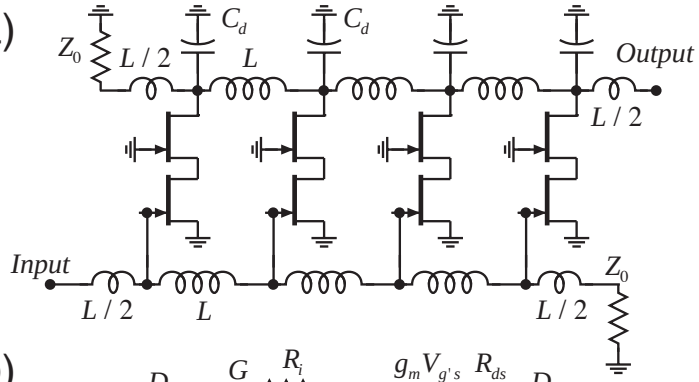


Here are Ga and Gp circles for a transistor, at 1 dB increments in Gain (50Ω impedance standard for the impedance charts). The transistor maximum available gain is 10 dB. If the input is impedance matched to the transistor, but the load impedance is 50Ω, what is the transistor transducer power gain?

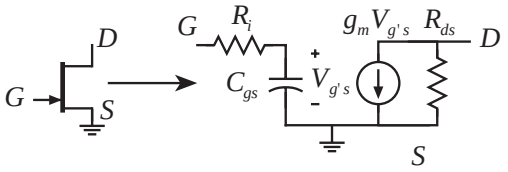
(the solid black dots are the impedances for maximum gain, not 1-dB contours)

Problem 3, 40 points

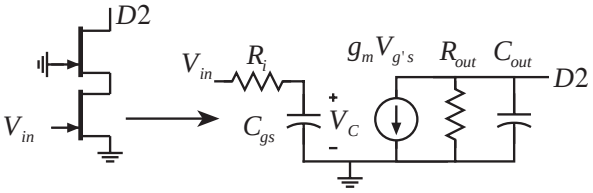
a)



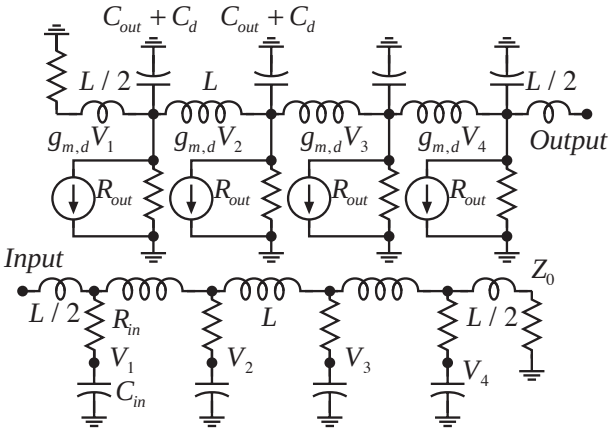
b)

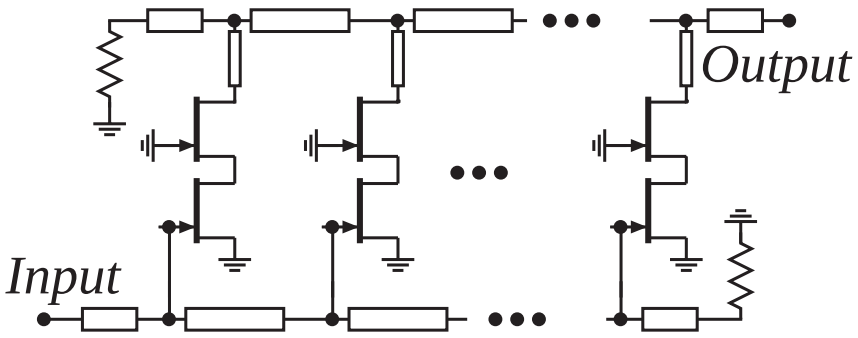


c)



d)





Circuit diagrams of a cascode traveling wave amplifier are shown on the previous page. As illustrated in b-c, a cascode combination can be viewed approximately as a single fet, where Ri, gm, Cgs are unchanged, and Rout is many times Rds. We will neglect the capacitance Cout.

The parameters of the cascode fet are gm=20 mS, Ri=25Ω, gmRout=50, and the fet ft=100 GHz.

Part 1, 5 points.

If the traveling-wave amplifier is to be implemented with inductor and capacitors (as in (a)), find the required values of the inductors L and drain-line capacitors Cd. Generator and load are to be 50Ω

Part 2, 5 points

Find the Bragg frequency of the synthetic lines.

Part 3, 10 points

Using the criterion of having no more than 3 dB total attenuation on the gate transmission line at the highest frequency of interest (the Bragg frequency in this case), find the maximum number of FET cells in the TWA

Part 4, 5 points

What is the amplifier mid-band gain S21?

Part 5, 10 points

We will now re-implement the inductors and capacitors with microstrip lines having effective dielectric constants of 2. The series lines will be 75 Ω impedance. Calculate the physical length (in μm) of all required transmission lines.

Part 6, 5 points

The Bragg frequency has now dropped. What is it now?