ECE 202A Problem set xx : Device Modeling.

Background

A recurring activity in semiconductor organizations, whether scientific or industrial, is developing high frequency models of semiconductor devices. Devices are measured on a microwave network analyzer, generally using microwave wafer probes. Devices are measured over a wide frequency range, as a function of DC bias, and perhaps as a function of device size and or lithographic design rules.

An activity then follows referred to as "model extraction". This means, fitting an equivalent circuit model to the device.

There are 2 intended purposes:

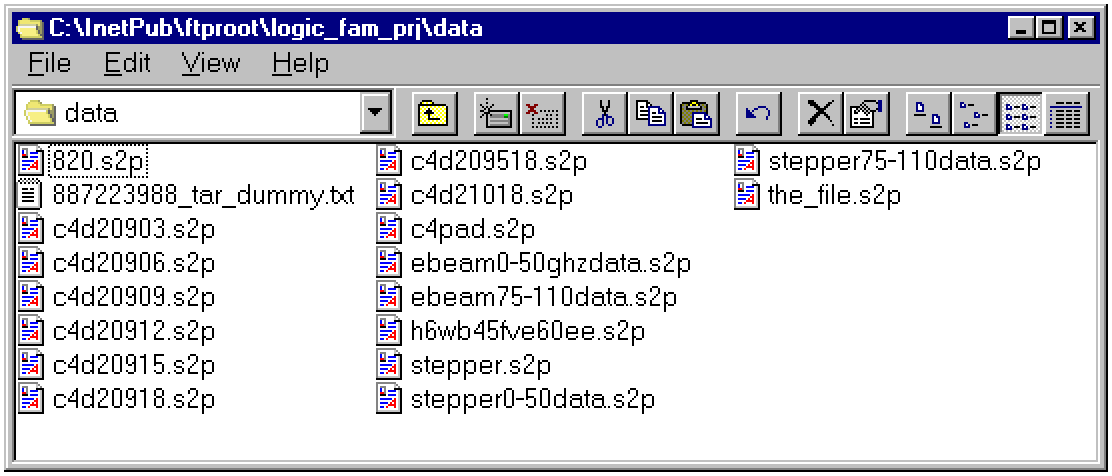
1) having a compact equivalent circuit model for circuit analysis. One would hope that the model can track adjustments in device DC bias and device size.

2) developing an electrical model which reflects the underlying device physics. If done properly, the device designer will then know **why** the device has its specific characteristics, and will know what to do to make the device better.

There is a common industrial practice of using a random search mathematical algorithm. The electrical circuit parameters are adjusted until the best fit is obtained between the measured electrical device parameters and an equivalent circuit model . This is sometimes (but not always) adequate for the first purpose, and emphatically not adequate for the second purpose.

We seek a systematic approach. This will be illustrated by model extraction for an HBT.

I have added to the data directory a number of files.

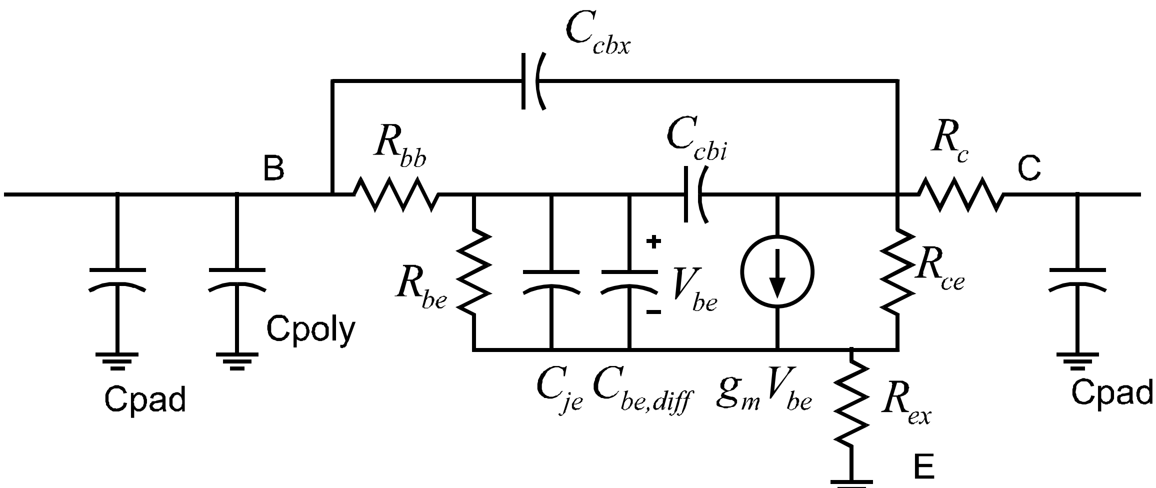


The files of concern here are those beginning with "c".

file	Vce, volts	Ic, mA
c4d20903	0.909	2.96
c4d20906	0.908	5.92
c4d20909	0.910	8.93
c4d20912	0.913	11.97
c4d20915	0.923	14.93
c4d20918	0.917	18.47
c4d2091518	0.95	17.94
c4d21018	1.0	18.27
c4pad	open pad test structure	*****

These are an HBT with a 300 Å thick base with 50 meV bandgap grading, and a 2000 Å thick collector. The emitter junction has dimensions on the mask are 0.7 μm by 12 μm , while the **physical** emitter dimensions are 0.6 μm by 12 . The collector dimensions are **physically*** 1.1 μm by 15 μm ; I recall that the junction was probably 1.2 micron width on the mask.

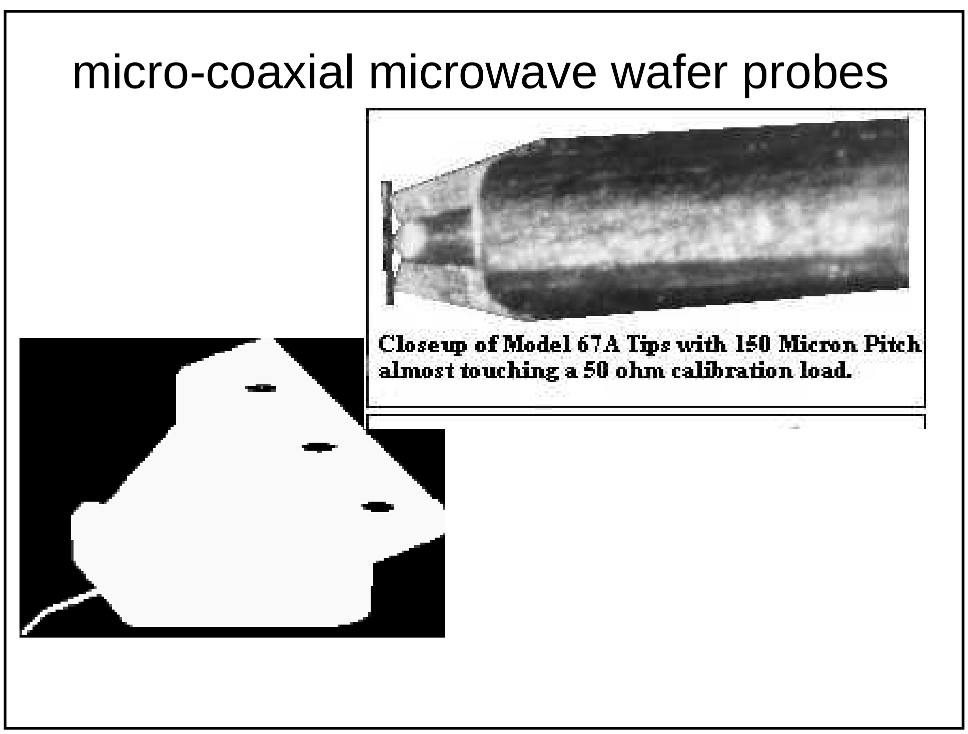
The objective is to develop an equivalent circuit model as below:



Where $C_{be,diff} = g_m \tau_f$, $R_{be} = \beta / g_m$, and $g_m = qI_c / NkT$. In our HBTs, we can safely ignore both Rc and Rce. On the other hand, we have a capacitance Cpoly arising from the device external layout (which I will give you as 7 fF). Further, though not shown above, Ccbi must have in parallel with it a resistance Rcb, which arises from weak collector-base avalanche breakdown.

Calibration methods:

This bears some discussion. The usual method is as below



Measuring Transistors on-Wafer

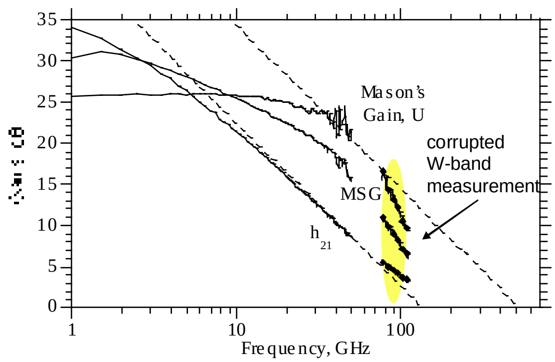
DC-50 GHz & 75-110 GHz Network Analysis

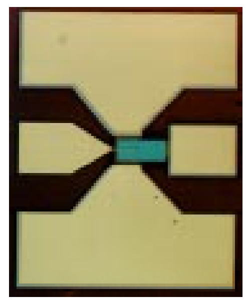
waveguide-coupled micro-coax probes

Parasitic probe-probe coupling

S_{12} error background: not corrected by calibration

$\rightarrow$ gain measurements corrupted, worse for W-band





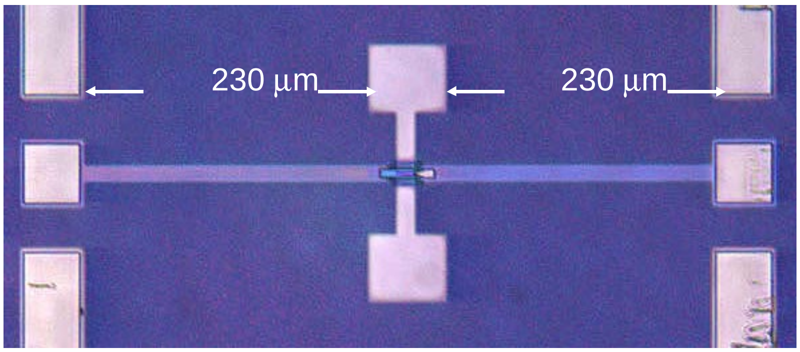
The picture above shows a transistor with **short** on-wafer pads. A separate calibration substrate with OSLT or LRL calibration standards are used to calibrate the network analyzer. This procedure does not fully calibrate out the pad capacitance. Hence, before measuring transistors, but after calibration, a pad structure with the transistor missing is measured. The S-parameters of this allow one to determine the pad capacitances to ground, which can then be subtracted from the transistor s-parameter data. There are some problems with this procedure, and hence I attach the 2 slides below for a better procedure using on-wafer LRL calibration standards; the problem there is that the on-wafer LRL standards prevent good calibration near DC. This exercise needs the data near DC, and hence uses the **short** on-wafer pads.

Measuring High f_{max} Transistors II

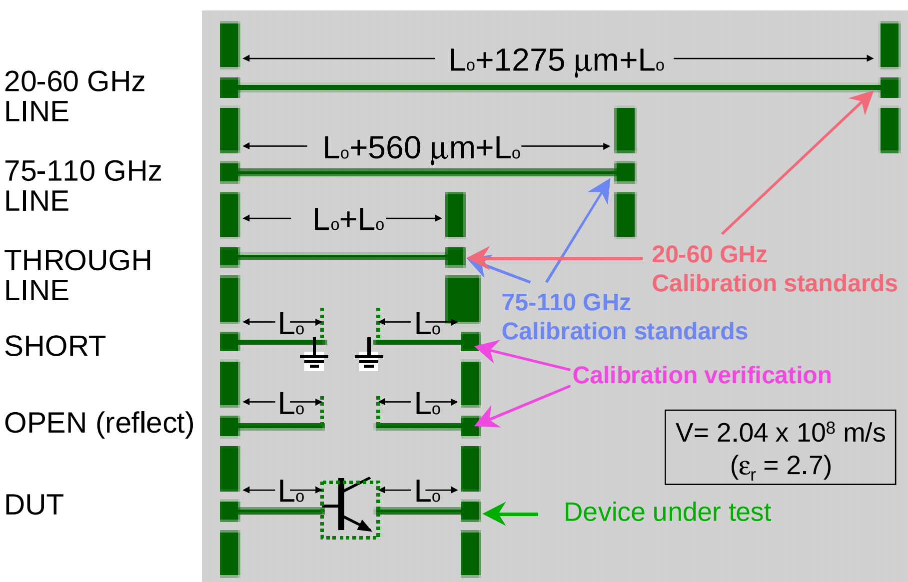
Offset reference planes, on-wafer LRL calibration standards

separate probes to reduce coupling

reference planes at transistor terminals



Line-reflect-line on-wafer cal. standards



The excess line length for the through lines is set to be lambda/4 at the center of the frequency band of interest, and the calibration method works for frequencies such that the excess line length lies between about lambda/8 and 3*lambda/8 . So, not a method for near-DC calibration.

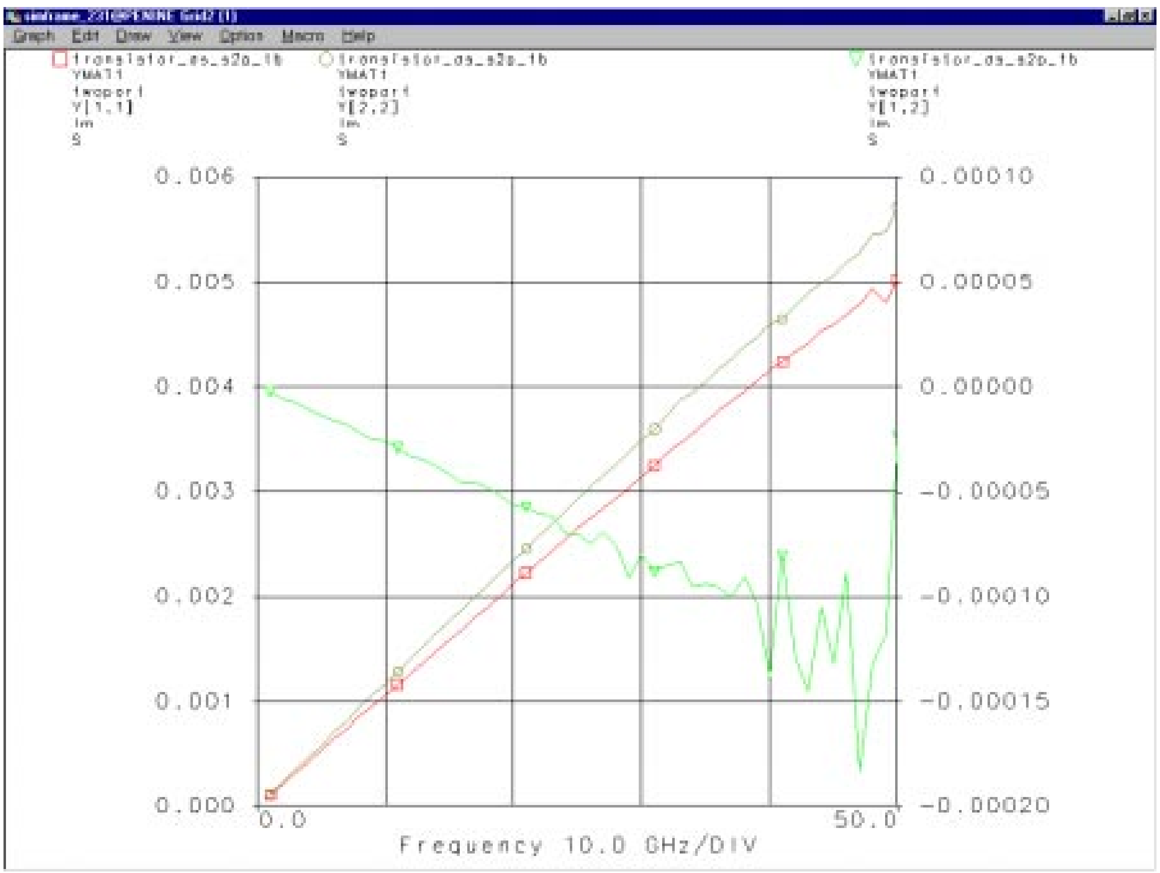
Again, the data you will be working with is from the "short pads" type of calibration. So, we need to strip pad capacitance.

The extraction procedure (hence the assignment)

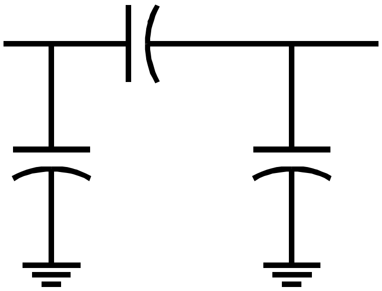
The procedure is as follows: (which are the steps in this exercise)

First

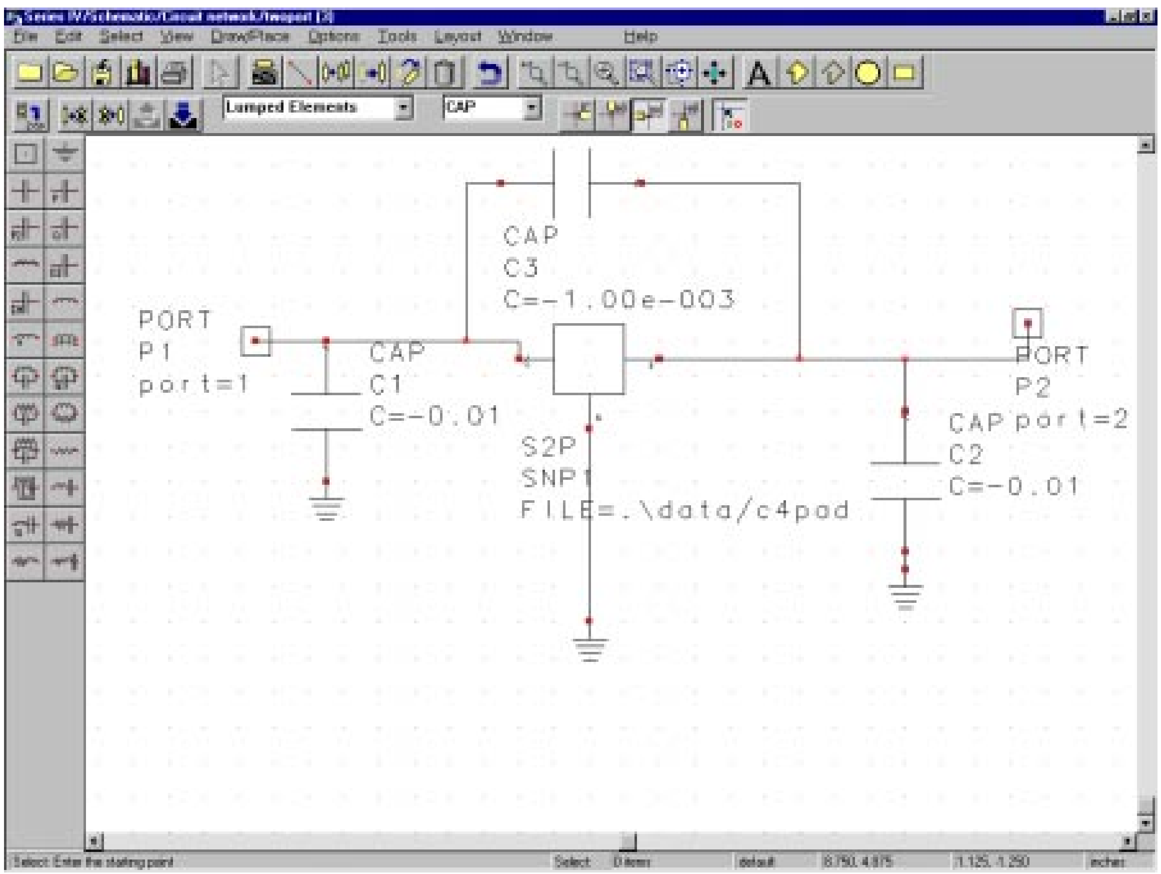
Simulate the open pads. Display the Y-parameters, like so…



and from the slope of the imaginary part of Y11 and Y22, determine the pad capacitances



you then place negatives of these pad capacitances around the device to strip off the pad capacitances….



I have used fictitious numbers above.

Again, the great weakness of the "short-pads" structure is this stripping…

<u>Second</u>

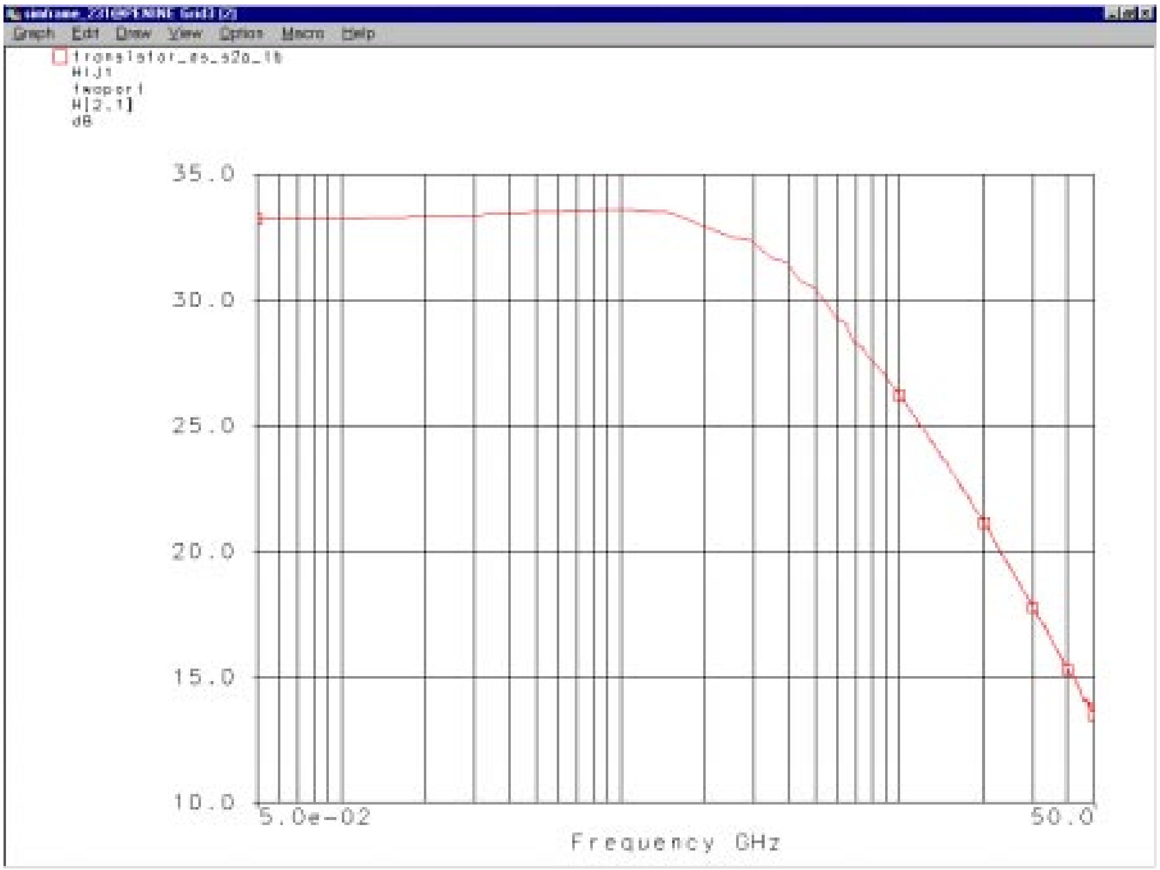
The device transconductance gm is given by $g_m = qI_c / NkT$. N is the ideality factor (read: fudge factor). We need to determine Rex and N. To do this, we use the relationship that at low frequencies,

$$Y_{21} = (R_{ex} + 1/g_m)^{-1} * \frac{\beta(R_{ex} + 1/g_m)}{R_{bb} + \beta(R_{ex} + 1/g_m)} = (R_{ex} + R_{bb}/\beta + NkT/qI_E)^{-1}$$, which

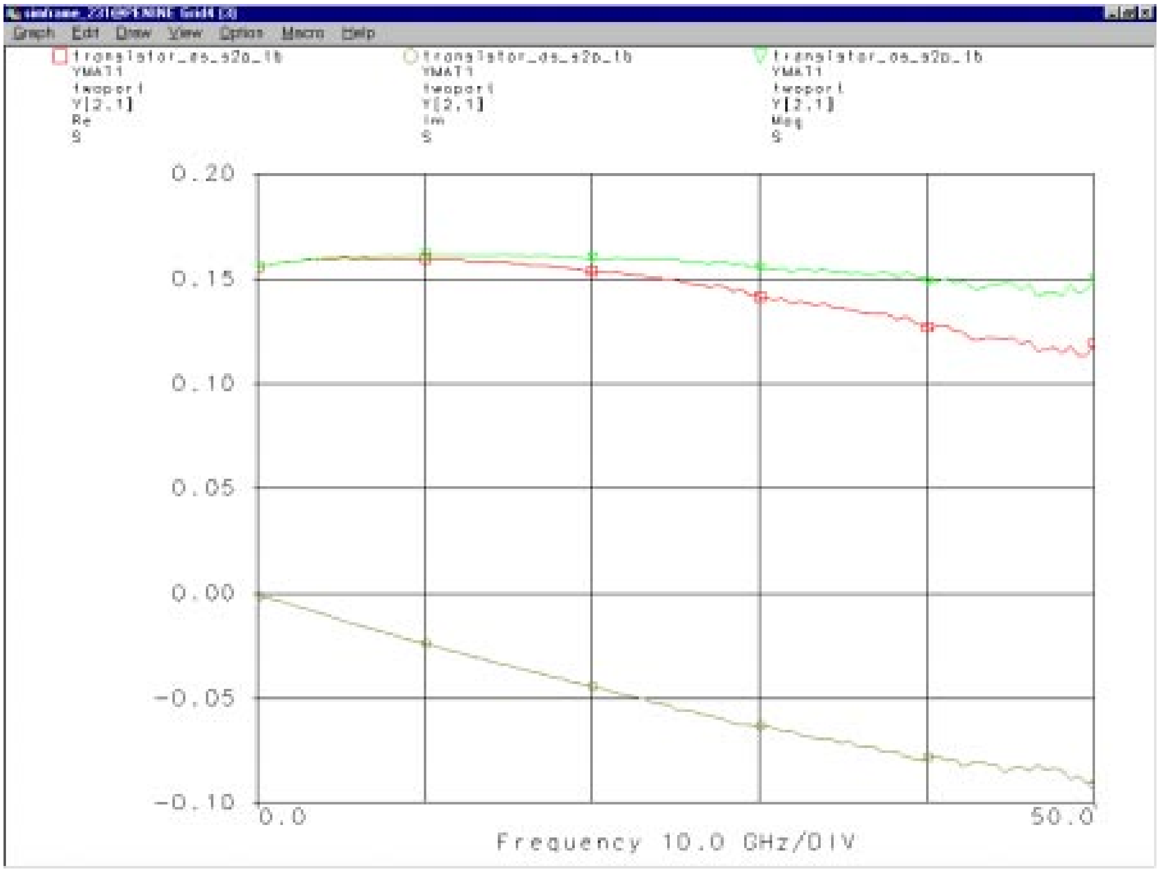
simplifies to

$Y_{21} = (R_{ex} + 1/g_m)^{-1}$ IFF $R_{bb} << \beta(R_{ex} + 1/g_m)$

so, first plot H21 vs. frequency , and determine beta from the low-frequency value.

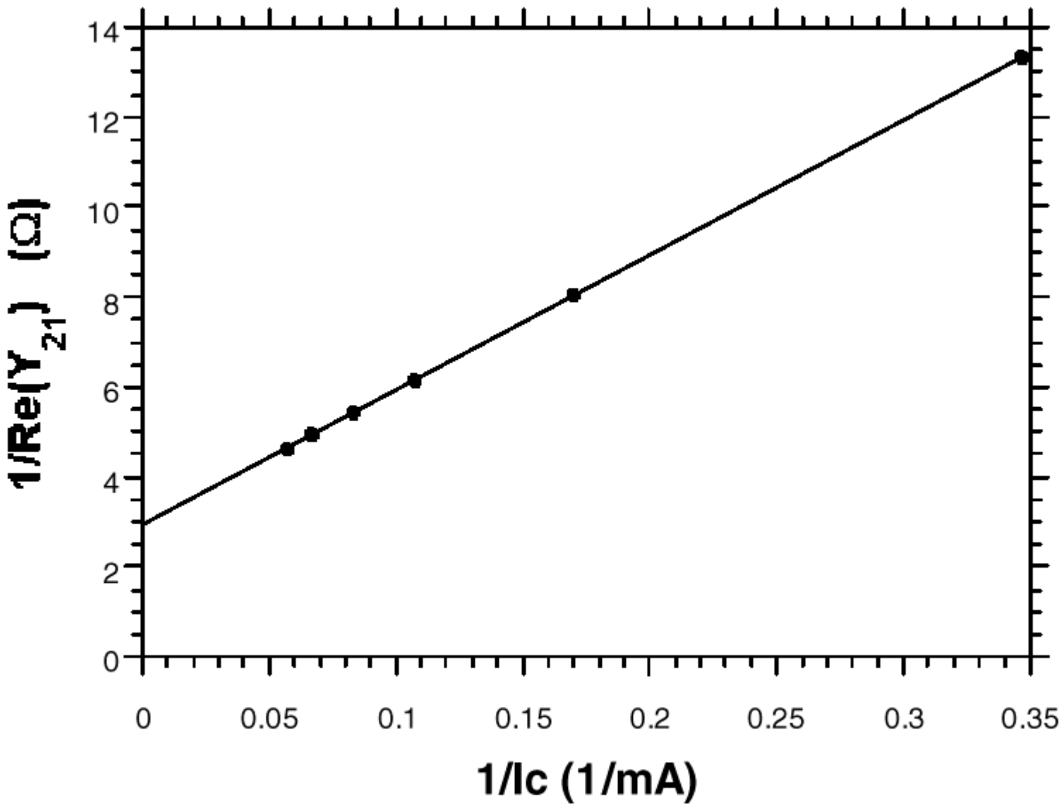


Then, for each data file, plot Y21, and determine the low-frequency value of Y21



…use the value around, say 5 GHz.

Make a plot of Re(Y21) vs. Ic, like so,



And from $(Y_{21})^{-1} = (R_{ex} + R_{bb}/\beta + NkT/qI_E)$, determine N and $R_{ex} + R_{bb}/\beta$.

Since you have found beta, you have found $R_{be} = \beta/g_m$ as well as g_m, and if R_{bb} is not too big, you have a good measure of R_{ex}. When we are really fussy about accuracy, we go through the whole procedure (1-6 below), determine Rbb, and then repeat steps1-6 to determine the parameters again.

<u>Third</u>

Analysis of the network gives $Y_{12} \cong (1/R_{cb} + \omega^2 C_{cbi}^2 R_{bb}) + j\omega(C_{cbx} + C_{cbi})$. Ignoring for now the quadratic term in frequency, which is pretty small, use this relationship to determine $(C_{cbx} + C_{cbi})$ and R_{cb}.

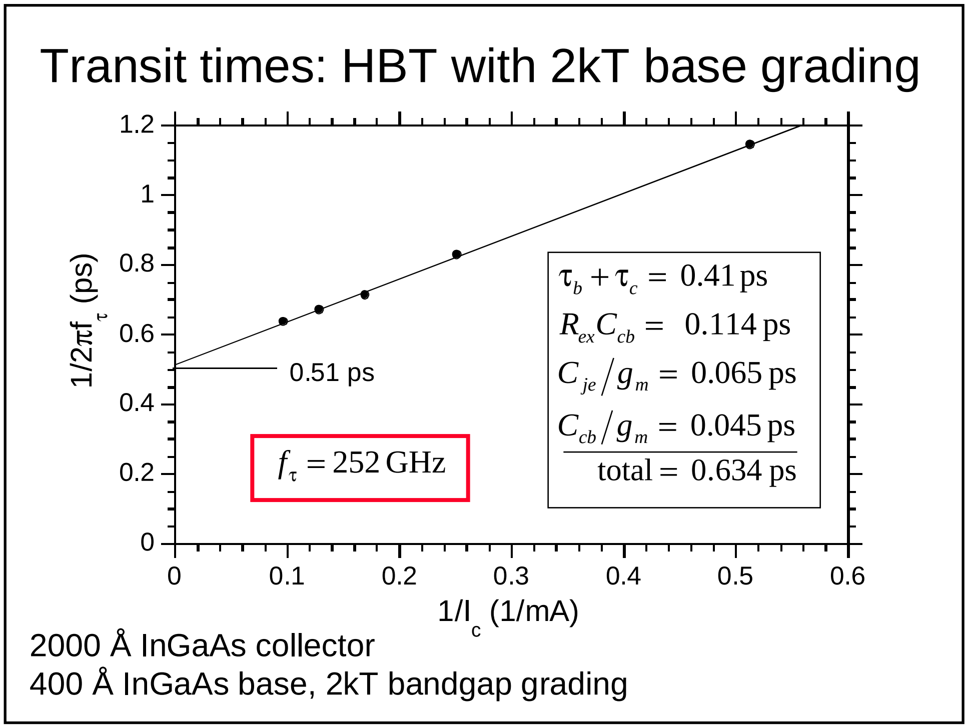
Is it independent of bias current ? Surprisingly, device physics says it should show some variation.

<u>Fourth</u>

We can derive from the device model we are using that (if Rc=0)

$$(1/2\pi f_\tau) = \tau_f + R_{ex}(C_{cb} + C_{poly}) + (NkT/qI_E)(C_{cb} + C_{je} + C_{poly})$$

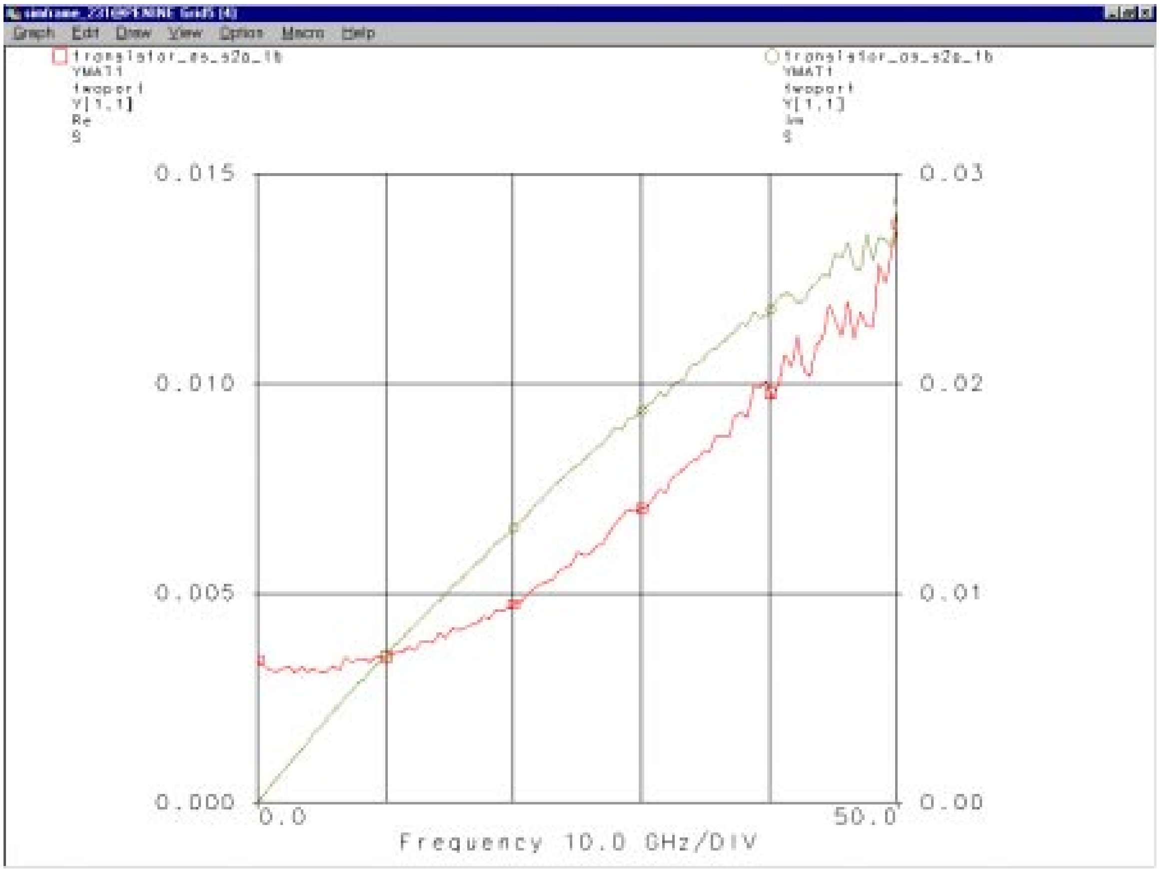
For each bias point, plot H21 vs. frequency, and extrapolate at -20 dB/decade to determine f_τ . Then plot $(1/2\pi f_\tau)$ vs. $(1/I_E)$. The plot will look something like below:



This will allow you to determine $\tau_f + R_{ex}(C_{cb} + C_{poly})$ and $(C_{cb} + C_{je} + C_{poly})$. But, you already know Rex, Ccb, and Cpoly, so you can now determine Cje and tau_f.

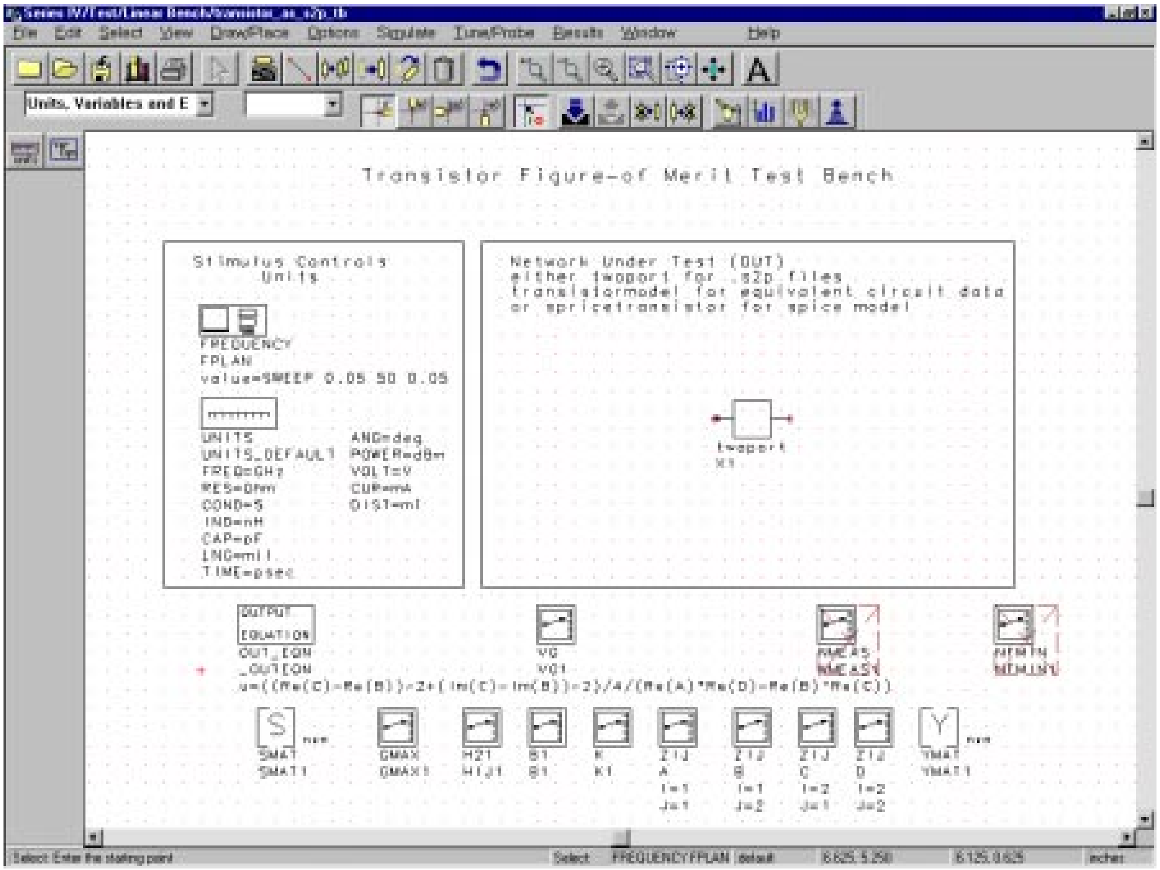
Fifth

We should now determine Rbb . To determine Rbb, we look at Y11.

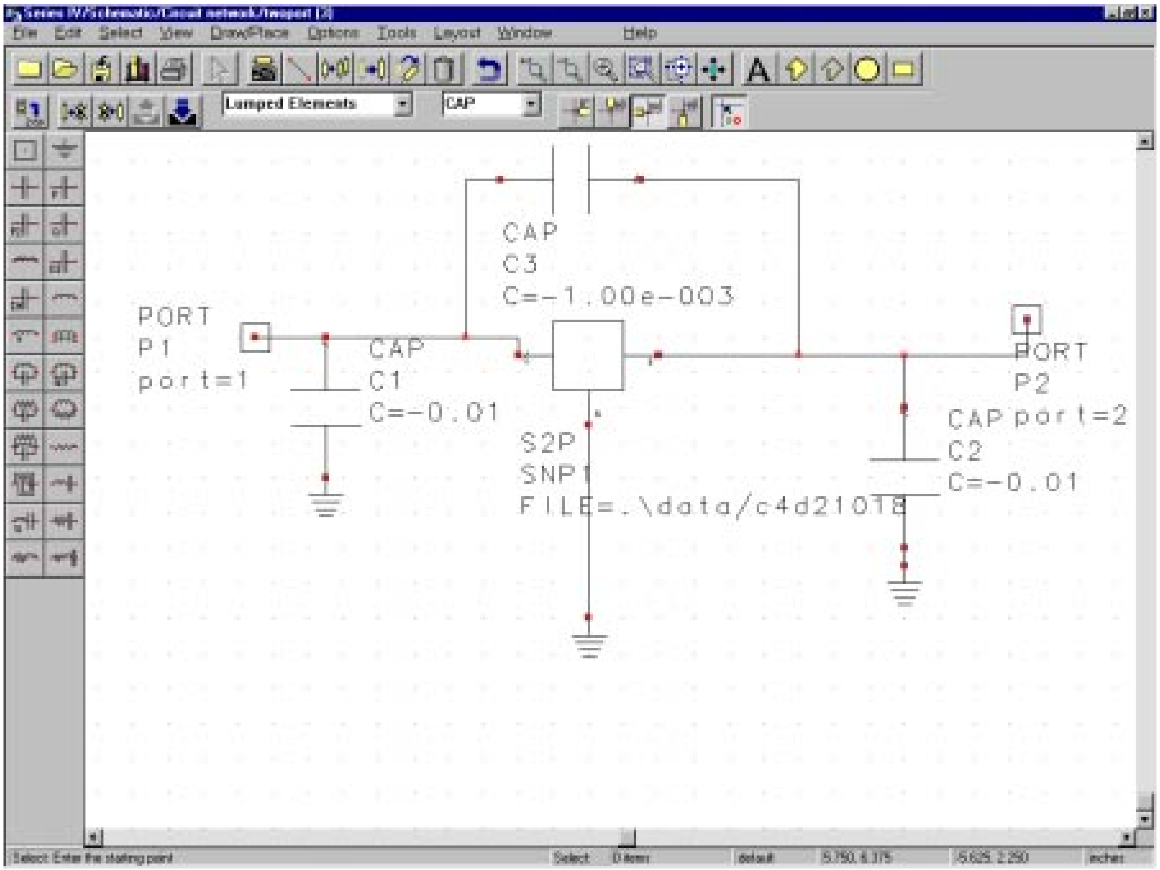


The imaginary part of Y11 is approximately $j\omega(C_{je} + C_{diff} + C_{cb})$. Never mind. The real part of Y11 is approximately $1/R_{be} + \omega^2 (C_{je} + C_{diff})^2 R_{bb}$. We have already obtained all terms in this expression except Rbb, so we can compare Im(Y11) of the data and the equivalent circuit to determine Rbb.

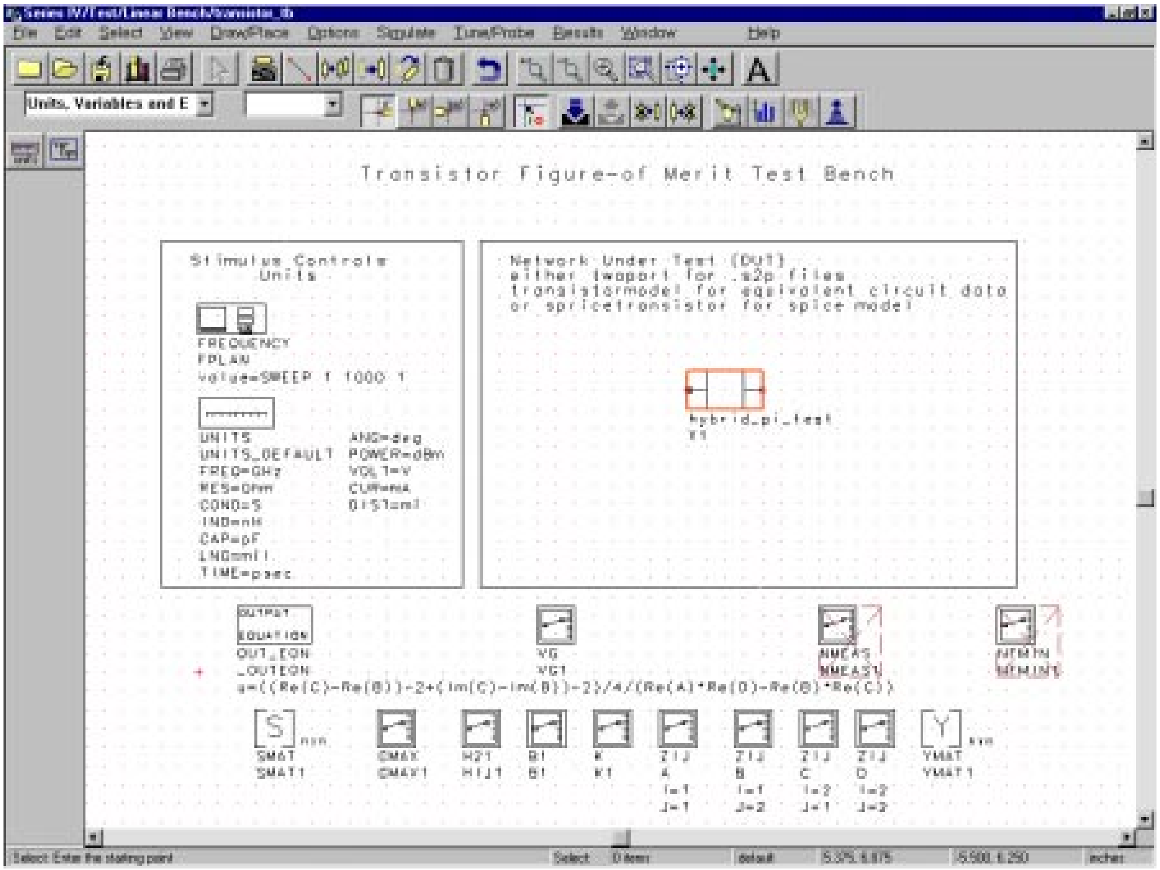
The way we do this is to create 2 test benches, one invoking the .s2p file:



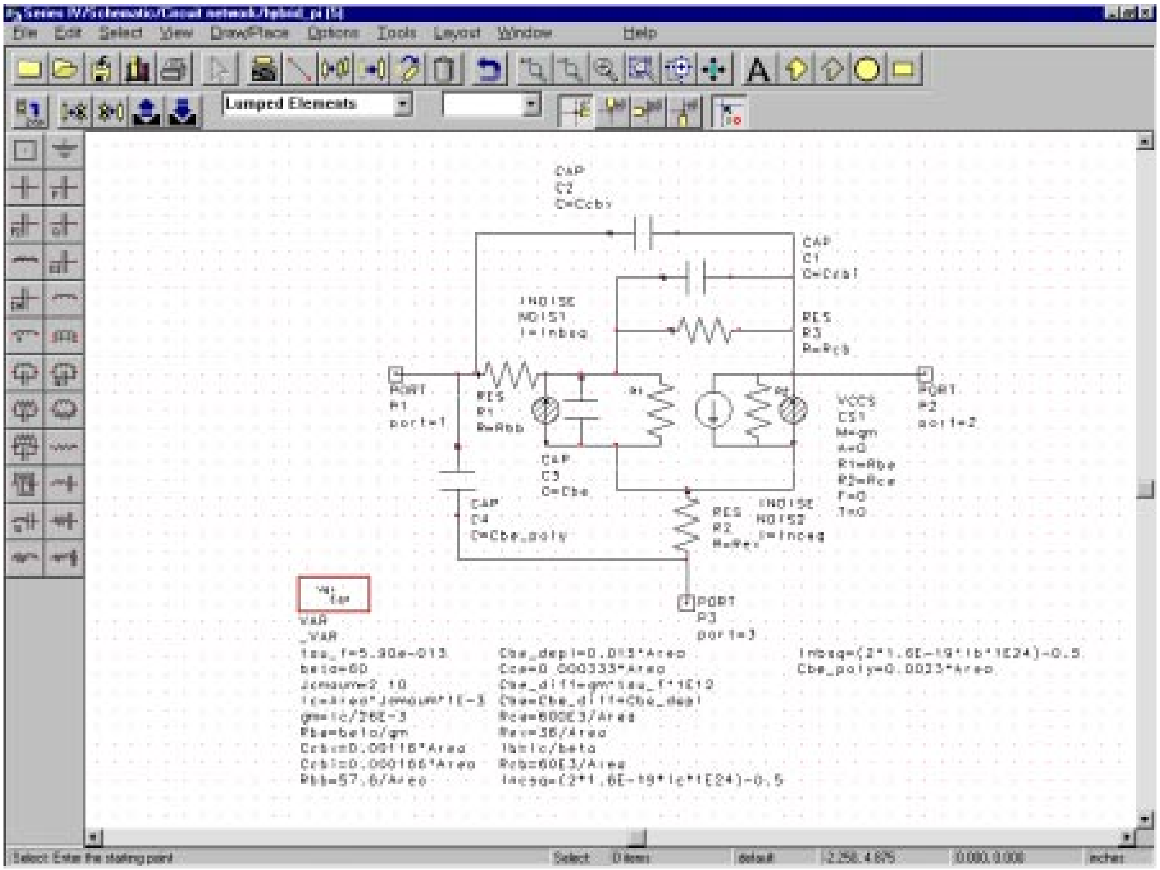
Transistor Figure-of Merit Test Bench
Stimulus Controls
Units
FREQUENCY
FPLAN
value=SWEEP 0.05 50 0.05
UNITS
UNITS_DEFAULT
FREQ=GHz
RES=Ohm
COND=S
IND=nH
CAP=pF
LNG=mil
TIME=psec
ANG=deg
POWER=dBm
VOLT=V
CUR=mA
DIST=mil
Network Under Test (DUT)
either twoport for .s2p files
transistormodel for equivalent circuit data
or spicetransistor for spice model
twoport
X1
OUTPUT
EQUATION
OUT_EQN
_OUTEQN
VG
VG1
SMAT
SMAT1
GMAX
GMAX1
H21
H1J1
B1
K
K1
ZIJ
YMAT
YMAT1



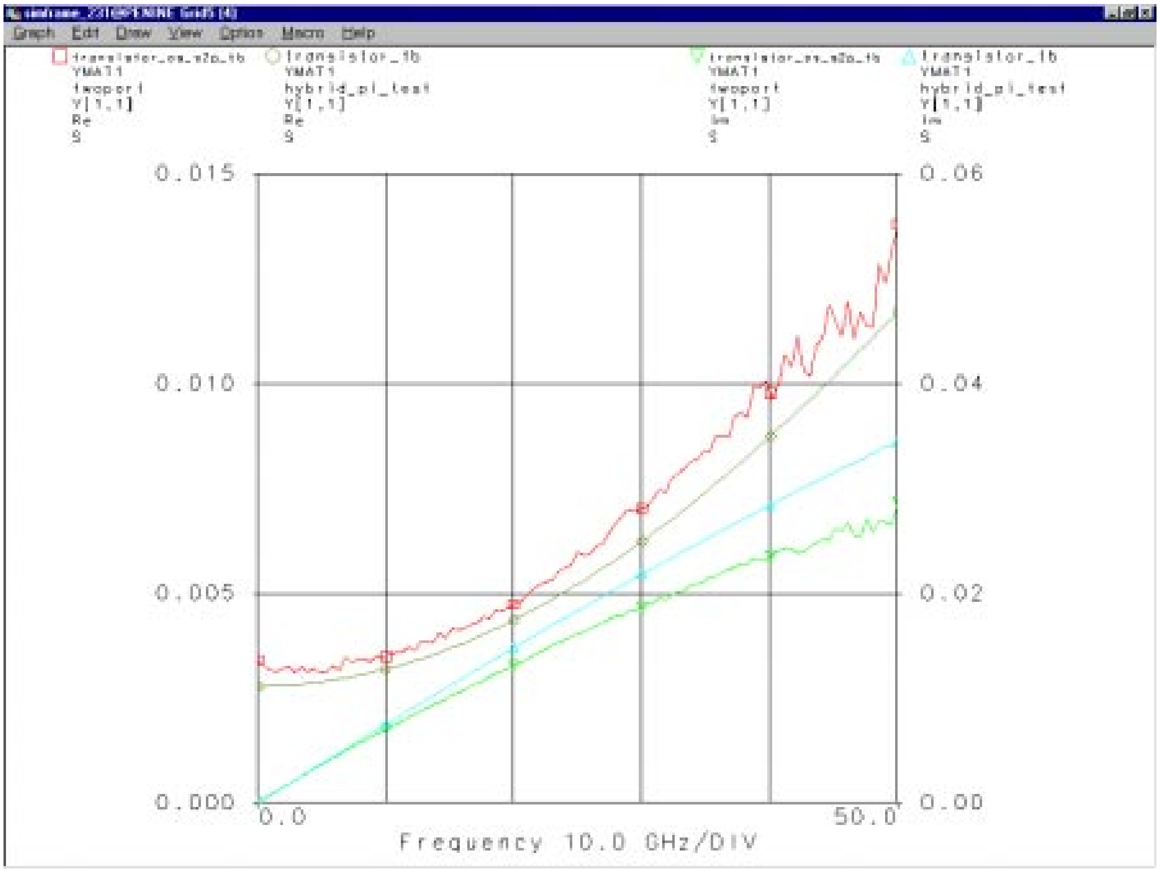
and the other invoking the hybrid-pi model:



File Edit Select View Draw/Place Options Simulate Tune/Probe Results Window Help
Units, Variables and E
Transistor Figure-of Merit Test Bench
Stimulus Controls
Units
FREQUENCY
FPLAN
value=SWEEP 1 1000 1
UNITS
UNITS_DEFAULT
FREQ=GHz
RES=Ohm
COND=S
IND=nH
CAP=pF
LNG=mil
TIME=psec
ANG=deg
POWER=dBm
VOLT=V
CUR=mA
DIST=mil
Network Under Test (DUT)
either twoport for .s2p files
transistormodel for equivalent circuit data
or spicetransistor for spice model
hybrid_pi_test
X1
OUTPUT EQUATION
OUT_EQN
_OUTEQN
VG
VG1
NMEAS
NMEAS1
NFMIN
NFMIN1
SMAT
SMAT1
GMAX
GMAX1
H21
HIJ1
B1
B1
K
K1
ZIJ
A
I=1
J=1
ZIJ
B
I=1
J=2
ZIJ
C
I=2
J=1
ZIJ
D
I=2
J=2
YMAT
YMAT1



We can then plot the Y parameters for the data file and the model on the same plot to compare….



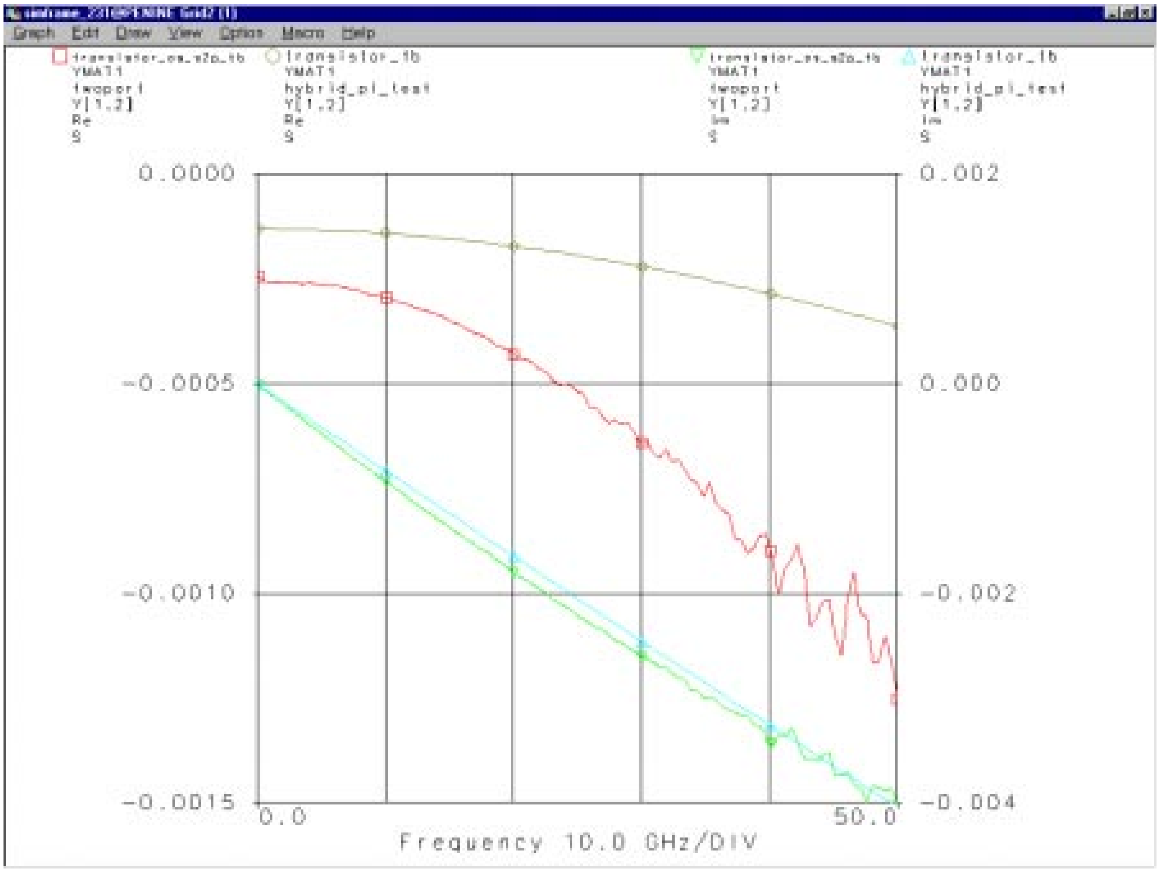
…where, as shown, we still have some work to do to get the model right.

Sixth, and finally

For separate determination of Ccbi and Ccbx….

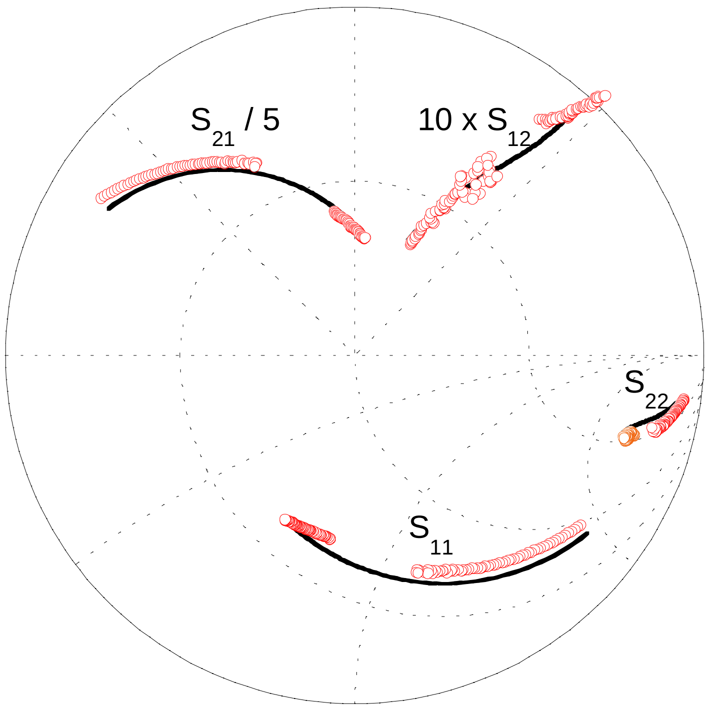
There are 2 methods. Your choice

The first is from the relationship $Y_{12} \cong (1/R_{cb} + \omega^2 C_{cbi}^2 R_{bb}) + j\omega(C_{cbx} + C_{cbi})$. This indicates that there is a quadratic component to the variation in Re(Y12) which can be used to determined Ccbi (all other #s having been determined). Look at the RED curve below. The $\omega^2 C_{cbi}^2 R_{bb}$ term stands out dramatically. We can adjust Ccbi to get this fit correctly, while keeping Ccbx+Ccbi constant.



The other method for fitting Ccbi is simply to plot Mason's Unilateral gain U (defined for you on the test benches above). f_{max} is determined by extrapolating U at -20 dB/decade. We can fit to Ccbi by making the U of the equivalent circuit equal to the U of the measured data files.

If the procedure goes well, the fit can be fantastic:



and the equivalent circuit model's parameters (R's and C's) can and usually do correspond to physically-sensible values ($R = \rho L / A$, $C = \varepsilon A / D$, etc)

A caveat: The Hybrid-Pi model really needs to have associated with it a delay of approximately the collector transit time + about 1/10 the base transit time. Some of the relationships have to be tweaked slightly given this fact. Exercise for the interested reader. We will ignore this in this exercise.

What should I turn in?

-A plot showing your determination of pad capacitances.

-A plot showing your determination of β from H21

-A plot showing your determination of Rex and N

- A plot showing your determination of Ccbx+Ccbi and Rcb

- A plot of the relationship $(1/2\pi f_{\tau}) = \tau_f + R_{ex}(C_{cb} + C_{poly}) + (NkT/qI_E)(C_{cb} + C_{je} + C_{poly})$ and your resulting determination of device parameters

- A plot showing your determination of Rbb

- A plot showing your determination of Ccbi

- 2 plots comparing the 4 S-parameters, model vs. data, for 3 and for 18.47 mA bias current.

- A plot comparing H21, MAG, and U of the model and the data at 18.47 mA bias current