ECE202A Problem set #5

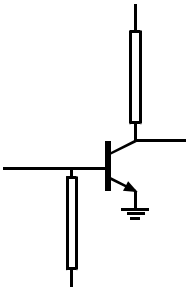
This is a somewhat simpler and easier assignment than we had originally planned; I think we all agree that the class has been plenty of work !

We will design a Tuned microwave amplifier using the small-signal model of Michelle Lee's best high-frequency HBT.

Assignment

Your objective is to design a narrowband reactively-tuned amplifier with this transistor. You many design either a single-stage or multistage circuit. You may design in common-base or common-emitter, or a mix. Your choice. The design frequency should be 200 GHz.

You must include the bias networks in your design, simulation, and layout…



The submitted design should consist of a circuit diagram, a hand drawing (sketch) of the physical layout, and simulations of circuit performance. The circuit design should use electrical models of *real* transmission lines, not idealized zero-loss ones. Please make a short report documenting key design decisions, with intermediate simulation results, etc.

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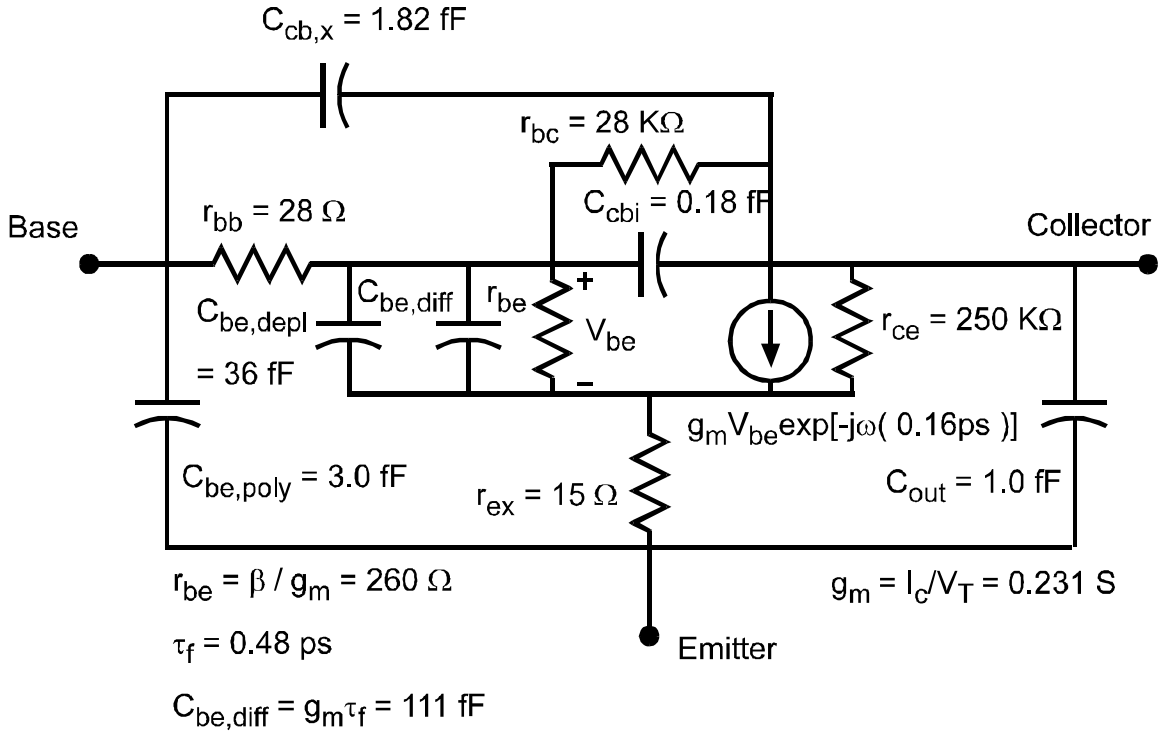
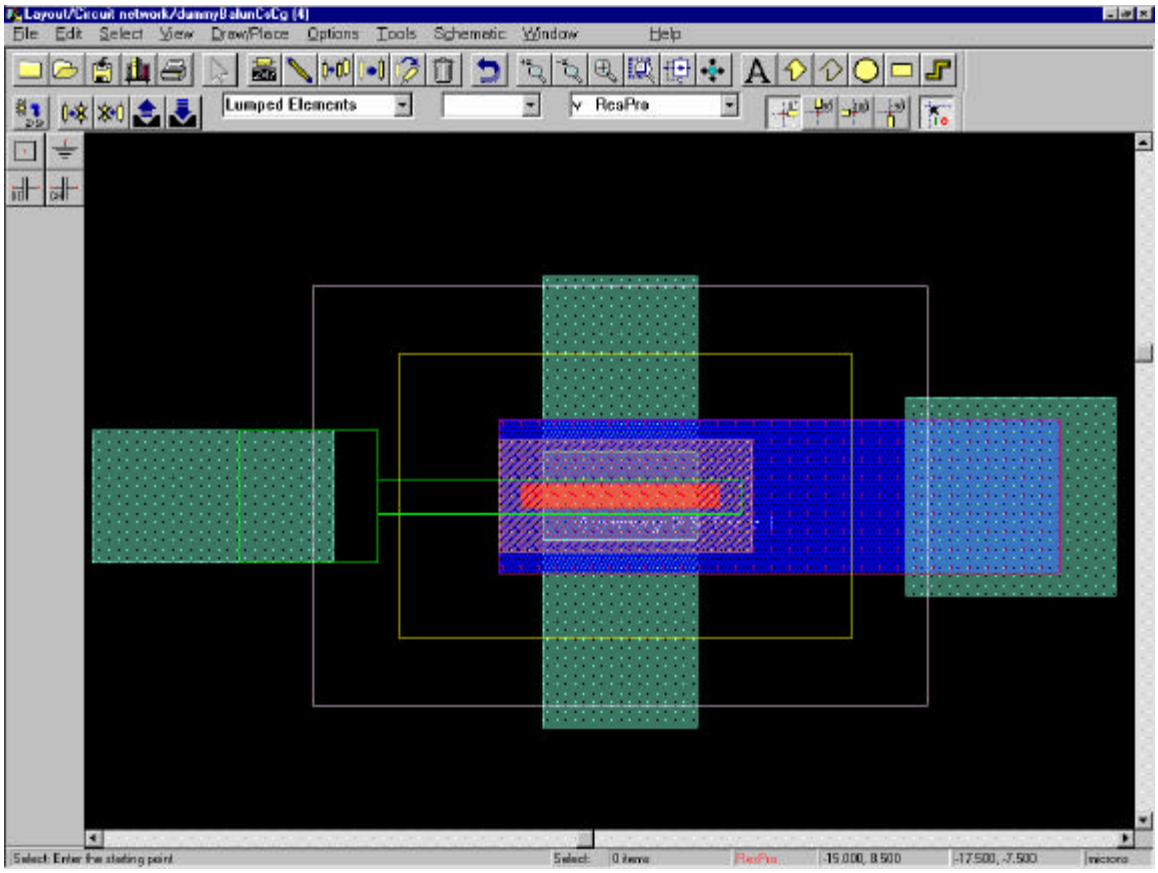
Technology description:

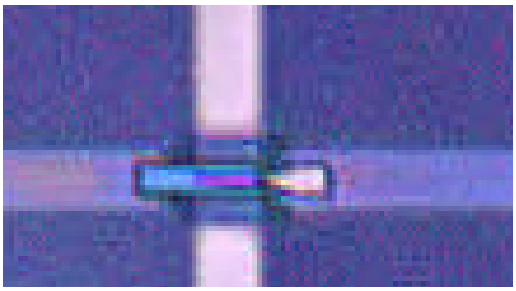
The transistor has the model below. When biased at Ie=6 mA and Vce=1.2 Volts (Vbe=0.7 Volts, and the base current is the emitter current divided by beta, where beta is about 20-30)), the device is modeled by the equivalent circuit below.



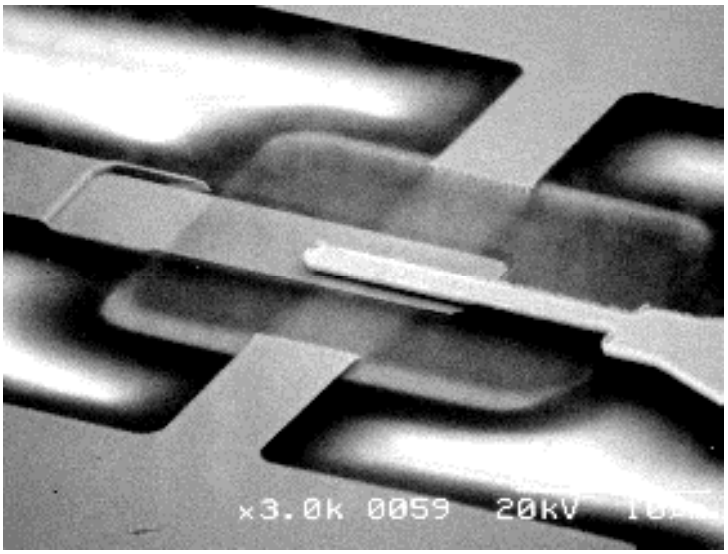
I couldn't find the real mask layout for this device. As a substitute, use the device layout below. For scale reference, the red stripe is the emitter stripe and is one by 9 microns dimensions (Michelle's real HBT had a 0.4 x 6 um emitter and a 0.7 x 8 um collector) The dark green is wiring; on the left is the conductor contacting the collector, on the right is the conductor contacting the base, and the central green stripe passing under the transistor is the emitter contact; you can connect to it from one side, the other side, or both.



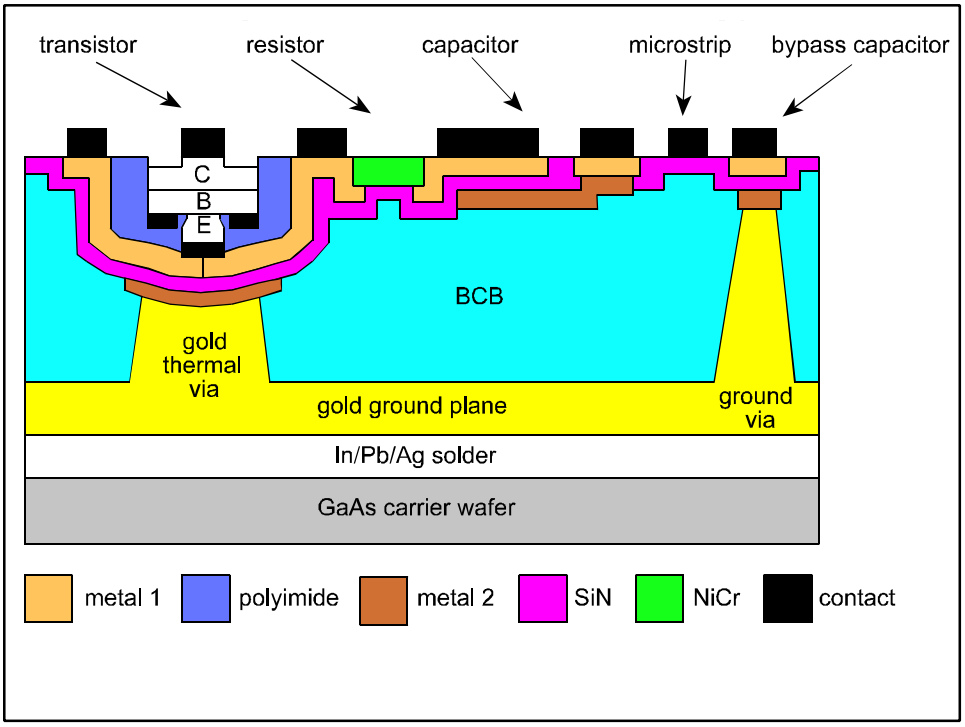
Here is a (rather blurry) photo of the actual transistor…the collector contact in this case is on the right.



…and here is a photo of another device…again with the collector on the right, the base on the left, and the emitter contacted by the wire which runs under the transistor.



You need to know something about the wiring environment. A cross-section is as below:



The key point is that there is a ***ground plane***. There are 2 planes of wiring metal, labeled *metal 1* and *metal2*. Between these and the ground plane there is a 5 micron thick layer of BCB, which is a dielectric with ε_r of 2.7.

Microstrip lines, thus, are Au conductors of 0.5 micron thickness, on a substrate of 5 um thickness with ε_r of 2.7. You can use LINECALC to determine Zo, velocity, and attenuation, alpha, as a function of geometry. Microstrip lines can be in metal 1 or 2; you just have 2 layers you can draw.

Resistors, are squares of NiCr metal. The resistance is 50 Ohms/square times the ratio of length to width of the resistor. You can use idealized resistor models.

Capacitors, are between metal 1 and 2. The Dielectric is Si3N4. It has ε_r of (about) 7 and is 0.5 micron thick. From this you can calculate the capacitance per unit area. In your circuit design, if you use capacitors, you must use the EESOF MTFC (microwave thin film capacitor) model, not that of an ideal capacitor. Real capacitors have layout inductance, and MTFC models this.

Vias, are necessary to electrically access the ground plane. Just draw a square.

Transistors: you have the model above, and a picture for sketching its layout. If you want to ground the emitter, the grounding via can be directly under the transistor.

Design Procedure

How much gain can you get

First, plot the transistor Unilateral gain (for fun) and the Maximum Available Gain (MAG) and Maximum stable gain (MSG). If you invoke MAG (or is it Gmax) in EESOF, it defaults to plotting the MAG when the device is unconditionally stable, and at other frequencies plots the maximum stable gains. Plot the stability factor K vs. frequency.

Examine the MAG/MSG in common-emitter and common-base before deciding which to use.

Stopping it from oscillating: .

It will be necessary to add some (shunt or series, input or output) resistive loss to stabilize the two-port before designing the matching networks. You must make sure that the amplifier is unconditionally stable at all frequencies, not just the frequencies you care about. An effective way of doing this is as follows: (1) add sufficient resistive loss to stabilize the HBT at the design frequency, but not a lot more. You must slightly over stabilize in order to make the input and output impedance matching feasible. This will fail to stabilize the device at lower frequencies. (2) then add a second resistor to stabilize the HBT at lower frequencies. This resistor can be effectively removed from the circuit at the signal frequency by decoupling it through an LC resonator, a quarter-wave line, etc.

Use of the stability circles are very helpful in determining the stabilization strategy.

Designing the input and output matching networks

Examining the Ga and Gp circles *of the stabilized transistor* will tell you the required input and output impedance-matching conditions. You must synthesize these impedance using the available devices: microstrip lines and MIM capacitors. They have some significant attenuation, and this must be modeled.

Make sure your matching networks do not short out your DC bias. Make sure you simulate your DC biasing elements in the RF simulations.

Tweaking the design

If you have impedance-matched at 200 GHz, you will generally find this is not the frequency of peak gain (why ?). It is common practice to isolate the second stabilization resistor with a frequency-dependent isolation network (an inductor…) such that the resulting MAG after stabilization is relatively flat at the design frequency. The gain-frequency curve (S21) of the resulting matched circuit then should show a gain peak at the design frequency. You can do this if you like.

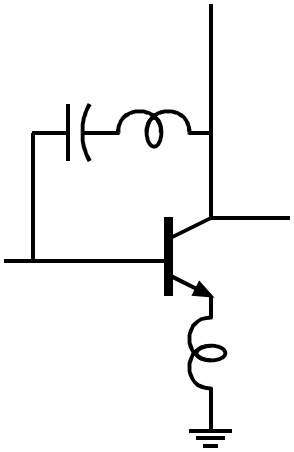
Sketch a layout

Based upon the physical description of the IC process above, draw a scaled drawing of your design, with all transmission-line and capacitor (etc) lengths and widths indicated.

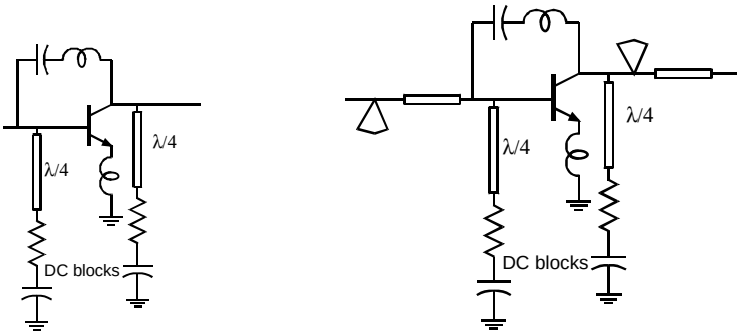
Optional If you want to be really clever

Two thoughts. First, you will find that the microstrip line losses really hurt. If you want to consider using microstrip lines with Au conductors, a substrate thickness of 50 microns, and an epsilon of 1.0 (air) please do so . We are trying to develop such "air microstrip" lines. Their loss is not zero…you must still model then as TLINP elements in EESOF.

The second thought. Michelle's transistor has a much higher Unilateral gain than the maximum available / maximum stable gain. You can get the Unilateral gain if you first unilateralize the device at the design frequency, like so:



The 2 inductors are adjusted until the real and imaginary parts of Y12 are both zero. The capacitor is just to prevent DC shorting the bias. Unilateralizing the device at the 200 GHz design frequency will likely make the device very unstable at other frequencies, and very aggressive out of band stabilization is then required. Something like this might work…



…where the lines are designed to isolate the stabilization resistors at the 200 GHz design frequency. You then impedance-match on input and output, as the final drawing suggests.