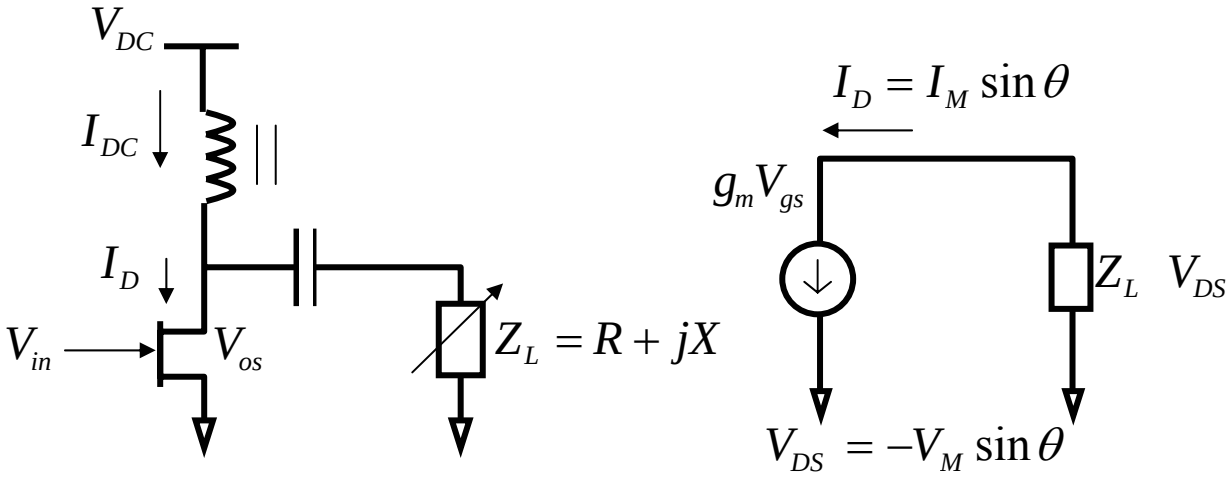
Power Amplifier Design 2

Power Amplifiers; part 2

1. PA impedance matching - large signal
   a. Load pull contours
   b. Package parasitics
   c. Large signal input match
2. PA bias circuits: design for stability

How does mismatch affect output power?

"Load Pull"



Let $Z_L = R_{opt} = \dfrac{V_{DC}}{I_{MAX}/2} = \dfrac{V_{DC}}{I_{DC}}$.

This is the optimum power match (neglecting knee voltage).

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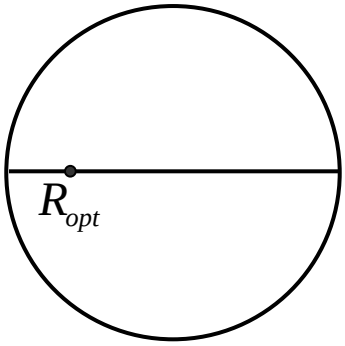
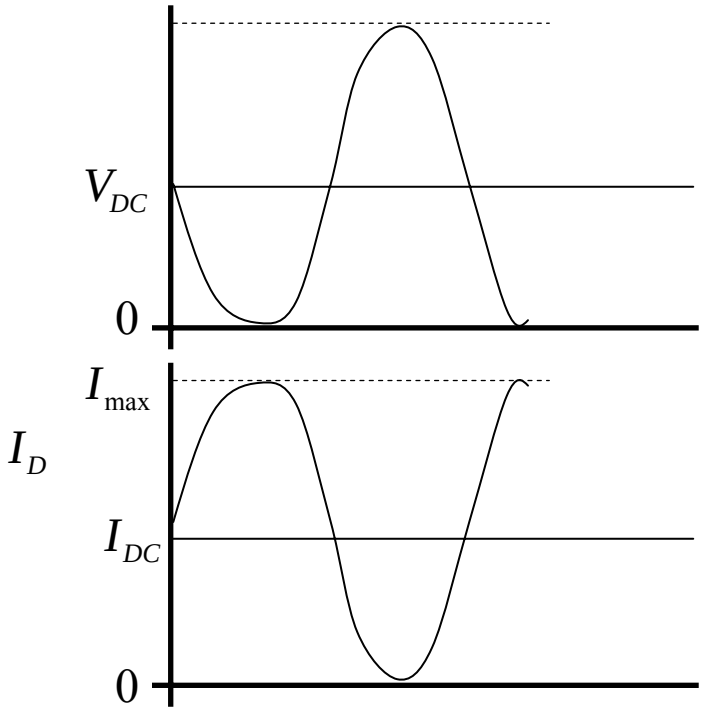


$$P_{opt} = \frac{V_{DC} I_{DC}}{2}$$

$$= \frac{V_{DC}{}^2}{2R_{opt}} = \frac{1}{2} I_{DC}^2 R_{opt}$$



Full voltage and current swing. (neglecting V_{knee})

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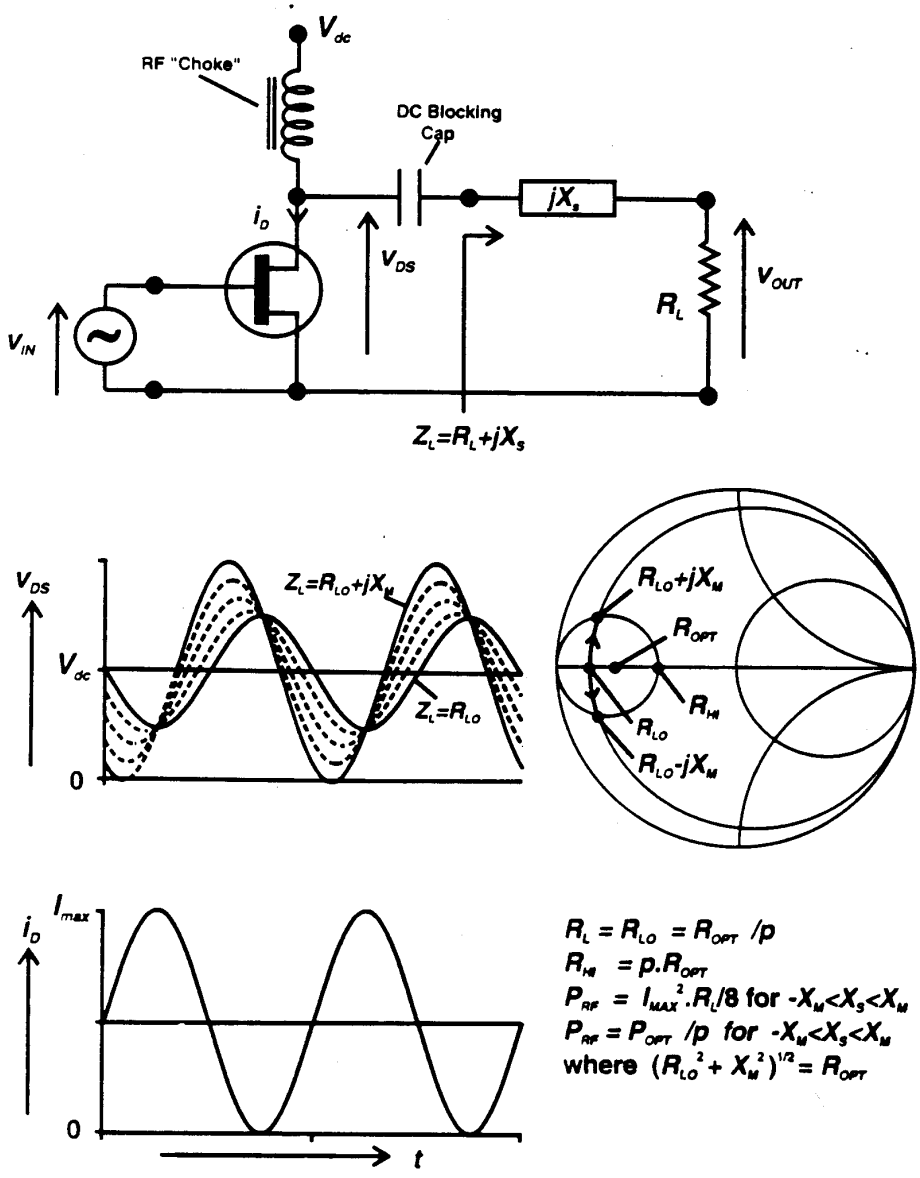

gure 2.10 Class A linear amplifier case 2: output load resistive component lower than R_{OPT}. For $R_L = R_{OPT}/p$, RF power output is P_{OPT}/p, over a range of series reactance $-X_M < 0 < X_M$.

Ref. S. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 1999.

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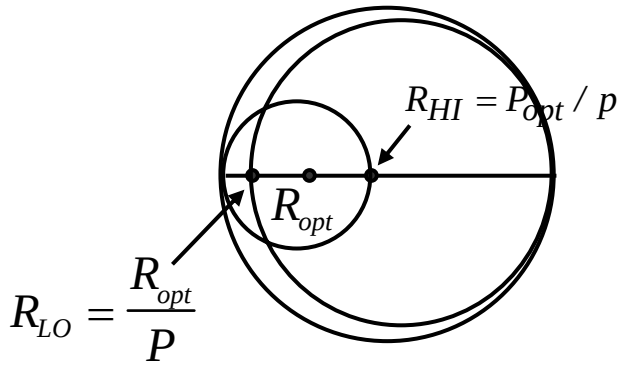
To determine the influence of a mismatched load on the power amplifier output power and also efficiency, we must trace out a contour on the Smith Chart that will give a power of P_{opt} / p. Here, p is the power reduction factor.

There are two solutions.

Resistive Terminations

1) pR_{OPT} $\begin{cases} I_m = \dfrac{V_{DC}}{pR_{opt}} \\ V_m = V_{DC} \end{cases}$ $\quad P_o = \dfrac{1}{2}\dfrac{V_{DC}^2}{pR_{opt}} = \dfrac{P_{opt}}{p}$

2) R_{opt}/p $\begin{cases} I_m = I_{max}/2 = I_{DC} \\ V_m = I_{DC}R_{opt}/p \end{cases}$ $\quad P_0 = \dfrac{1}{2}\dfrac{I_{DC}^2 R_{opt}}{p} = \dfrac{P_{opt}}{p}$



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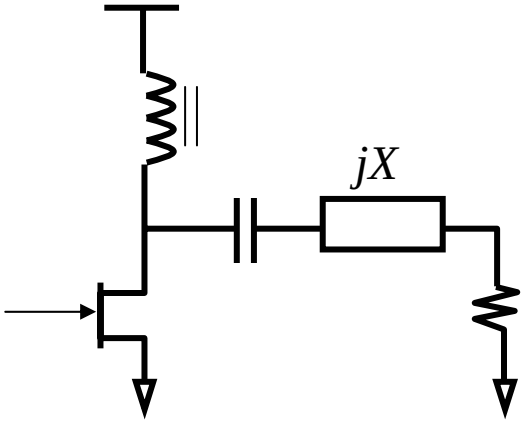
Series reactance; When $R = \frac{R_{opt}}{p} = R_{LO}$, add jX.

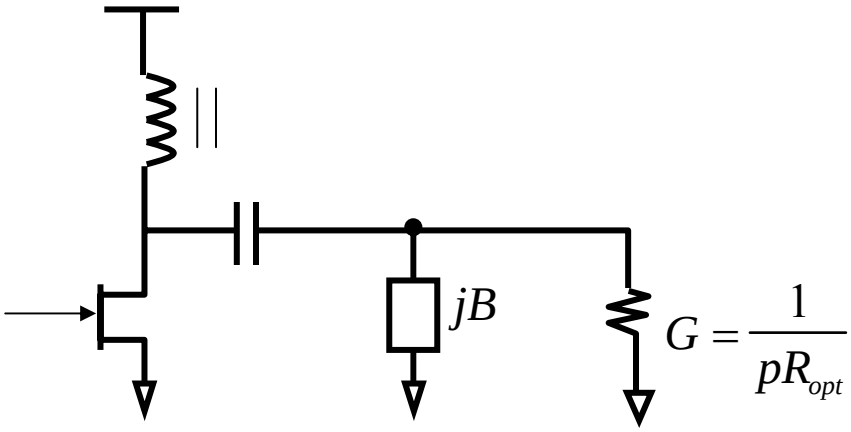


$R_{opt} / p = R_{LO}$ $\quad |V_M| = I_{DC}|R_{LO} + jX|$

in this limit when $R = R_{LO}$, we have power limited by I_{MAX}. Voltage $V_m < V_{DC}$. So, series reactance will increase the voltage swing but not affect current.

This is valid up to $\pm X_m$, where $|R_{LO} + jX_m| = R_{opt}$

Shunt susceptance; When $R = pR_{opt} = R_{HI}$, add jB



at this limit, power is limited by the voltage swing, $V_m = V_{DC}$. $I_D < I_{MAX}$.

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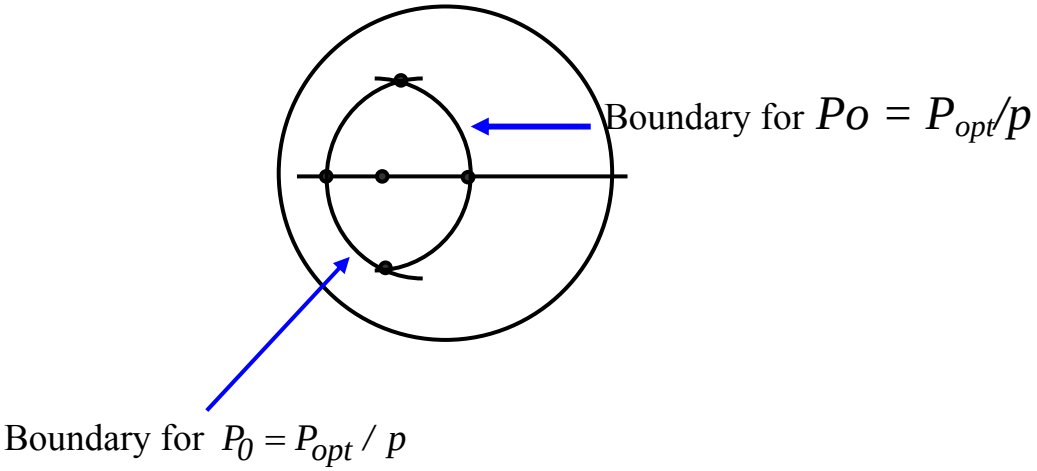
Shunt susceptance can be added. It will cause current to increase until

$$|G + jB_m| = \left|\frac{1}{R_{opt}}\right|$$

These are called Load Pull Contours, and they follow constant *r* or *g* circles on Smith Chart. It can be shown that the intersection of these circles represents X_m or B_m.



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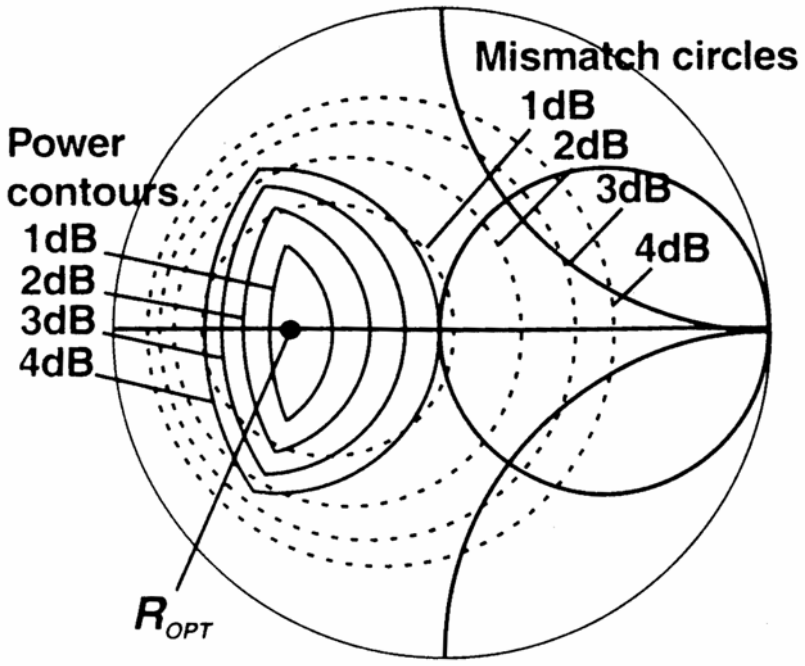

Figure 2.13 Power-match contours (solid, 1 dB to 4 dB contours shown) compared with gain mismatch circles (dotted) based on a source impedance equal to the optimum power match ($R_{OPT} = 20\Omega$).

Ref. S. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 1999.

The load pull contour takes the place of gain circles for power amplifier designs.

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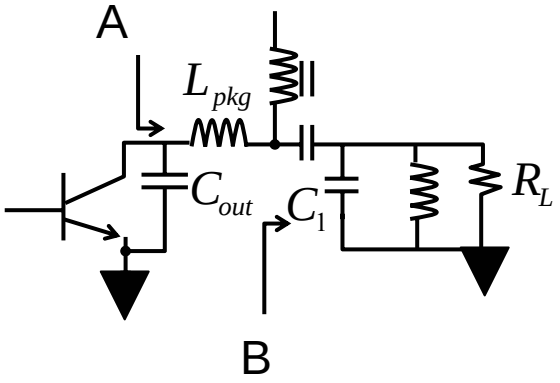
At higher frequencies, device capacitances and package capacitance and inductance can be significant.



Utilize C_{OUT} as part of matching network-

- a pi-section can accomplish this if C_{OUT} and L_{pkg} is not extremely large.
- Smith chart or design equations can be used to design network. $Q \leq 5$ is reasonable for narrowband design.
- Note that we must provide the load line match at plane A, not plane B.

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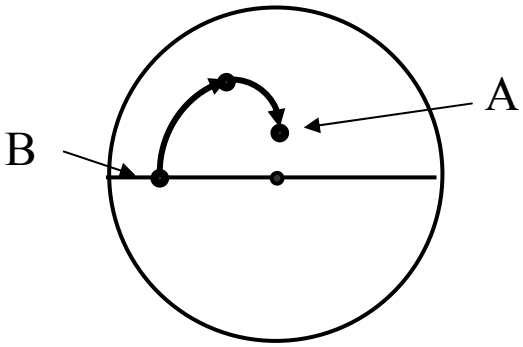
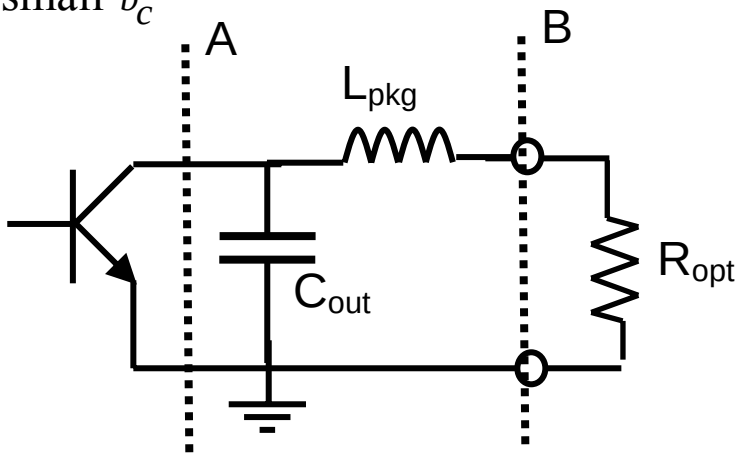
What does the package do to Z_L?



large x_L, small b_C



We require that ZA = Ropt, so there is a problem – the output capacitance and the package will transform Ropt into something else. So, Ropt must be compensated to account for the package.

Power Amplifier Design 2

Input Matching

For PAs, we often have large voltage or current variations on input. This can lead to large input impedance variation with drive power, P_{IN}.

So, what procedure can be used to design input network?

For Class A, we never cutoff or swing into knee region of device *I-V*.

- 1st approximation: use small signal S parameter calculation to find Γ_{IN} at quiescent bias.

- Conjugately match the input.

- If gain is adequate, stop. Otherwise, you may need to optimize Γ_S experimentally in simulation. (source pull)

Power Amplifier Design 2

Simulation methods for power amps[1]

At small signal levels, most linear power amps will behave like a small signal amplifier. S parameter simulation may be useful as a starting point for estimating input impedance.

BUT, power amps always become nonlinear at some input drive level. Clipping, compression, and distortion are inevitable. Thus, we need to use a nonlinear simulator to predict these effects. Agilent ADS gives us two options:

- Harmonic Balance, a frequency domain method
- Transient Analysis, a time domain method

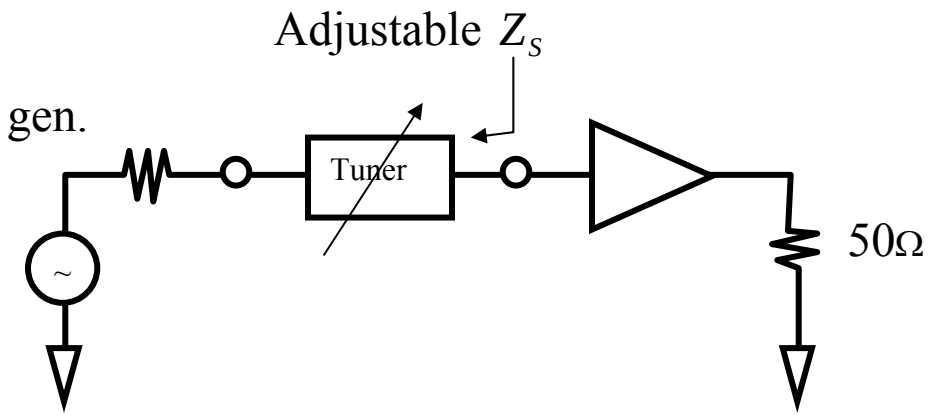
Since we are designing the amplifier mainly in the frequency domain, HB makes the most sense and is usually more efficient in simulation time (when it converges properly).

Using HB with parameter sweeps, you can determine key performance measures such as:

- Gain vs. P_{IN}
- Efficiency vs. P_{IN}
- Output power vs. P_{IN}
- Distortion

[1] Read the ADS Harmonic Balance Tutorial on the course web page. There will also be sample simulation files that can be downloaded and modified.

Power Amplifier Design 2



Experimental approach: measure Z_S for best gain. Design *MN* accordingly.

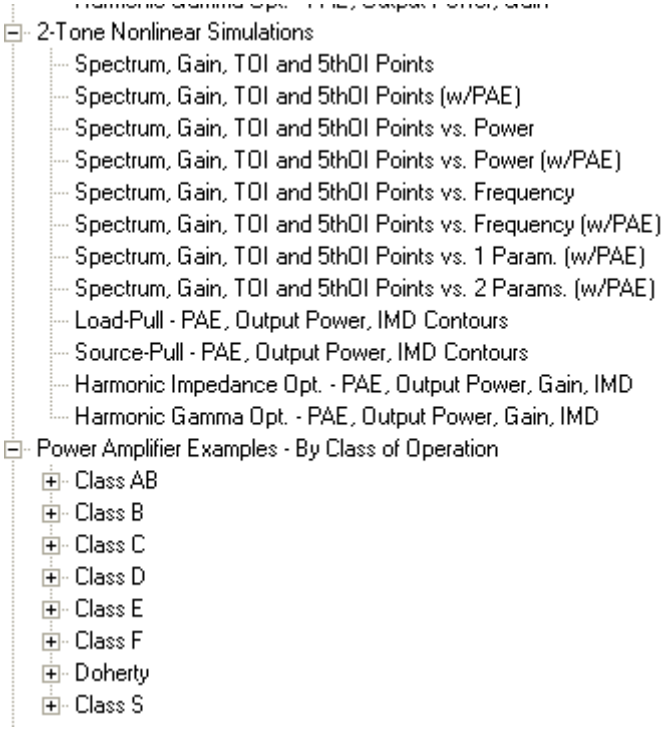
Simulation approach: Use amplifier design guide found in the design guide menu on ADS. There are extensive simulation panels that can be adapted to your design that will evaluate:

- Power vs frequency
- Output spectrum
- Gain, efficiency vs power
- 2 tone distortion measurement
- Source and load pull simulations

Power Amplifier Design 2

- S-Parameter Simulations
  - S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay
  - Feedback Network Optimization to Attain Stability
  - S-Params, Gain, NF, Stability, Group Delay vs. Swept Parameters
  - S-Params., Stability, and Group Delay vs. Frequency and Input Power
- 1-Tone Nonlinear Simulations
  - Spectrum, Gain, Harmonic Distortion
  - Spectrum, Gain, Harmonic Distortion (w/PAE)
  - Spectrum, Gain, Harmonic Distortion vs. Power
  - Spectrum, Gain, Harmonic Distortion vs. Power (w/PAE)
  - Spectrum, Gain, Harmonic Distortion vs. Frequency
  - Spectrum, Gain, Harmonic Distortion vs. Frequency (w/PAE)
  - Spectrum, Gain, Harmonic Distortion vs. Frequency & Power
  - Spectrum, Gain, Harmonic Distortion vs. Frequency & Power (w/PAE)
  - Spectrum, Gain, Harmonic Distortion at X dB Gain Compression
  - Spectrum, Gain, Harmonic Distortion at X dB Gain Compression vs. Freq.
  - Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 1 Param.
  - Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 2 Params.
  - Noise Figure, Spectrum, Gain, Harmonic Distortion
  - Large-Signal Load Impedance Mapping
  - Load-Pull - PAE, Output Power Contours
  - Load-Pull - PAE, Output Power Contours at X dB Gain Compression
  - Source-Pull - PAE, Output Power Contours
  - Harmonic Impedance Opt. - PAE, Output Power, Gain
  - Harmonic Gamma Opt. - PAE, Output Power, Gain

Power Amplifier Design 2



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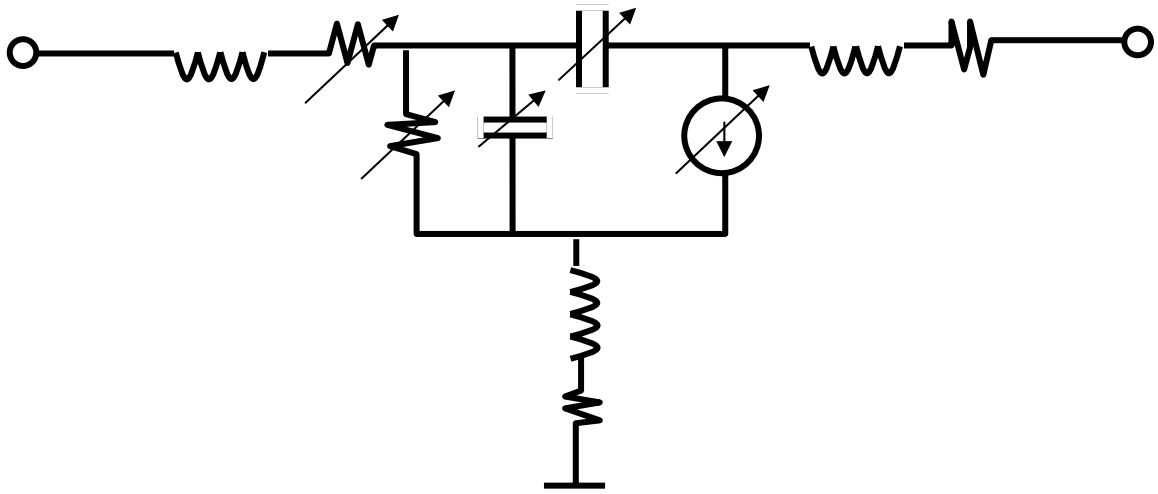
Power amp bias circuits.

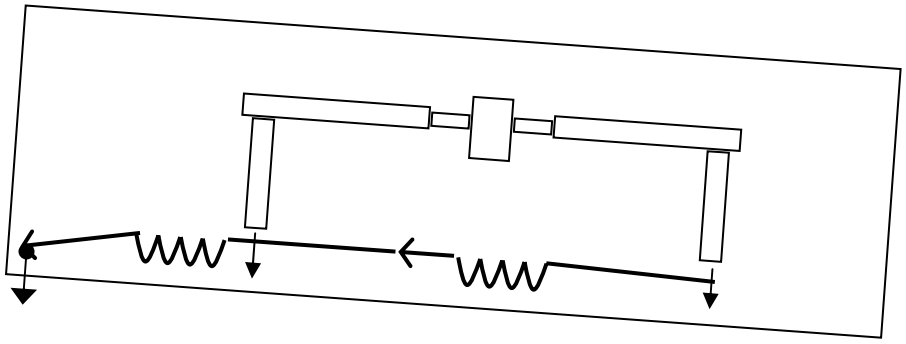
Power amps may often be harder to stabilize than small signal amps.

- large voltage swing causes capacitance and *gm* variation with time. Your SS stability predictors are not necessarily accurate.
- common mode feedback is more serious. Power amps have higher ground, I_{DC} currents.

Nonlinear device model:



Layout on circuit board. Ground connection may have a lot of inductance.



Power Amplifier Design 2

* Impedance levels are often lower – much lower. Need better bypassing, isolation.

* Need to provide proper termination impedances at all frequencies. *MN* only good in-band.

* High current transients are beyond what DC regulated supply can provide. Inadequate bypassing produces "memory effects", long time constant transients in amplitude which will add to distortion.

* Therefore, you need to bypass for both LF and HF

RF Chokes are frequently used at lower frequencies to provide isolation between the DC power system and the amplifier (<1Ghz). $\frac{\lambda}{4}$ lines are useful at higher frequencies for the same function.

Rule: $|Z_{choke}| >> |Z_L|$

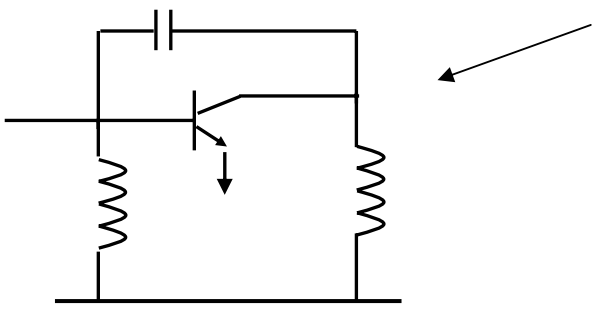
Why? Don't want to lose power into your DC feed system.

Power Amplifier Design 2

Potential problems:
1. Typically large Z_{choke} is in conflict with the requirements of amplitude modulation;
the envelope of the RF signal varies greatly at modulation frequencies up to several MHz for wideband digital signals. This requires small Z_{choke}.

2. Stability.

Oscillation: If no series *R* in the bias network, the device feedback capacitance and bias inductances can cause negative resistances.



Pi network: 180° phase shift at some frequency

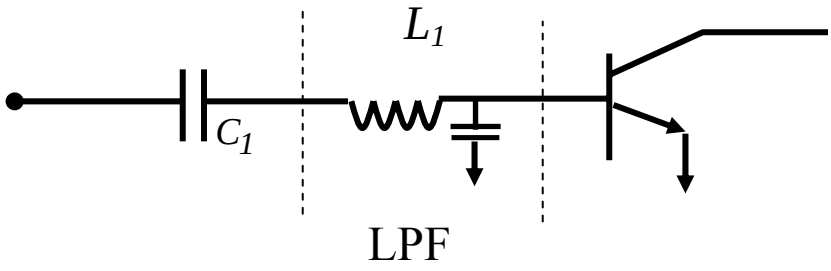
=> Hartley Oscillator

Need good damping at low frequency to keep loop gain < 1. This must be done with care so that you do not throw away gain or efficiency unnecessarily.

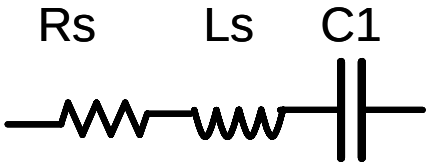
Power Amplifier Design 2

Coupling Caps.

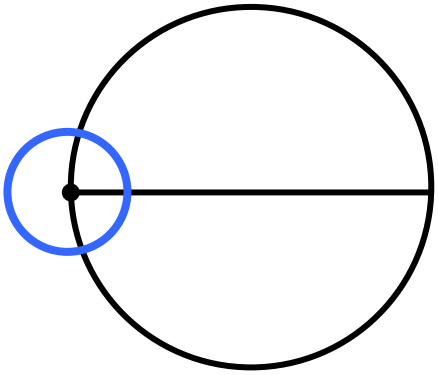
Want to kill low frequency gain if *MN* is *lowpass* type.



Choose C_1 to be no larger than needed for self series res.



Choose $\omega_0 = \frac{1}{\sqrt{L_S C_1}}$ where ω_0 = design frequency.



This disconnects the RF matching network from the bias network at low frequencies where the oscillation problem is greatest.

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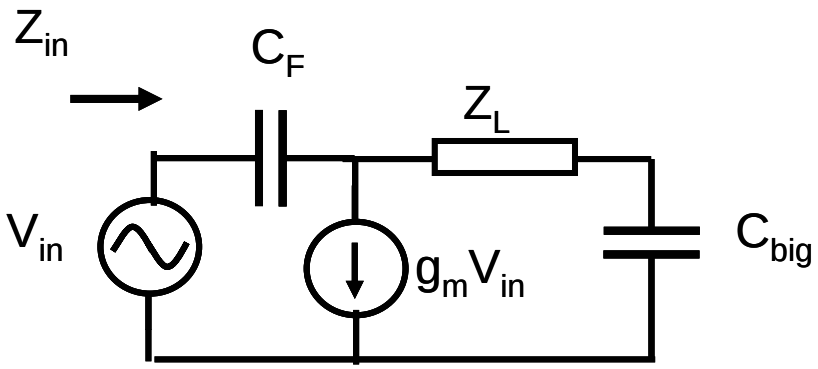
Stability

The remaining circuit for low frequency stability analysis consists of the biasing networks and the device.



Z_L represents the bias feed inductance, parasitic inductance of bypass capacitors, and ESR of capacitors.
C_F is the feedback capacitance, Cgd.

Find values of Z_L that produce negative real Zin.

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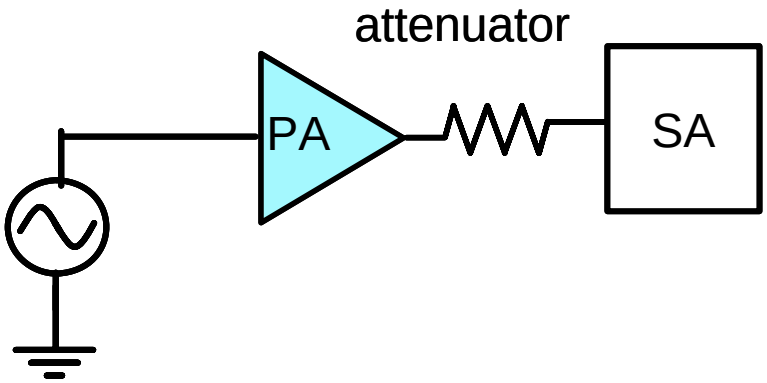
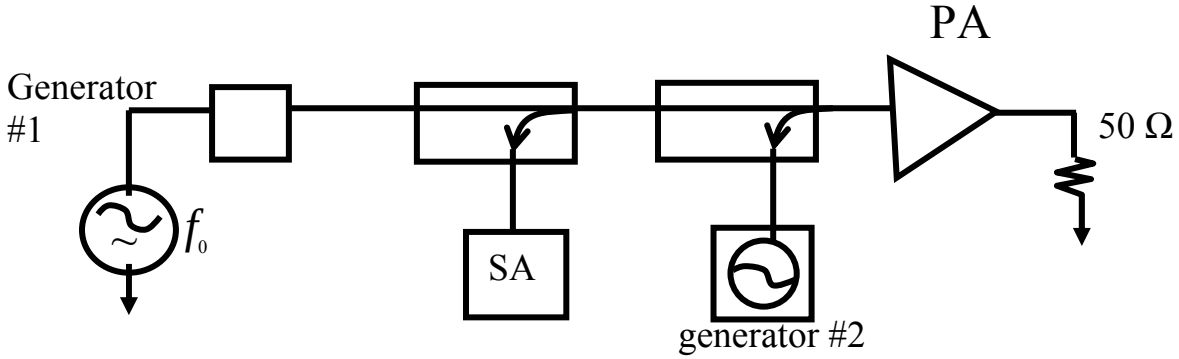
Experimental Measurement for Stability

Test #1

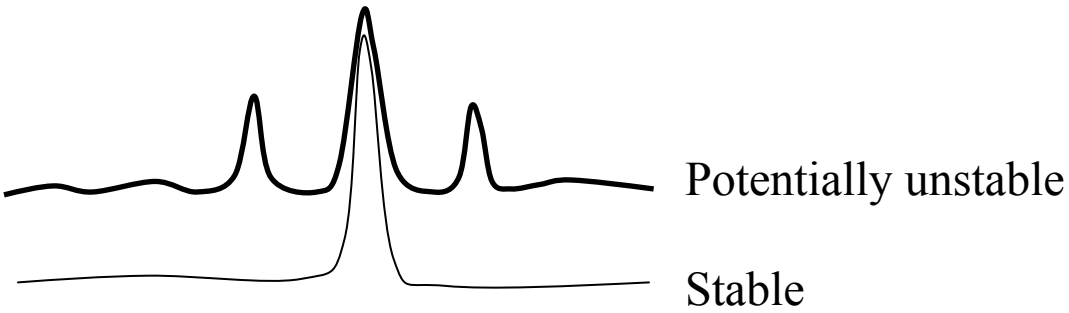


Generator at f0. Turn generator on. Is there any output at other frequencies? Turn generator off. Is there any output at all with no input?

Test #2



* Zoom in around f_0
* Vary frequency of generator 2 around f_0
* Look for peaks in reflected power



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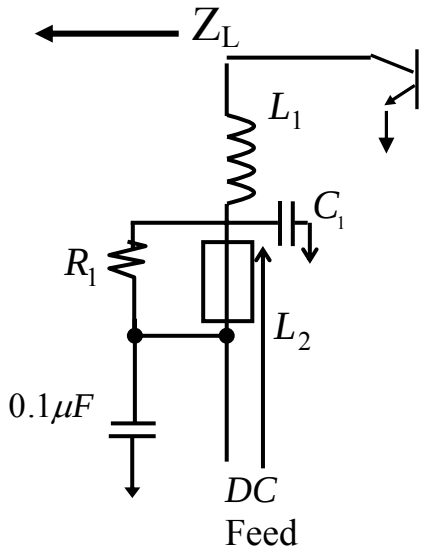
How can we provide low inductance bias feed and still have good control of L at low frequencies?

Typically, a more complicated decoupling system is required for power amplifiers to avoid resonances and oscillation (which could be done by introducing loss). The trick is to do this without losing power or efficiency.

Here is one approach for the drain or collector bias feed:



$$Z_{L_1} \quad 10 \bullet |Z_L|$$

$$R_1 \quad \approx |Z_L|$$

$$Z_{C_1} \quad \frac{1}{10}|Z_L|$$

L_2 Ferrite Bead

Power Amplifier Design 2

Summary:

PA impedance matching techniques

a. Load pull contours are used instead of gain circles to map power output and power gain as a function of load impedance.
b. Package parasitics can transform load impedances. It's the impedance at the collector or drain that is critical to achieving optimum performance.
c. Large signal input match will be different from small signal. Harmonic balance simulation method can be used to predict the proper input source impedance.

Design for stability. Bias circuits and associated components must be designed to limit low frequency gain. Harmonic balance methods must be used to predict large signal stability of the amplifier over a wide frequency range.