Receiver design suggestions ece145C/218C

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Simulating the phase frequency difference detector

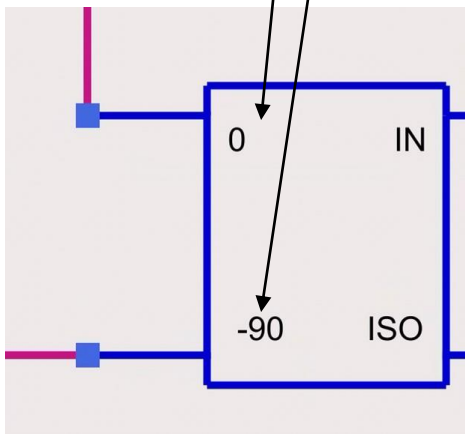
This is a transistor level representation. It uses very approximate models of the recommended PNP and NPN transistors. Don't use these models elsewhere in your design; elsewhere, instead use the mrf 901 model provided to you

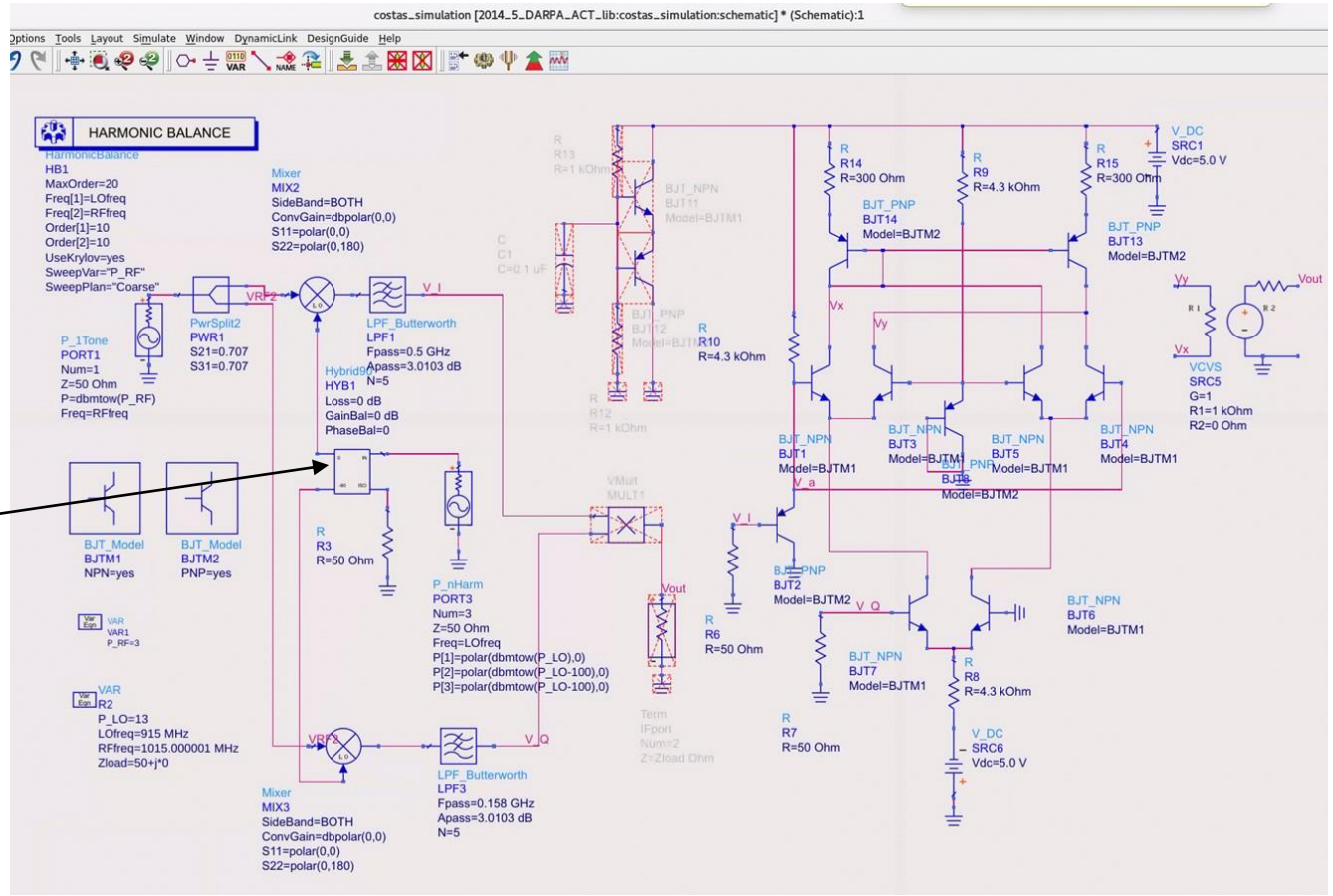
The rf power is 3dBm and is split to give 0 dbm at the input to each mixer. The LO power is 13 dBm and is split to give 10 dbm at the LO port of each mixer.

The resistor R8 provides 0.99 mA bias current to BJT7/8.

There is a current-mirror load (BJT13/14). The VCVS, SRC5 Is a temporary device for some simulations. Here I set it to one kOhm input impedance

Note very carefully the zero degree and -90 degree port markings on the 90 degree power splitter…
If you reverse these, the gain of the phase frequency detector will change sign (!).





Simulating the Frequency difference detector

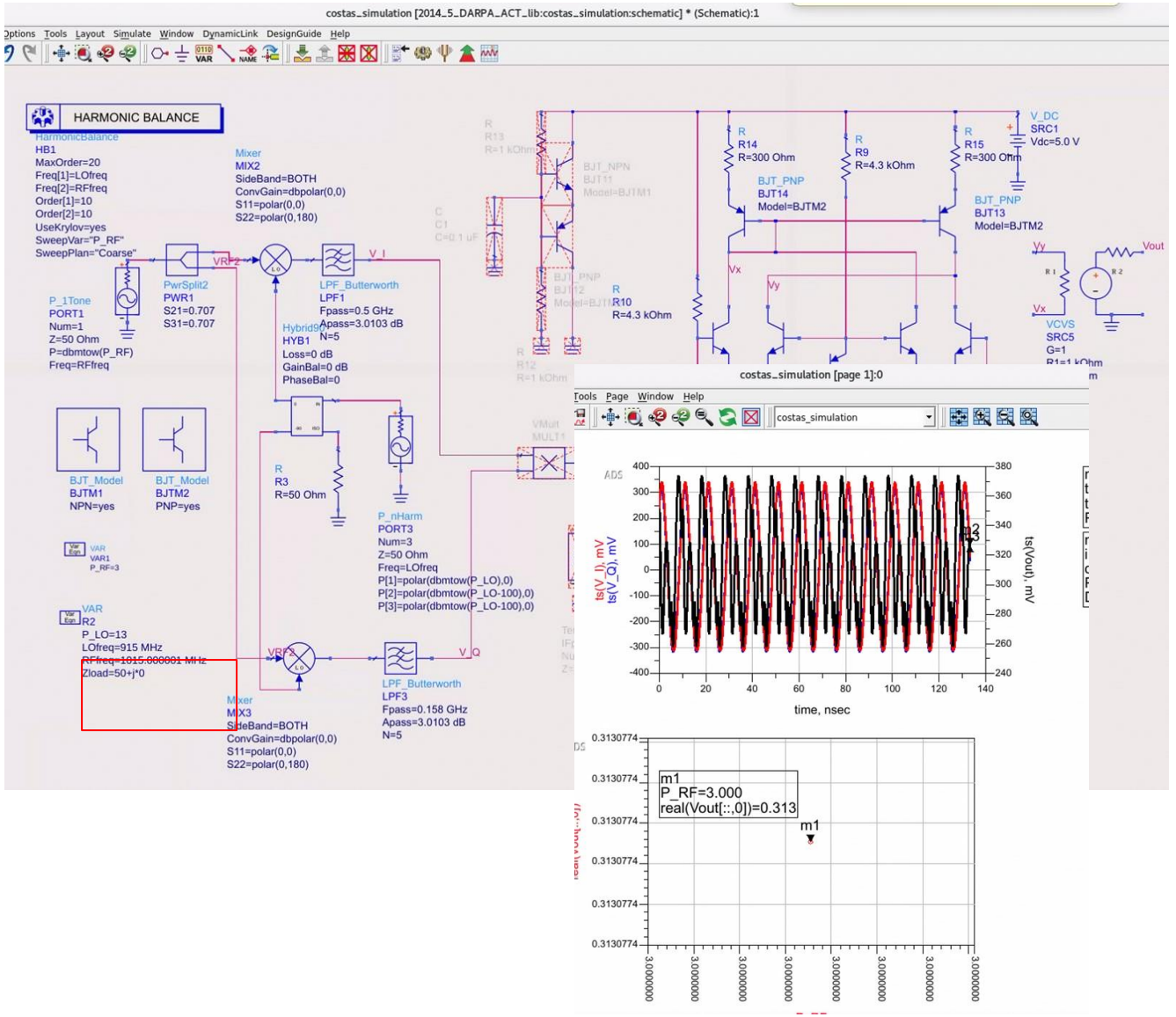
The RF frequency is set 100 MHz above the LO frequency, 100 MHz offset

The detector output is +0.326 V into this 1kOhm load,
so the detector output is +0.326 **mA**.

Note $dI_{out} / df_{RF} > 0$
$\rightarrow dI_{out} / df_{LO} < 0.$
Given that df_{LO} / V_{LO} is positive, $dI_{out} / df_{LO} < 0$ gives the desired negative feedback

You can vary the frequency and make a plot of the frequency difference detector output CURRENT as a function of frequency difference.

Note the filter labelled LPF3....this is the filter setting the time delay difference between the two paths.



Simulating the phase difference detector

The RF frequency is set 1 Hz above the LO frequency, giving a phase difference that sweeps from zero degrees to 360 degrees in one second.
The output changes 0.485Volts, hence 0.485 mA, in 0.032 seconds,
but 1 second is 360 degrees or 2π radians, so the phase detector slope is

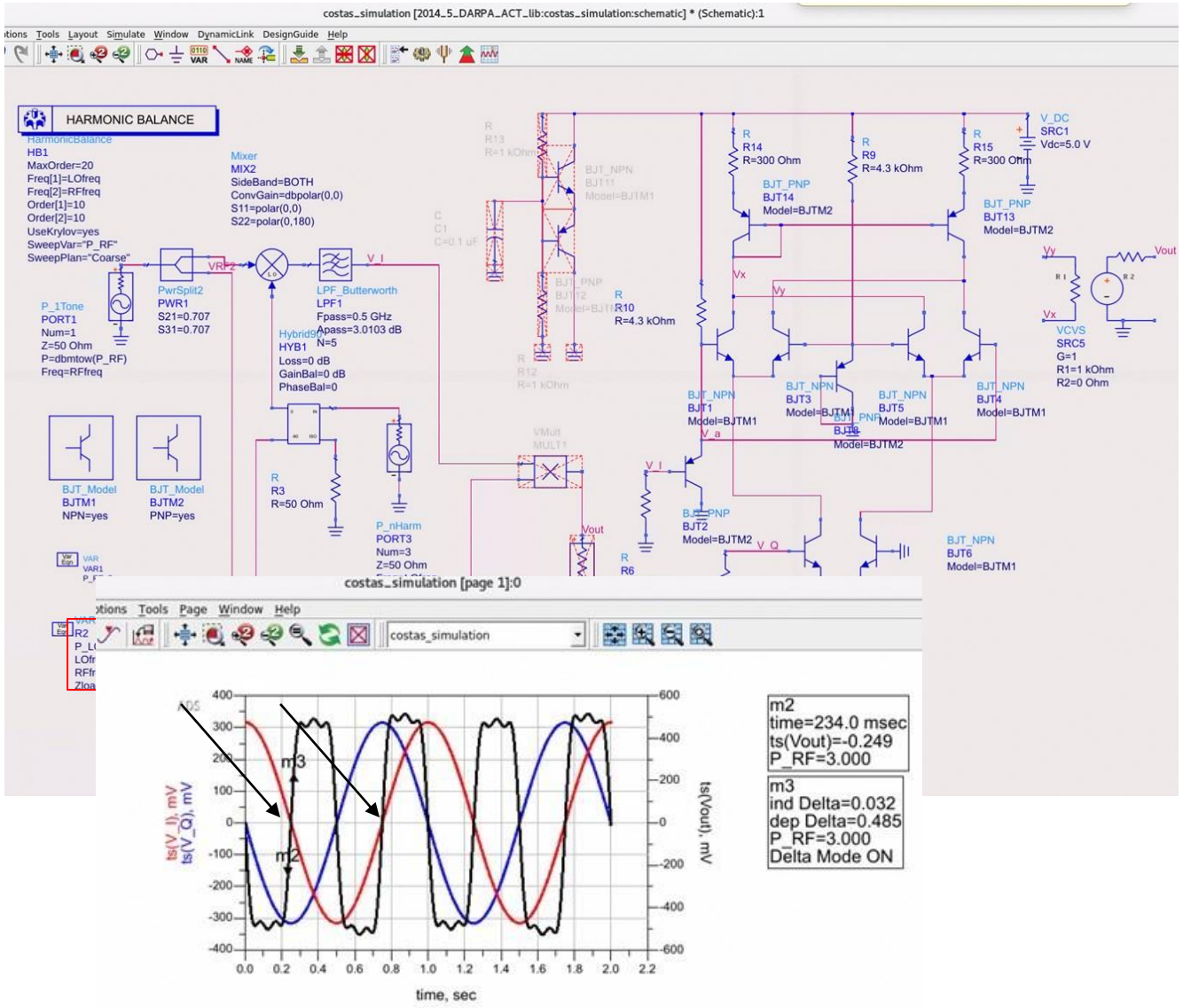
$$K_{\det} = \frac{dI_{out}}{d\theta_{RF}} = \frac{0.485mA}{0.032\sec}\frac{1\sec}{2\pi\text{radians}} = 2.41\frac{mA}{\text{radian}}$$

Tricky point: the loop will lock when $I_{out} = 0$ *and* when $dI_{out} / d\theta_{LO}$ *is negative*.
Hence, $I_{out} = 0$ *and* when $dI_{out} / d\theta_{RF}$ *is postive*.

Hence, the loop will lock at one of the phase states indicate by the arrows.

Note, that, at those phase states, $V_I = 0$ and $V_Q \neq 0$.
So, the data outputs must be taken from the *Q* outputs, not the I outputs.

In case we've made a mistake here, it would be wise to provide an option on the PCB to use either mixer output.

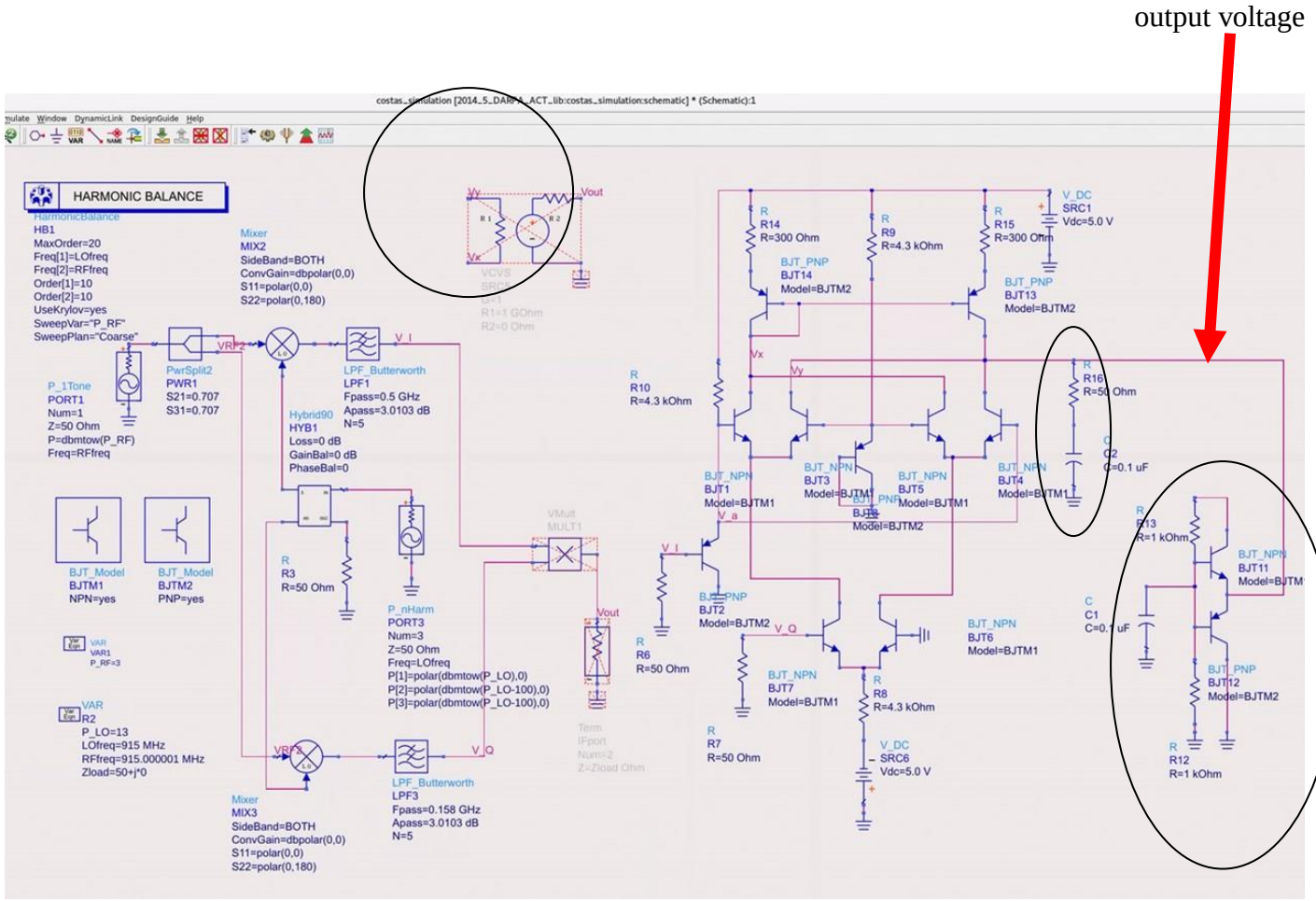


The combined phase detector and loop integrator

The VCVS SRC5 was just a way to monitor
the output current of the 3rd mixer during simulations

In the actual circuit, the output of the 3rd mixer is a *current*,
which drives a series RC network (circled). That makes the loop integrator.

Also circled is a limiter circuit (R12, R13, BJT11, BJT12), that limits the VCO control voltage to the range $5\text{V}\cdot(R_{12}/(R_{12}+R_{13}))\pm 0.7\text{V}$. Pick the resistors so that the VCO can't tune more than about ± 100 MHz away from 915MHz.



The combined phase detector and loop integrator

This re-draws the 3rd mixer and the loop integrator more clearly.

Here we we have

$I_{DET} = K_{DET}(\theta_{RF} - \theta_{LO})$

$V_C = I_{DET}(1/sC_i + R_z) = K_{DET}(\theta_{RF} - \theta_{LO})(1/sC_i + R_z) =$

$V_C = K_{DET}(\theta_{RF} - \theta_{LO})\dfrac{1+sR_zC_i}{sC_i}$

In the time domain: $\omega_{VCO}(t) = \omega_0 + K_{VCO}V_C(t)$

In the LaPlace domain: $\theta_{VCO}(s) = \theta_{LO}(s) = K_{VCO}V_C(s)/s$

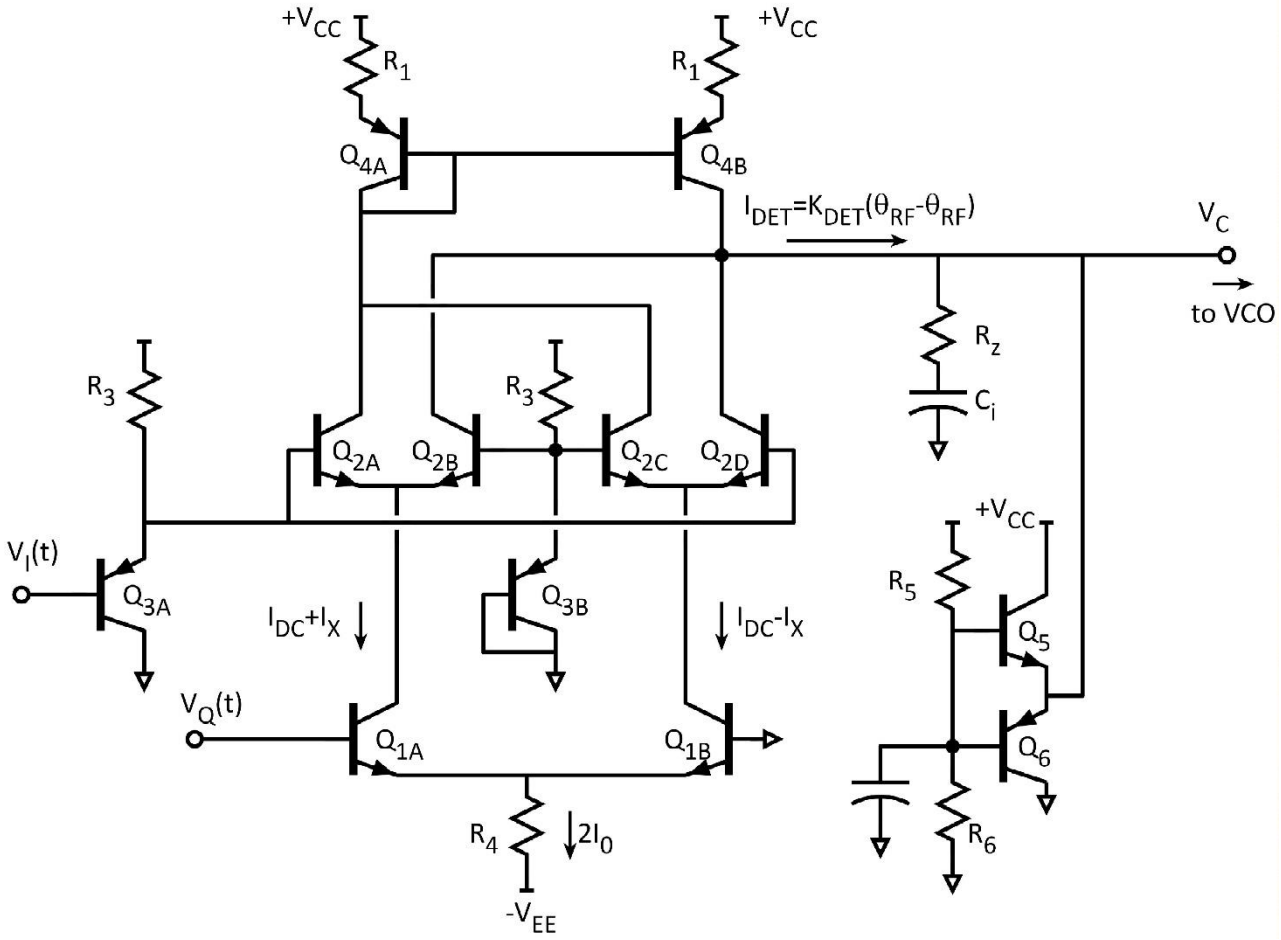
$\theta_{LO}(s) = K_{VCO}K_{DET}(\theta_{RF} - \theta_{LO})\dfrac{1+sR_zC_i}{s^2C_i}$

which gives us:

$\theta_{LO}(s) = \theta_{RF}(s)\dfrac{T(s)}{1+T(s)}$ where $T(s) = K_{VCO}K_{DET}\dfrac{1+sR_zC_i}{s^2C_i}$

Note again the clamping circuit (Q5,Q6) which limits the VCO frequency tuning range, keeping it close to 915 MHz

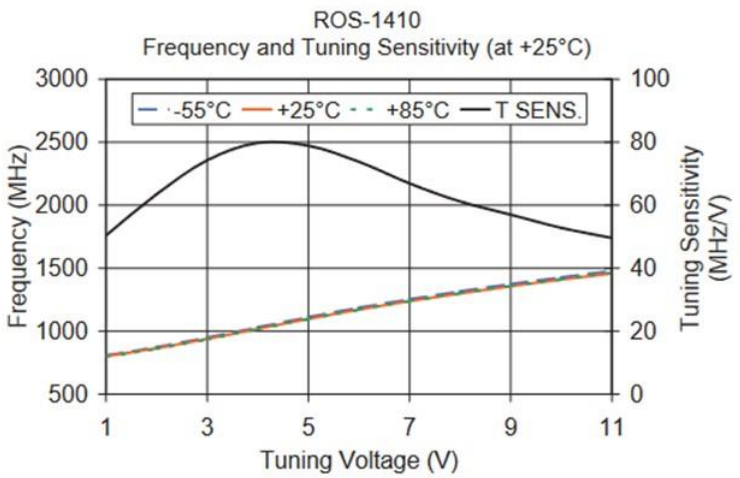
Note that the inputs don't have 50 OHm termination resistances.... the block diagram will make clear why



VCO characteristics

The VCO tunes from 864 to 939 MHz between 2 and 3 V…that is 75 MHz/V
The 3dB modulation bandwidth is 95 MHz

Note that you should limit the VCO tuning range to near to 915 MHz

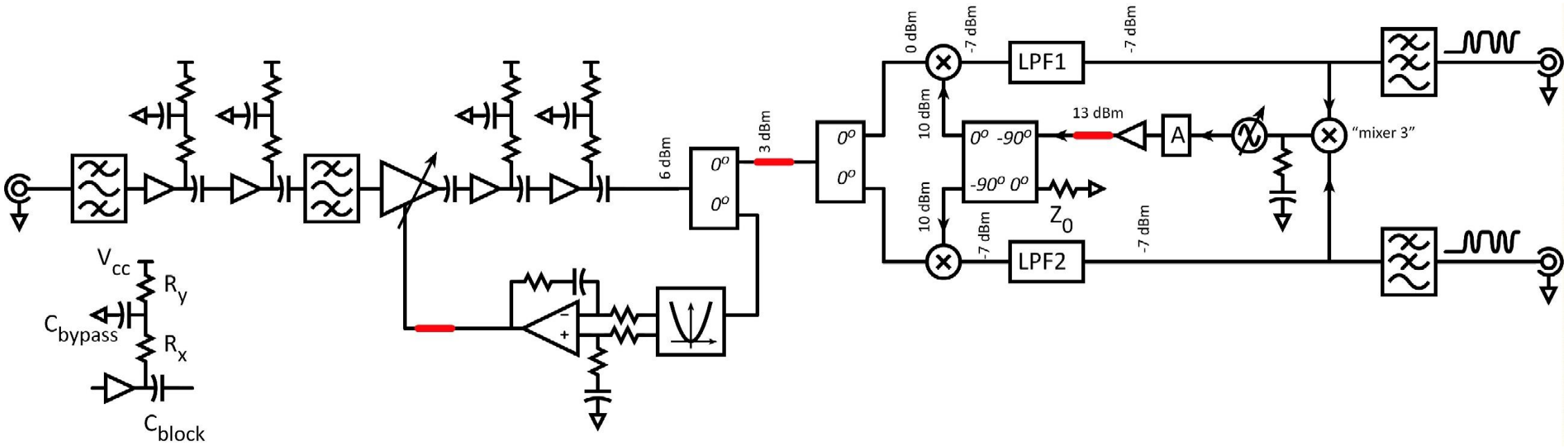


V TUNE	TUNING SENS. (MHz/V)	FREQUENCY (MHz)		
		-55°C	+25°C	+85°C
1.00	50.40	807.72	801.40	796.23
2.00	63.50	873.09	864.86	860.66
3.00	74.30	949.34	939.17	936.08
4.00	79.80	1030.94	1018.98	1017.08
5.00	78.90	1111.03	1097.86	1097.10
6.00	73.80	1185.85	1171.66	1172.04
7.00	66.90	1253.22	1238.55	1240.14
8.00	61.20	1315.49	1299.71	1302.25
9.00	57.00	1373.25	1356.73	1360.05
10.00	52.80	1427.15	1409.55	1413.71
11.00	49.60	1477.46	1459.17	1464.05

Overall Suggested receiver block diagram: changed

The AGC loop now measures the signal at the PLL input, not the PLL output. The red lines denote jumper line locations. I show 4 RF gain stages. Please calculate sensitivity (kT/2)FB*SNR, and determine how many stages you would need for the receiver to be noise-limited (about 6, giving about 100 dB RF gain). There is a danger this will cause oscillation through supply coupling so (1) maybe use less stages (or provide the option to use more or less) (2) use the supply bypass networks (RY, RX), use blocking capacitors Cblock no larger than needed to pass 915 MHz, and (4) use, as shown, a 2nd filter midway through the chain to bandlimit the amplification.

Be sure to analyze carefully which output to use of the peak detector, so your AGC loop has negative feedback



Phase Frequency difference detector

The phase frequency difference detectoris red boxed region in the block diagram.

The third multiplier, circled in blue on the left diagram, is shown in detail on the right diagram