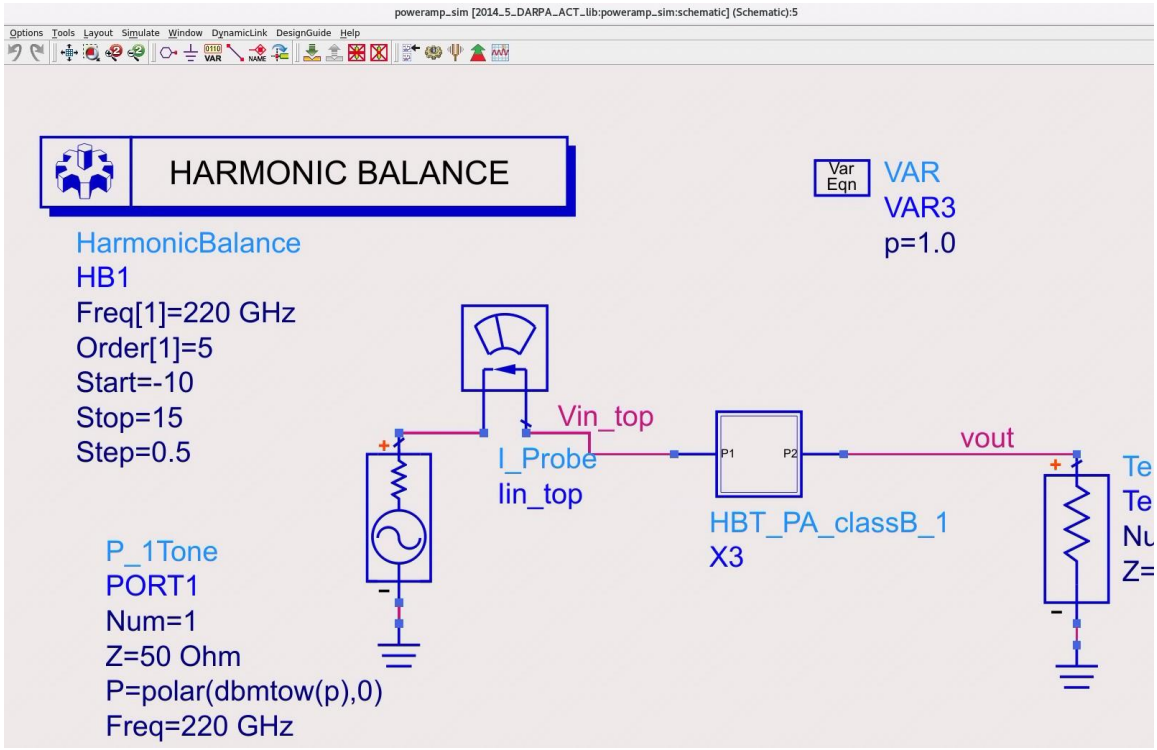
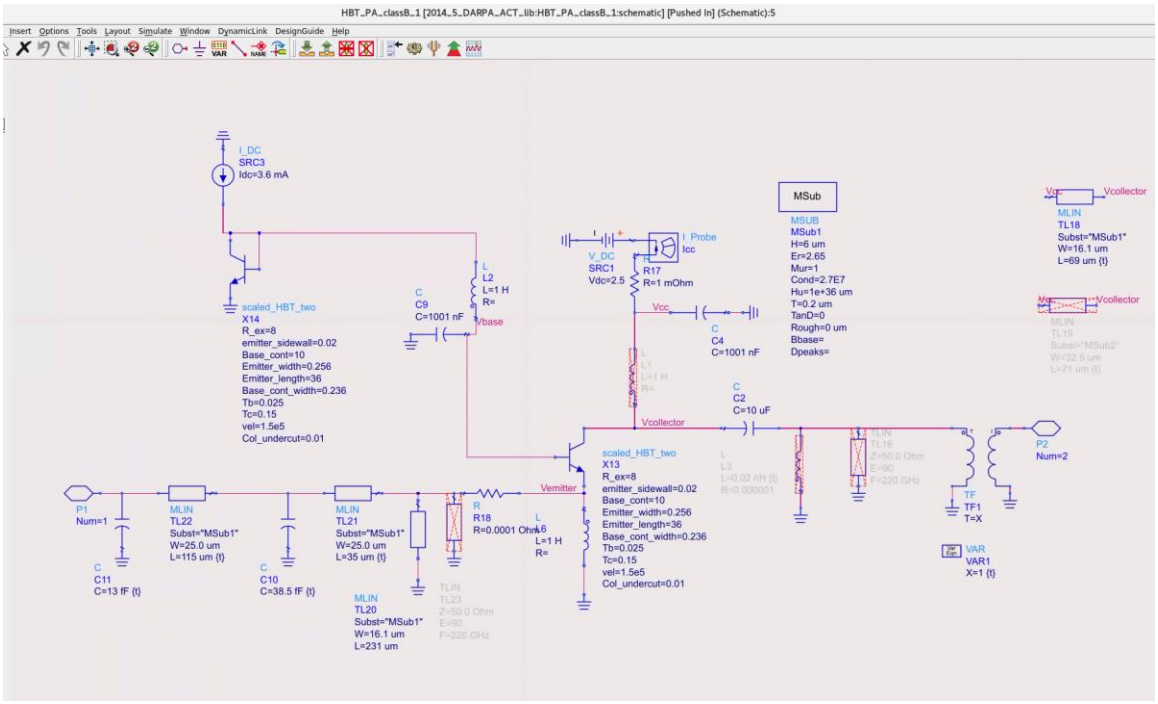
ECE 145C/218C third problem set: class B amplifiers and frequency doublers.

This will use an ads directory called 2021_4_class_B_doublers. A compressed version of this is on the website, with a link next to that of problem set 3.

Problem 1:
Open the simulation file: poweramp_sim



Then click on the circuit HBT_PA_classB_1 :

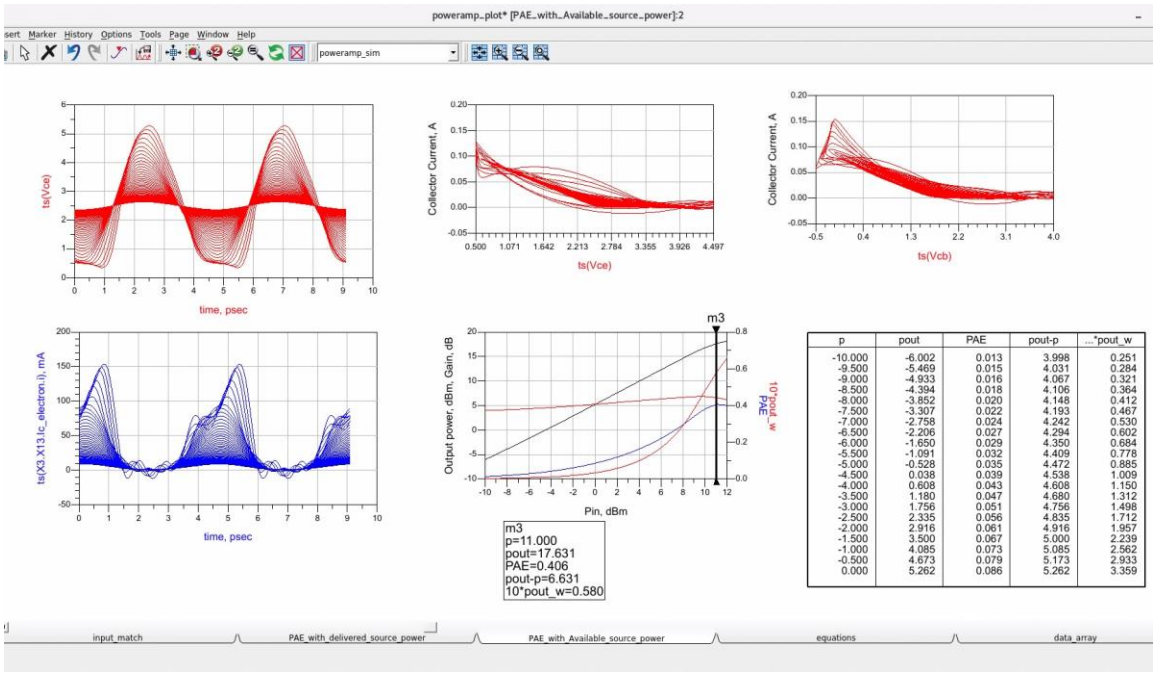


The circuit has a bias feed line TL19, and , crossed out, and ideal output tuning network consisting of L3 and TF1. Also crossed out is 1/4 wavelength transmission line TL16 Which is used to short circuit the second harmonic of the output signal.

Note that the HBT has a 36 micromeeter emitter length. It has a maximum emitter current density of 2 mA/micrometer, hence a maximum emitter current of 72 mA. The maximum collector-emitter voltage (Vce) is 4.5V; the minimum (at "saturation"; actually the Kirk effect) is about 0.7V-0.8V. That information defines the optimum loadline.

Note the class B bias circuit using a current mirror. This is *not recommended* in a real design; it would be electrothermally unstable. But, it is fine for this design exercise.

The circuit is presently set up to work correctly at two hundred and twenty GHz, with the input and output tuning networks correctly designed:



p	pout	PAE	pout-p	...*pout_w
-10.000	-6.002	0.013	3.998	0.251
-9.500	-5.469	0.015	4.031	0.284
-9.000	-4.933	0.016	4.067	0.321
-8.500	-4.394	0.018	4.106	0.364
-8.000	-3.852	0.020	4.148	0.412
-7.500	-3.307	0.022	4.193	0.467
-7.000	-2.758	0.024	4.242	0.530
-6.500	-2.206	0.027	4.294	0.602
-6.000	-1.650	0.029	4.350	0.684
-5.500	-1.091	0.032	4.409	0.776
-5.000	-0.528	0.035	4.472	0.885
-4.500	0.038	0.039	4.538	1.009
-4.000	0.608	0.043	4.608	1.150
-3.500	1.180	0.047	4.680	1.312
-3.000	1.756	0.051	4.756	1.498
-2.500	2.335	0.056	4.835	1.712
-2.000	2.916	0.061	4.916	1.957
-1.500	3.500	0.067	5.000	2.239
-1.000	4.085	0.073	5.085	2.562
-0.500	4.673	0.079	5.173	2.933
0.000	5.262	0.086	5.262	3.359

Note the class B loadline. Note the plot of output power and PEA vs. Available input power. Note also the other graph tab that gives plots of PA versus *delivered* (as opposed to available) input power; this is useful to simulate the performance of the PA as a function of the output tuning network, when the *input* tuning network has not yet been correctly adjusted.

Your assignment is to re-design the circuit at 140 GHz.

a) change the simulation frequency to 140 GHz. Enable the elements L3, TL16, and L1, to bring in the ideal output tuning network. Make TL16 a quarter wavelength at 140 GHz. Disable (Remove from the circuit) the element TL18. Then, adjusting the available input power as necessary, tune the output network to obtain the optimum class B load line. Include in your submitted work graphs of the circuit diagram with element values, the resulting loadline, and the graph of Pout and PAE vs. *delivered* input power.

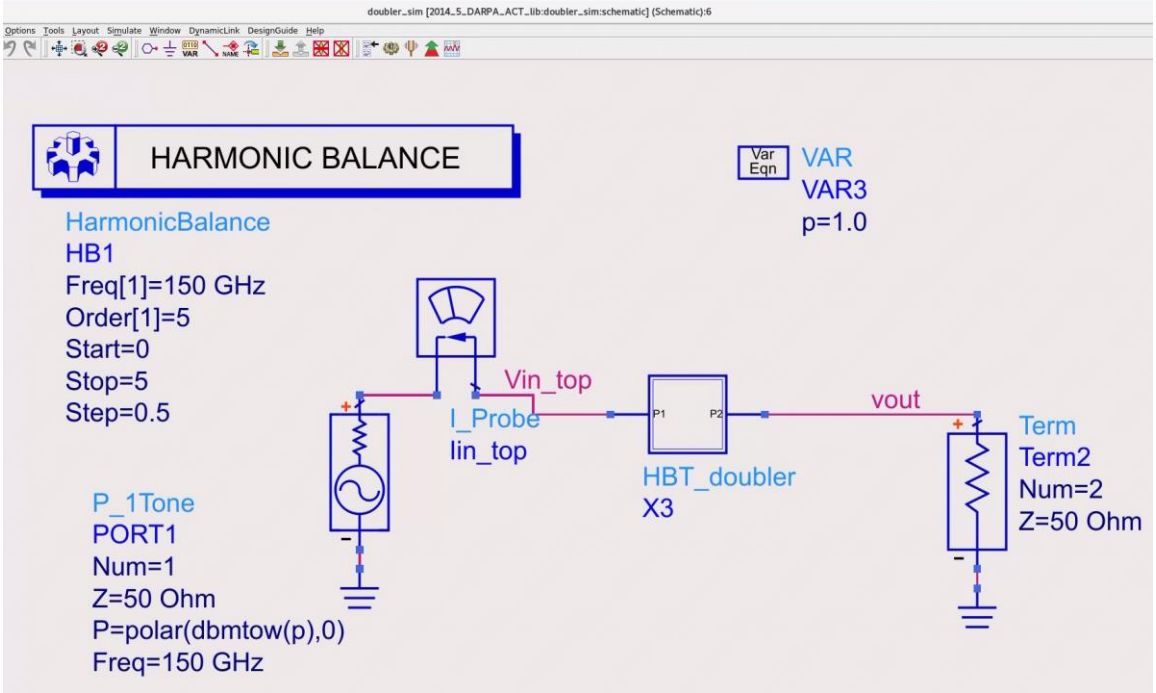
b) The simulation above gives you the required value of load admittance. Now replace the ideal output tuning network with one using MLIN transmission-lines (with substrate Msub1), and, as needed, ideal capacitors. No ideal inductors are allowed. No capacitor larger than 500 fF are allowed. Except, the bypass capacitor C4 can be as large as 1 pF. Re-simulate the circuit. Include in your submitted work graphs of the circuit diagram with element values, the resulting loadline, and the graph of Pout and PAE vs. *delivered* input power.

c) Now using the "input match" tab on the graph, adjust the input tuning network to give a small large-signal S11 when the amplifier is operating at an output power corresponding to maximum PAE. Include in your submitted work graphs of the circuit

diagram with element values, the resulting loadline, and the graph of Pout and PAE vs. *available* input power.

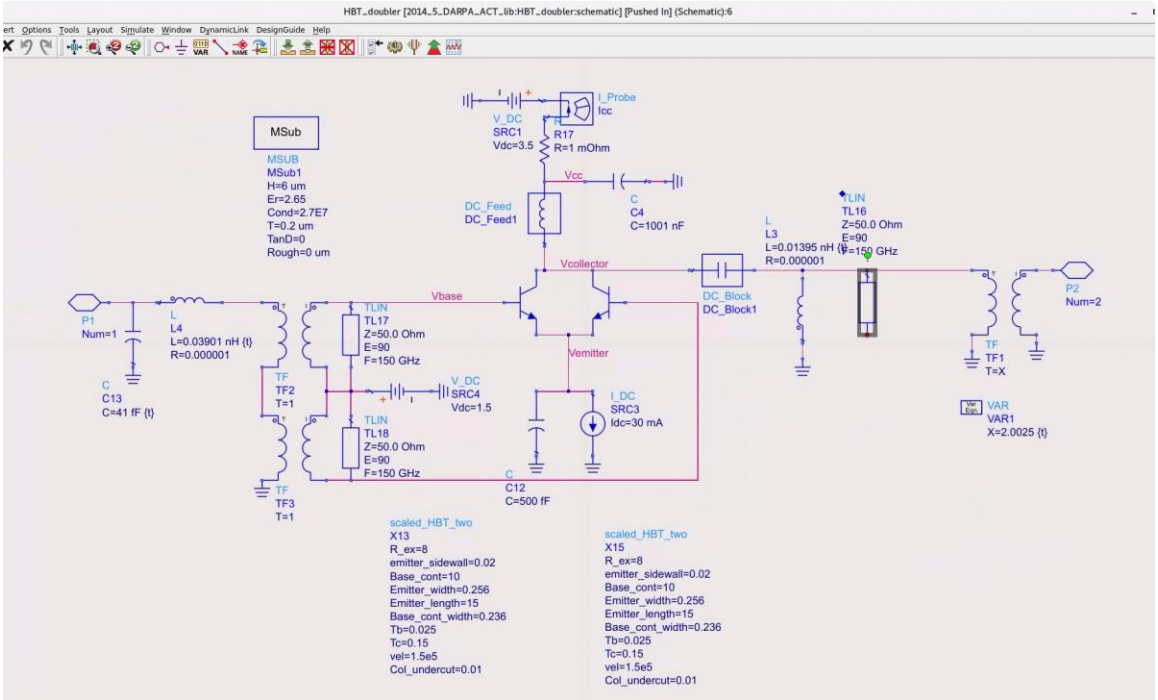
Problem 2:

Open the simulation file: doubler_sim



THis drives a frequency doubler at 150 GHz input frequency.

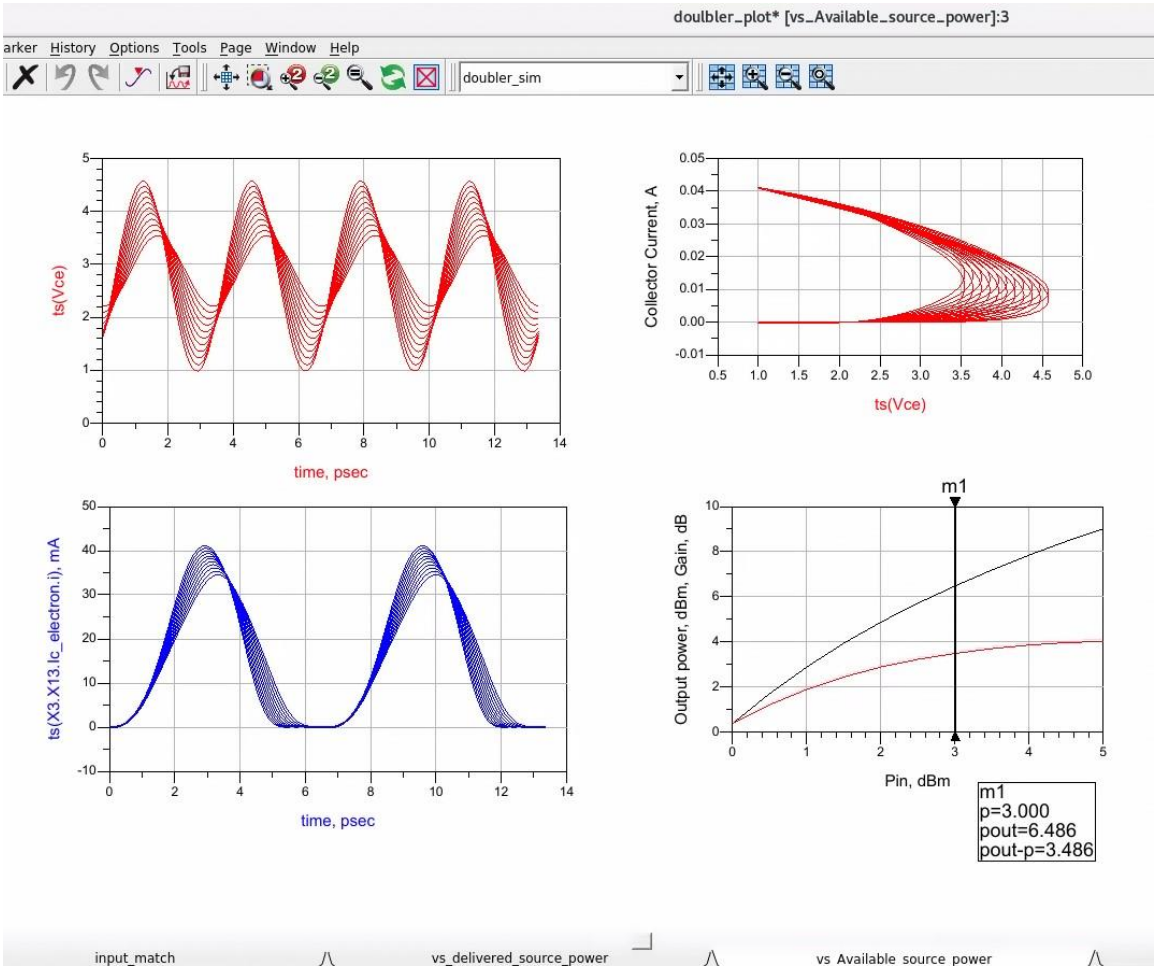
Then click on the circuit HBT_doubler :



The circuit has a bias feed line DC_Feed1, a blocking capacitor DC_block1, and an output ideal tuning network L3 and TF1. There is also an open-circuited line that is a quarter wavelength at the input frequency. This short-circuits the input frequency and its third harmonic at the output, while presenting an open at the 2nd harmonic.

Note that the two HBTs each have a 15 micrometer emitter length. It has a maximum emitter current density of 2 mA/micrometer, hence a maximum emitter current of 30 mA. The maximum collector-emitter voltage (Vce) is 4.5V; the minimum (at "saturation"; actually the Kirk effect) is about 0.7V-0.8V. That information defines the optimum loadline.

The circuit is presently set up to work correctly with a 150 GHz input and a 300 GHz output, with the input and output tuning networks correctly designed.



Note the nearly ideal frequency doubler load line in the top righthand corner. This plot shows power added efficiency versus Available input power. Once again there is also a tab which will show a graph of output power and efficiency versus delivered source power. There is also a tab for large signal input match.

Your assignment is to re-design the circuit for a 70 GHz input, such that the output is at 140 GHz.

a) change the simulation frequency to 70 GHz. Appropriately change the "F" parameter of lines TL16, TL17, TL18. Adjust the output ideal tuning network (L3, TF1) To obtain the optimum load line, with peak 4.5 V, minimum ~0.7V to 1.0V, And maximum 30 mA peak collector current. Replace SRC3 with a resistor giving the same DC current. Include in your submitted work graphs of the circuit diagram with element values, the resulting loadline, and the graph of Pout and PAE vs. *delivered* input power.

b) The simulation above gives you the required value of load admittance. Now replace the ideal output tuning network with one using MLIN transmission-lines (with substrate Msub1), and, as needed, ideal capacitors. You must replace the dc block and dc feed with practical elements: finite capacitors and real MLIN transmission-lines. No ideal inductors are allowed. No capacitor larger than 500 fF are allowed. Except, the bypass capacitor C4 can be as large as 1 pF. Re-simulate the circuit. Include in your submitted work graphs of the circuit diagram with element values, the resulting loadline, and the graph of Pout and PAE vs. *delivered* input power.

c) Now using the "input match" tab on the graph, adjust the input tuning network to give a small large-signal S11 when the amplifier is operating at an output power corresponding to maximum PAE. Replace L4 With a real microstrip line in your input matching network design. If necessary change the topology of the input matching network. Include in your submitted work graphs of the circuit diagram with element values, the resulting loadline, and the graph of Pout and PAE vs. *available* input power. Note that the resulting design still has ideal Transformers on the input. This is not reflective of a real design, but it is too much to ask you to design a transformer or ballon in this process and its interconnect geometry.