

# Design of a 32.7-GHz Bandwidth AGC Amplifier IC with Wide Dynamic Range Implemented in SiGe HBT

Kenichi Ohhata, Toru Masuda, Eiji Ohue, and Katsuyoshi Washio

**Abstract**—A wide-bandwidth automatic gain control (AGC) amplifier IC was developed using a self-aligned selective-epitaxial SiGe heterojunction bipolar transistor (HBT). A transimpedance load circuit was used, and its damping factor was optimized to achieve a wide bandwidth of 32.7 GHz. Capacitor peaking was introduced to the second variable-gain amplifier in order to obtain a wide gain dynamic range of 19 dB. The amplifier IC has a noise figure of 18 dB and an eye pattern at 25 Gb/s.

**Index Terms**—Automatic gain control (AGC) amplifier, optical transmission system, SiGe heterojunction bipolar transistor (HBT).

## I. INTRODUCTION

THE recent popularity of the Internet and multimedia communications has greatly increased the demand for high-speed communication systems. Optical transmission systems operating at 10 Gb/s have been developed for large capacity networks to meet this demand, and a transmission system as fast as 40 Gb/s is just now being developed. Several component IC's for a 40-Gb/s system have been reported, which use various high-speed devices such as Si bipolar transistors [1], heterojunction bipolar transistors (HBT's) based on SiGe [2]–[5] and InP/InGaAs [6], GaAs MESFET's [7], and high electron mobility transistors (HEMT's) [8]. SiGe HBT is one of the most promising of these devices because it is inexpensive and highly reliable.

Automatic gain control (AGC) amplifier IC's are key components in optical-fiber transmission systems. Both wide bandwidth and wide dynamic range are indispensable for an AGC amplifier IC. A packaged AGC amplifier with a bandwidth of 26 GHz and a dynamic range of 6 dB, developed using AlGaAs/GaAs HBT's with a cutoff frequency of 76 GHz, has been reported [9]; however, both its bandwidth and dynamic range were insufficient for the 40-Gb/s system. In general, the minimum bandwidth needed in a bit rate  $f_b$  is about  $3/4 f_b$  [10]; therefore, a bandwidth of more than 30 GHz is required in a 40-Gb/s system. We recently reported on a Si-based AGC amplifier having a wide bandwidth of 32.7 GHz and a dynamic range of 19 dB [3], which uses self-aligned selective-epitaxial SiGe HBT's [2].

Manuscript received January 5, 1999; revised March 24, 1999.

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Publisher Item Identifier S 0018-9200(99)06491-4.

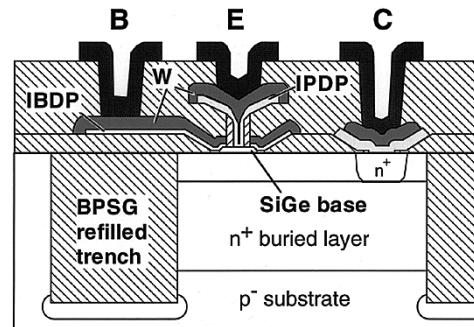


Fig. 1. Schematic cross section of a selective-epitaxial SiGe HBT with SMI electrodes.

To develop an AGC amplifier for a 40-Gb/s optical transmission system, not only high-performance devices but also appropriate circuit designs are required in order to extract the device's maximum performance. Peaking techniques are especially essential to achieve a wide bandwidth. However, peaking should be carefully controlled because excessive peaking degrades the flatness in the group delay response, resulting in waveform distortion.

In this paper, we propose design aspects that optimize the peaking control of the variable-gain amplifier stage and show that this technique allows both a wide bandwidth and a wide dynamic range. Experimental results that prove the effectiveness of our design are also shown.

## II. SiGe HBT TECHNOLOGY

Fig. 1 shows a schematic cross section of a self-aligned selective-epitaxial SiGe HBT with self-aligned stacked metal/*in situ* doped poly-Si (SMI) electrodes. A 0.54- $\mu\text{m}$ -wide SiGe-base and Si-cap multilayer, self-aligned to a 0.14- $\mu\text{m}$ -wide emitter, was selectively grown by using an ultrahigh vacuum (UHV)/chemical vapor deposition (CVD) system. This self-aligned structure is very effective for reducing collector capacitance. To obtain high-speed characteristics, we used a 20-nm-thick  $1 \times 10^{19} \text{ cm}^{-3}$  boron-doped selective-epitaxial  $\text{Si}_{1-x}\text{Ge}_x$  layer with a 10-nm-thick two-step-ramped Ge profile (from 0 to 10% over 5 nm and from 10 to 15% over 5 nm) to form the intrinsic base, which was as shallow as 30 nm. A low thermal cycle process also resulted in a shallow emitter junction depth of 20 nm. To reduce the parasitic resistance of the base, emitter, and collector, tungsten

TABLE I  
TRANSISTOR SPECIFICATIONS

$A_F$	$0.14 \times 1.5 \mu\text{m}^2$
$r_{bb}$	$210 \Omega$
$C_{TE}$	$2.9 \text{ fF}$
$C_{TC}$	$3.6 \text{ fF}$
$C_{TS}$	$0.6 \text{ fF}$
$f_T$	$92 \text{ GHz}$ ( $V_{CE} = 2 \text{ V}$ )
$f_{\text{max}}$	$108 \text{ GHz}$

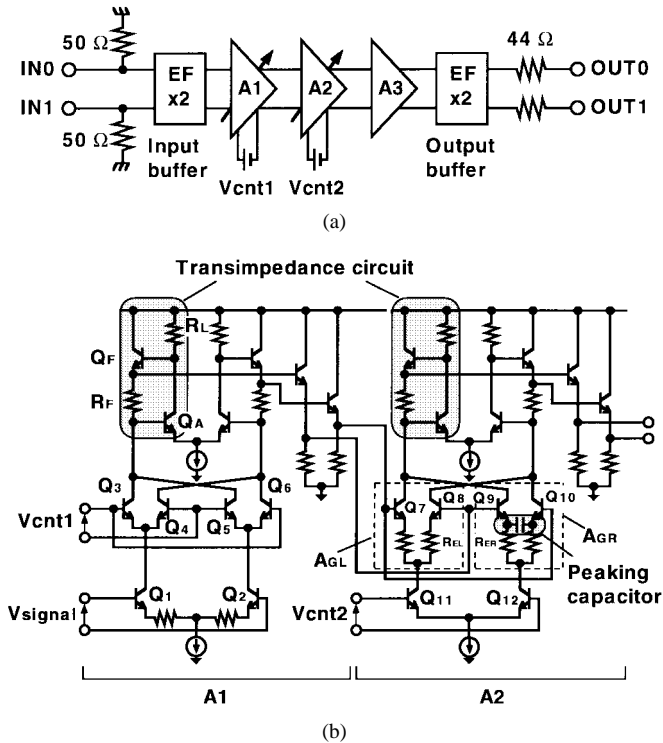


Fig. 2. Schematic of an AGC amplifier core: (a) block diagram and (b) variable-gain stage (A1 and A2).

film was selectively stacked, in a self-aligned manner, on *in situ* boron-doped poly-Si (IBDP) as the base electrode and on *in situ* phosphorous-doped poly-Si (IPDP) as the emitter and collector electrodes. Moreover, a  $2\text{-}\mu\text{m}$ -wide borophosphosilicate-glass-refilled trench was introduced to reduce the substrate capacitance.

The transistor characteristics are listed in Table I. The transistors with an emitter area of  $0.14 \times 1.5 \mu\text{m}^2$  had a cutoff frequency of 92 GHz and a maximum oscillation frequency of 108 GHz. The low collector capacitance of 3.6 fF is attributed to the fully self-aligned SiGe base structure, while the low substrate capacitance of 0.6 fF is attributed to the wide  $\text{SiO}_2$ -refilled trench. The base resistance of  $210 \Omega$  is attributed to the stacked tungsten/IBDP base electrode.

### III. CIRCUIT DESIGN

A schematic of the AGC amplifier core is shown in Fig. 2. The AGC amplifier is composed of an input buffer, two variable-gain stages (A1 and A2), a constant-gain stage (A3), and an output buffer. The differential gain of each amplifier

circuit stage is 8, 8, and 9 dB, respectively. Six dB is lost at the impedance-matching resistor in the output buffer, and another 6 dB is lost because of the single-ended output mode. The input and output buffers each contain two-stage emitter followers. The variable-gain stages consist of a Gilbert multiplier, whose load circuit is composed of a transimpedance circuit [11]–[13]. The transimpedance circuit is used because its low input impedance suppresses the Miller effect of the  $Q_7$ – $Q_{10}$  in the second variable-gain stage and because the bandwidth can be improved by peaking since the transfer function of transimpedance circuit can have two complex conjugate poles. The signal is applied to the lower transistor pair ( $Q_1$  and  $Q_2$ ), and the gain-control signal ( $V_{cnt1}$ ) is input to the upper transistor pairs ( $Q_3$ – $Q_6$ ) in the first gain-control stage. The connections of the signal and gain-control signal ( $V_{cnt2}$ ) are exchanged in the second gain-control stage because the two gain-control stages (A1 and A2) have opposite frequency-response dependencies on the gain, so the gain dependence of the frequency response can be compensated by optimizing the peaking capacitance  $C_P$  in the second gain-control stage [12]. In this circuit, the keys to achieving both a wide bandwidth and a wide dynamic range are the design of the transimpedance circuit, which is used as a load circuit of the Gilbert multiplier, and the peaking capacitance  $C_P$ .

The transimpedance circuit is composed of a common emitter amplifier ( $Q_A$  and  $R_L$ ) and a feedback circuit ( $Q_F$  and  $R_F$ ). The transimpedance gain  $Z_T$  of this circuit is approximately expressed as

$$Z_T \approx \frac{-R_F}{1 + \left(\frac{2K}{\omega_0}\right) + \frac{s^2}{\omega_0^2}}$$

$$\omega_0 \approx \sqrt{\frac{|a_{v0}|}{R_F r_{\pi} r_b (C_{\pi} + C_M)^2}}$$

$$K \approx \frac{1}{2} \sqrt{\frac{R_F}{r_b |a_{v0}|}} \quad (1)$$

where  $a_{v0}$  is an open-loop gain of the common emitter amplifier and  $r_{\pi}$ ,  $r_b$ ,  $C_{\pi}$ , and  $C_M$  are the input resistance, base resistance, sum of diffusion capacitance and base-emitter junction capacitance, and Miller capacitance of  $Q_A$ , respectively. The derivation of this equation is given in Appendix I.  $K$  is a damping factor, and the  $Z_T$  peaks when  $K < 1/\sqrt{2}$ . The bandwidth of the transimpedance circuit is dominated by  $\omega_0$ . Thus,  $r_b$ ,  $C_{\pi}$ , and  $C_M$  should be made small to obtain a wide bandwidth. The large emitter size of transistor  $Q_A$  reduces the  $r_b$ ; however, this makes the  $C_M$  large. Therefore, the emitter size of transistor  $Q_A$  should be optimized carefully. Moreover, a large  $a_{v0}$  also allows a wide bandwidth; however, this makes  $K$  small, resulting in a large peak in the frequency response.

The relationship between the bandwidth ( $\omega_{BW}$ ), peak height, and  $K$  is calculated by using (1) and is shown in Fig. 3. The bandwidth improves as  $K$  decreases due to the peaking effect; however, this improvement is small, and the peak height increases rapidly when  $K$  becomes less than 0.4. Fig. 4 shows the calculated 40-Gb/s eye pattern of the transimpedance circuit when  $K$  is 0.5 and 0.25. Here,  $K$  is changed by

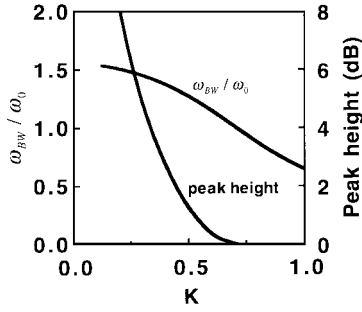


Fig. 3. Bandwidth and peak height dependence on damping factor  $K$ .

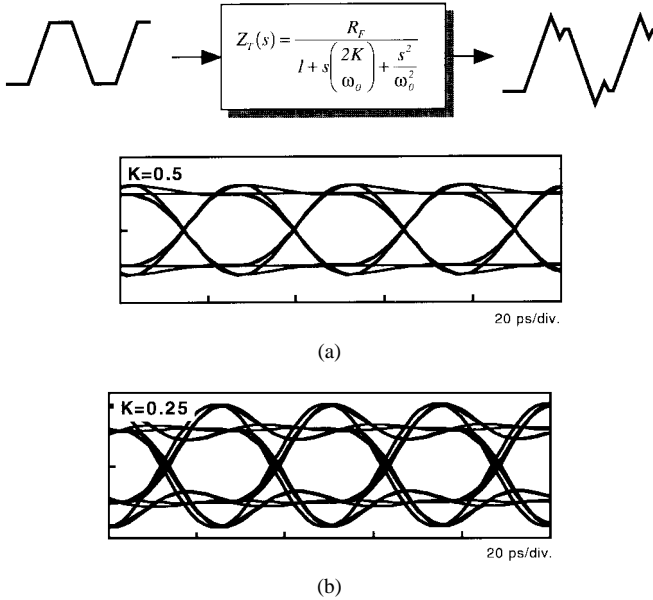


Fig. 4. Relationship between eye pattern and damping factor  $K$ : (a)  $K = 0.5$  and (b)  $K = 0.25$ .

the open-loop gain  $a_{v0}$ . The eye pattern is calculated by transforming the input waveform to the frequency domain by Fourier transform. Then the output frequency response of the transimpedance circuit is calculated by multiplying the input waveform spectrum and the  $Z_T(s)$ . Last, the output waveform is obtained by the inverse Fourier transform. A clear eye opening is achieved when  $K = 0.5$ . Large ringing and jitter arise as a result of the large peak and fluctuation in the group delay when  $K = 0.25$ . These results suggest that  $K$  should be controlled to be 0.4–0.5.

The damping factor  $K$  can be controlled by an open-loop gain  $a_{v0}$ . The circuit simulator should be used to precisely control the damping factor. To obtain accurate results, the delay element concerned with the feedback loop (the excess phase of  $h_{21}$  of  $Q_A$  and  $Q_F$ , interconnection delay in the transimpedance stage, etc.) should be carefully estimated. Fig. 5 shows the bandwidth and the peak height in the frequency-response dependence on the open-loop gain of the transimpedance circuit. These results are obtained by circuit simulation. A large open-loop gain lowers  $K$ , resulting in a wider bandwidth; however, the peak height also increases. Considering the tradeoff between the bandwidth and the peak height, we chose an open-loop gain of 12.

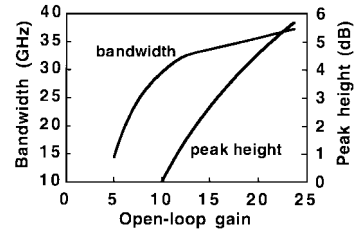


Fig. 5. Bandwidth and peak-height dependence on the open-loop gain.

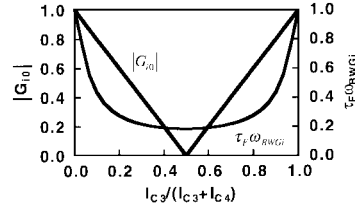


Fig. 6. Current gain and normalized bandwidth ( $\tau_F \omega_{BW G_i}$ ) dependence on the normalized current.

The current gain  $G_i$  of the gain-control circuit ( $Q_3$ – $Q_6$  in Fig. 2) is expressed as

$$G_i(s) \approx \frac{G_{i0}}{(1 + s\tau_F)(1 + s\alpha\tau_F)}$$

$$G_{i0} = \frac{g_{m3} - g_{m4}}{g_{m3} + g_{m4}}$$

$$\alpha = \frac{2g_{m3}g_{m4}}{g_{m3} + g_{m4}} r_b \quad (2)$$

where  $g_{m3}$  and  $g_{m4}$  are the transconductance,  $\tau_F$  is the base transit time, and  $r_b$  is the base resistance of transistors  $Q_3$  and  $Q_4$ . The bandwidth of  $G_i$  is expressed as

$$\omega_{BW G_i} = \frac{1}{\tau_F} \sqrt{\frac{\sqrt{(1 + \alpha^2) + 4\alpha^2} - (1 + \alpha^2)}{2\alpha^2}} \quad (3)$$

The derivation of these equations is given in Appendix II. Fig. 6 shows the gain and bandwidth dependence on the normalized collector current of  $Q_3$  ( $I_{C3}$ ). The dc gain  $G_{i0}$  increases linearly as  $I_{C3}$  increases and becomes zero at  $I_{C3} = I_{C4} = I_{C1}/2$ ; then the bandwidth also has a minimum value. This is because  $\alpha$  has a maximum value when  $g_{m3} = g_{m4}$ . Thus, the bandwidth of the first variable-gain amplifier decreases as the gain decreases. To compensate the bandwidth dependence on the gain in the first variable-gain amplifier, the peaking capacitor  $C_P$  is introduced in the second variable-gain amplifier. The transconductance gain ( $G_L$  and  $G_R$ ) of the two amplifiers ( $A_{GL}$  and  $A_{GR}$  in Fig. 2) is expressed as

$$G_L = \frac{G_{L0}}{1 - \frac{s}{p_{L0}}}$$

$$G_{L0} = \frac{g_{mL}}{1 + g_{mL}R_{EL}}$$

$$p_{L0} = -\frac{1 + g_{mL}R_{EL}}{r_{bL}C_{\pi L}} \quad (4)$$

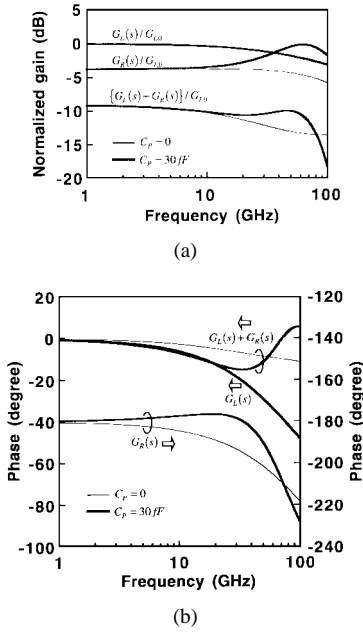


Fig. 7. Frequency response of (a) normalized gain and (b) phase of  $G_L$  and  $G_R$ .

and

$$G_R = \frac{-G_{R0} \left(1 - \frac{s}{z_{R0}}\right)}{1 + s \left(\frac{2K_G}{\omega_{0G}}\right) + \frac{s^2}{\omega_{0G}^2}}$$

$$G_{R0} = \frac{g_{mR}}{1 + g_{mR}R_{ER}}$$

$$z_{R0} = -\frac{1}{2R_{ER}C_P}$$

$$\omega_{0G} = \sqrt{\frac{1 + g_{mR}R_{ER}}{2r_{bR}R_{ER}C_{\pi R}C_P}}$$

$$K_G = \frac{2R_{ER}C_P + r_{bR}C_{\pi R}}{2\sqrt{2r_{bR}R_{ER}C_{\pi R}C_P(1 + g_{mR}R_{ER})}} \quad (5)$$

where  $g_{mL(R)}$ ,  $r_{bL(R)}$ , and  $C_{\pi L(R)}$  are transconductance, base resistance, and the sum of diffusion capacitance and base-emitter junction capacitance of  $Q_7$  and  $Q_8$ , ( $Q_9$  and  $Q_{10}$ ). The derivation of these equations is given in Appendix III.

Fig. 7 shows the normalized gain and phase of  $G_L$  and  $G_R$  calculated by using (4) and (5), when  $I_C(Q_{11}) = 1.8$  mA and  $I_C(Q_{12}) = 1.2$  mA. A peak is generated in the gain of  $G_R$  due to the zero  $z_0$ , concerning the peaking capacitor  $C_P$ . At first sight, the bandwidth of total gain ( $G_L + G_R$ ) seems to decrease due to this peak because  $G_R$  has an opposite phase to  $G_L$  due to the inverted input signal, so the peak of  $G_R$  decreases the total gain at high frequency. However, the bandwidth increases as shown in Fig. 7(a) when the  $C_P$  is introduced. This is because the phase of  $G_R$  is not opposite to  $G_L$  by the influence of  $z_0$ , as shown in the Fig. 7(b). The phase difference between  $G_R$  and  $G_L$  decreases and has a

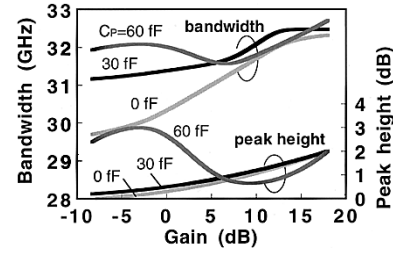


Fig. 8. Bandwidth and peak-height dependence on the gain.

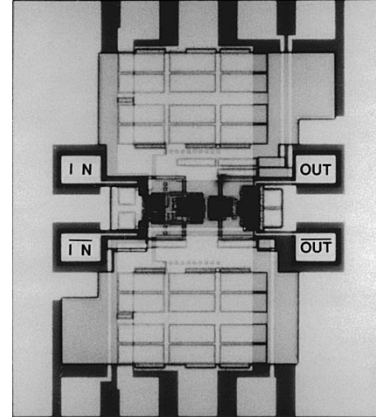


Fig. 9. AGC amplifier chip photomicrograph.

minimum value of  $155^\circ$  at 40 GHz when  $C_P$  is 30 fF. This improves the bandwidth of the total gain from 30 to 70 GHz. Thereby, these two amplifiers ( $A_{GL}$  and  $A_{GR}$ ) do not limit the bandwidth of the whole AGC amplifier.

Fig. 8 shows the simulated bandwidth and peak height dependence on a  $C_P$ . It is shown that a large  $C_P$  improves the bandwidth in the small gain range. The bandwidth from  $-8$  to 14 dB is almost constant when  $C_P$  is 60 fF; however, the peak height in the frequency response becomes 3 dB. A  $C_P$  of 30 fF was chosen to suppress the excessive peaking. A metal-insulator-metal (MIM) capacitor was used for the peaking capacitors to reduce the parasitic resistance. A 75-nm-thick TEOS film, deposited by plasma CVD, was used as an insulator, and  $0.5$  fF/ $\mu\text{m}^2$  was obtained.

#### IV. EXPERIMENTAL RESULTS

Fig. 9 shows a photomicrograph of the fabricated AGC amplifier core. The circuit elements composing the amplifier core were arranged symmetrically to minimize the offset. MIM shunt capacitors of 72 pF, which were connected between a supply voltage  $V_{EE}$  and the ground, were located above and below the amplifier core. The power dissipation was 725 mW at  $V_{EE}$  of  $-7.5$  V on a chip with a size of  $0.95 \times 1.08$  mm<sup>2</sup>. The gain, noise figure, and output eye pattern were measured using an on-wafer radio-frequency probe.

The measured gain versus frequency characteristics are shown in Fig. 10. A bandwidth of 32.7 GHz was achieved at a maximum gain of 13 dB, and it was 31.6 GHz at the minimum gain of  $-6$  dB. The input voltage range was 90–800

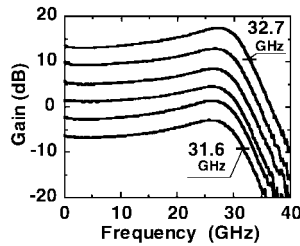


Fig. 10. Frequency response of the gain ( $C_P = 30$  fF).

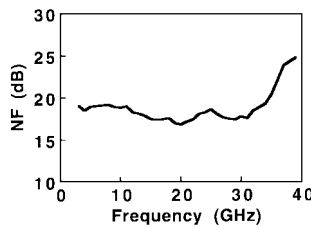


Fig. 11. Frequency response of the noise figure.

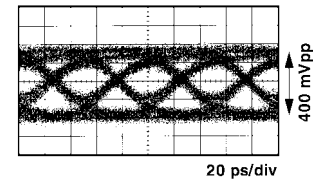
mV<sub>pp</sub>. Small fluctuation in the bandwidth was attributed to careful optimization of the peaking capacitor. The measured peak height was larger than the simulation value, as shown in Fig. 8. This is because the base resistance was larger than the design value, resulting in a small  $K$ .

Fig. 11 shows the noise figure (NF) versus frequency characteristics. The noise power of the AGC amplifier is very small; therefore, the output noise was amplified by a low-noise, wide-bandwidth amplifier (HP83051A), and the noise power was measured by a spectrum analyzer (HP8565E). The noise power of the low-noise, wide-bandwidth amplifier was subtracted from the measured noise power. An NF of about 18 dB below 30 GHz was achieved, and in the range above 30 GHz the NF rapidly increased because the gain decreased quickly beyond the bandwidth. The average NF up to the bandwidth was 18 dB.

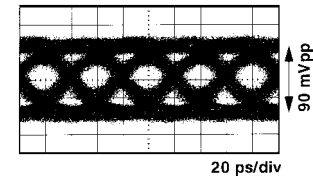
Fig. 12 shows the output eye pattern at 20 and 25 Gb/s. A 12.5-Gb/s pulse-pattern generator and a 2:1 multiplexer were used to generate an input pulse of  $2^{31}-1$  pseudorandom bitstream. The eye patterns were measured in single end. The voltage swing of the input pulse was 90 mV<sub>pp</sub>, and the gain was set to the maximum gain. A well-opened eye pattern was obtained at 20 Gb/s [Fig. 12(a)]; however, the eye pattern at 25 Gb/s [Fig. 12(c)] was not good enough. This is because the output waveform of the 2:1 multiplexer (the specification of maximum operating rate was 20 Gb/s) was not good, as shown in Fig. 12(b).

## V. CONCLUSION

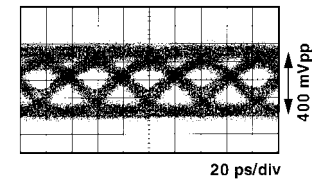
A wide-bandwidth AGC amplifier IC was developed using a high-performance SiGe HBT and a circuit design with peaking technique. A transimpedance load circuit was used, and its damping factor was optimized to achieve a wide bandwidth of 32.7 GHz. Capacitor peaking was introduced to the second variable-gain amplifier in order to obtain low-bandwidth variation. A gain dynamic range of 19 dB, a noise



(a)

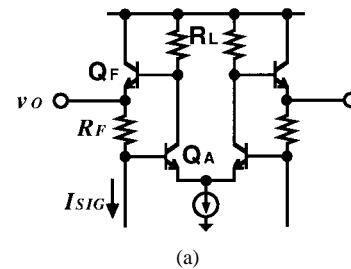


(b)

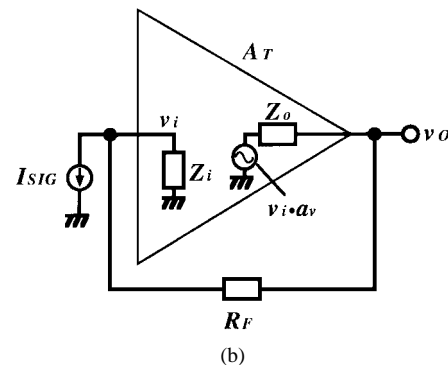


(c)

Fig. 12. Single-ended operational waveforms: (a) output waveform at 20 Gb/s, (b) input waveform at 25 Gb/s, and (c) output waveform at 25 Gb/s.



(a)



(b)

Fig. 13. Schematic of transimpedance: (a) load circuit and (b) its equivalent circuit.

figure of 18 dB, and an eye pattern at 25 Gb/s were also achieved.

## APPENDIX I DERIVATION OF (1)

Fig. 13 shows the schematic of the transimpedance load circuit and its equivalent circuit. The common emitter amplifier  $A_T$  is composed of  $Q_A$ ,  $Q_F$ , and  $R_L$ . The following equations

are obtained from the equivalent circuit:

$$\begin{cases} i_{\text{SIG}} = \frac{v_i}{Z_i} + \frac{v_i - v_o}{R_F + Z_o} \\ v_o = v_i - \frac{R_F}{R_F + Z_o}(v_i - a_v v_i) \end{cases} \quad (\text{A.1})$$

where  $Z_i$  and  $Z_o$  are the input and output impedance of  $A_T$ , respectively, and  $a_v$  is the voltage gain of  $A_T$ . The output impedance of  $A_T$  is much smaller than  $R_F$  because an emitter follower is used as an output buffer. Approximating  $Z_o \ll R_F$ , the transimpedance  $Z_T$  is obtained from (A.1) as

$$Z_T = \frac{v_o}{i_{\text{SIG}}} \approx \frac{a_v Z_i R_F}{R_F + Z_i(1 - a_v)}. \quad (\text{A.2})$$

$Z_i$  and  $a_v$  are obtained by using Miller capacitance approximation

$$Z_i(s) \approx \frac{r_\pi}{1 + s r_\pi (C_\pi + C_M)} \quad (\text{A.3})$$

$$a_v(s) \approx \frac{a_{v0}}{(1 + s R_L C_L)(1 + s r_b (C_\pi + C_M))} \quad (\text{A.4})$$

where  $r_\pi$ ,  $r_b$ ,  $C_\pi$ , and  $C_M$  are the input resistance, base resistance, sum of diffusion capacitance and base-emitter junction capacitance, and Miller capacitance of  $Q_A$ , respectively.  $a_{v0}$  is an open-loop gain, and  $C_L$  is the parasitic capacitance at the collector of  $Q_A$  that contains the output load seeing from the base of  $Q_F$ . Here, the bandwidth of the emitter follower ( $Q_F$ ) is much wider than the common emitter amplifier ( $Q_A$  and  $R_L$ ); thus, a pole concerning with the emitter follower is neglected. The time constant at the collector ( $R_L C_L$ ) is smaller than the time constant at the base ( $r_b (C_\pi + C_M)$ ); thus, (A.4) is reduced to

$$a_v(s) \approx \frac{a_{v0}}{1 + s r_b (C_\pi + C_M)}. \quad (\text{A.5})$$

Rearranging (A.2) by substituting (A.3) and (A.5) into it, the transimpedance is obtained as

$$\begin{aligned} Z_T &\approx \frac{\frac{a_{v0} r_\pi R_F}{R_F - a_{v0} r_\pi}}{1 + \left(\frac{2K}{\omega_0}\right) + \frac{s^2}{\omega_0^2}} \approx \frac{-R_F}{1 + \left(\frac{2K}{\omega_0}\right) + \frac{s^2}{\omega_0^2}} \\ \omega_0 &= \sqrt{\frac{R_F - a_{v0} r_\pi}{R_F r_\pi r_b (C_\pi + C_M)^2}} \approx \sqrt{\frac{|a_{v0}|}{R_F r_\pi r_b (C_\pi + C_M)^2}} \\ K &= \frac{1}{2} \sqrt{\frac{R_F}{R_F - a_{v0} r_\pi} \frac{(r_\pi + r_b)^2}{r_\pi r_b}} \approx \frac{1}{2} \sqrt{\frac{R_F}{r_b |a_{v0}|}} \end{aligned} \quad (\text{A.6})$$

where approximation of  $R_F \ll a_{v0} r_\pi$  and  $r_b \ll r_\pi$  is used.

$$G_i(s) = \frac{i_{c3} + i_{c5}}{i_1} \approx \frac{g_{m3}(1 + s r_b C_{\pi 4}) - g_{m4}(1 + s r_b C_{\pi 3})}{g_{m3}(1 + s r_b C_{\pi 4}) \left(1 + s \frac{C_{\pi 3}}{g_{m3}}\right) + g_{m4}(1 + s r_b C_{\pi 3}) \left(1 + s \frac{C_{\pi 4}}{g_{m4}}\right)} \quad (\text{A.8})$$

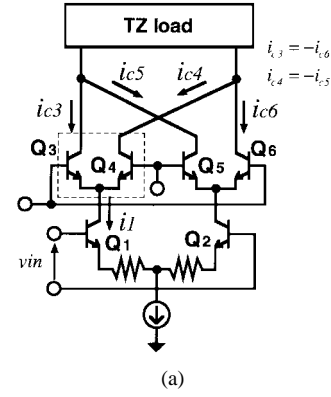


Fig. 14. Schematic of variable: (a) gain amplifier and equivalent circuit of the (b) gain-control circuit.

## APPENDIX II DERIVATION OF (2)

Fig. 14 shows the schematic of a variable-gain amplifier and an equivalent circuit of the gain-control circuit ( $Q_3$  and  $Q_4$ ). The following equations are obtained from the equivalent circuit:

$$\begin{cases} v_{be3} g_{m3} + v_{be4} g_{m4} + \frac{v_{be3}}{z_{\pi 3}} + \frac{v_{be4}}{z_{\pi 4}} = i_1 \\ \frac{v_{be3}}{z_{\pi 3}} = \frac{v_i}{r_b + z_{\pi 3}} \\ \frac{v_{be4}}{z_{\pi 4}} = \frac{v_i}{r_b + z_{\pi 4}} \end{cases} \quad (\text{A.7})$$

where  $z_\pi$  is  $r_\pi // C_\pi$ .

Approximating  $r_b \ll r_\pi$ , the current gain  $G_i$  is obtained from (A.7) as shown in (A.8) at the bottom of the page. Approximating  $C_\pi \approx g_{mi} \tau_F$

$$\begin{aligned} G_i(s) &= \frac{G_{i0}}{(1 + s \tau_F)(1 + s \alpha \tau_F)} \\ G_{i0} &= \frac{g_{m3} - g_{m4}}{g_{m3} + g_{m4}} \\ \alpha &= \frac{2g_{m3}g_{m4}}{g_{m3} + g_{m4}} r_b \end{aligned} \quad (\text{A.9})$$

$$G_R(s) = \frac{i_{cR}}{-v_i} = \frac{-g_{mR}r_{\pi R}(1 + 2sR_{ER}C_P)}{(r_{bR} + r_{\pi R} + g_{mR}r_{\pi R}R_{ER}) + s\{r_{bR}r_{\pi R}C_{\pi R} + 2(r_{bR} + r_{\pi R})R_{ER}C_P\} + 2s^2r_{bR}r_{\pi R}R_{ER}C_{\pi R}C_P} \quad (\text{A.11})$$

$$G_R(s) \approx \frac{g_{mR}(1 + 2sR_{ER}C_P)}{(1 + g_{mR}R_{ER}) + s(r_{bR}C_{\pi R} + 2R_{ER}C_P) + 2s^2r_{bR}R_{ER}C_{\pi R}C_P} = \frac{-G_{R0}\left(1 - \frac{s}{z_{R0}}\right)}{1 + s\left(\frac{2K_G}{\omega_{0G}}\right) + \frac{s^2}{\omega_{0G}^2}}$$

$$G_{R0} = \frac{g_{mR}}{1 + g_{mR}R_{ER}}$$

$$z_{R0} = -\frac{1}{2R_{ER}C_P}$$

$$\omega_{0G} = \sqrt{\frac{1 + g_{mR}R_{ER}}{2r_{bR}R_{ER}C_{\pi R}C_P}}$$

$$K_G = \frac{2R_{ER}C_P + r_{bR}C_{\pi R}}{2\sqrt{2r_{bR}R_{ER}C_{\pi R}C_P(1 + g_{mR}R_{ER})}} \quad (\text{A.12})$$

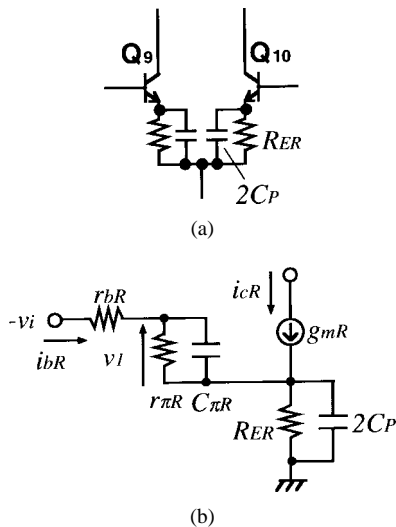


Fig. 15. Schematic of transconductance amplifier in the second variable: (a) gain stage and its (b) equivalent circuit.

is obtained. The  $-3$ -dB bandwidth of  $G_i$  is

$$\omega_{BWGi} = \frac{1}{\tau_F} \sqrt{\frac{\sqrt{(1 + \alpha^2)^2 + 4\alpha^2} - (1 + \alpha^2)}{2\alpha^2}}. \quad (\text{A.10})$$

### APPENDIX III

#### DERIVATION OF (4) AND (5)

Fig. 15 shows the schematic and equivalent circuit of the transconductance amplifier  $A_{GR}$  in the second variable-gain stage. The peaking capacitor  $C_P$  connected between the emitters of  $Q_9$  and  $Q_{10}$  is equivalent to twice of  $C_P$  connected in parallel with  $R_{ER}$ . The input voltage is  $-v_i$  because the input signal is input in inverse relation to another amplifier  $A_{GL}$ . The transconductance gain  $G_R$  is obtained from the equivalent circuit as shown in (A.11) at the top of the page.

Approximating  $r_{bR} \ll r_{\pi R}$ , (A.11) is reduced as shown in (A.12) at the top of the page.

The transconductance gain of another amplifier  $A_{GL}$  is obtained by substituting  $C_P = 0$  to (A.12)

$$G_L = \frac{G_{L0}}{1 - \frac{s}{p_{L0}}}$$

$$G_{L0} = \frac{g_{mL}}{1 + g_{mL}R_{EL}}$$

$$p_{L0} = -\frac{1 + g_{mL}R_{EL}}{r_{bL}C_{\pi L}}. \quad (\text{A.13})$$

#### ACKNOWLEDGMENT

The authors would like to thank K. Oda, R. Hayami, M. Tanabe, H. Shimamoto, and Dr. M. Kondo for their valuable discussions.

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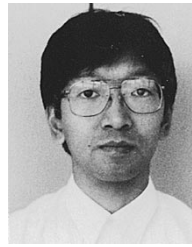
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