

A > 400 GHz  $f_{max}$  Transferred-Substrate HBT Integrated Circuit Technology  
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HBTs are used in Gb/s fiber-optic ICs, GHz analog-digital converters, and microwave PLLs. To permit clock rates exceeding 100 GHz, transistors with several hundred GHz bandwidth are required. The interconnects must have small inductance and capacitance per unit length, and the transistor spacings must be small to minimize wire lengths. Given that fast HBTs operate at  $\sim 10^5$  A/cm<sup>2</sup>, efficient heat sinking is then vital. We report here a transferred-substrate HBT IC technology with record HBT power-gain cutoff frequency ( $f_{max}$ ). The interconnects, microstrip on Benzocyclobutene (BCB), have a low ( $\epsilon_r = 2.7$ ) dielectric constant for low capacitance and a ground plane for low ground-return inductance. Transistor heatsinking is provided by electroplated gold thermal vias.

Obtaining high transistor bandwidths requires both vertical and lateral device scaling. In typical double-mesa HBTs, the transfer length of the base Ohmic contacts sets a minimum size for the base-collector junction, and hence the base-collector  $r_{bb}C_{cb}$  time constant is not appreciably reduced by device scaling. HBTs are consequently typically fabricated at 1-2  $\mu$ m emitter widths. By using a substrate transfer process, HBTs can be fabricated with narrow emitter and collector stripes aligned on opposing sides of the base epitaxial layer.  $r_{bb}C_{cb}$  becomes proportional to the process minimum feature size, and  $f_{max}$  increases rapidly with scaling [1].

In work reported earlier [2], die-attach epoxy was used for substrate transfer. Epoxy has low thermal conductivity, and the process was unsuitable for IC fabrication. In the present process, the transferred substrates are bonded to the carrier by In/Pb/Ag solder. A 13  $\mu$ m BCB dielectric layer between the Au plated ground plane and the wiring plane provides a low-loss, low dielectric constant (2.7) microstrip wiring environment. Thermal vias etched in the BCB provide a low thermal resistance path from emitter to ground plane. Device fabrication starts with conventional base-emitter processing, mesa isolation, polyimide passivation and planarization, and electroplated gold airbridges. This is followed by SiN insulator deposition, BCB deposition, dry via etch and Au electroplating. Transistor epitaxial layers with BCB and thermal vias are then bonded to the transfer substrate using In/Pb/Ag solder. The InP substrate is removed in HCl. Deposition of Schottky collector metal completes the process.

HBTs with 0.6  $\mu$ m emitters and 1.8  $\mu$ m wide collectors have an extrapolated  $f_{max} = 365$  GHz and  $f_t = 164$  GHz. The smallest devices fabricated have 0.6  $\mu$ m emitter and 0.8  $\mu$ m collector widths. While the microwave measurements reproducibly give extrapolated  $f_{max}$  above 500 GHz for the smaller devices, such measurements are at the limits of reliability for a DC-50 GHz instrument.  $f_{max}$  estimated by hand calculation from known values of  $f_t$ ,  $C_{cb}$ , and base sheet resistance is 400-450 GHz. We therefore conclude that  $f_{max}$  is in excess of 400 GHz for the 0.8  $\mu$ m collector devices.

[1] U. Bhattacharya et al, Electron. Lett., vol. 32, p. 1405-1406, July 1996.

[2] B. Agarwal et al, Conference on Indium Phosphide & Related Materials, May 1997.

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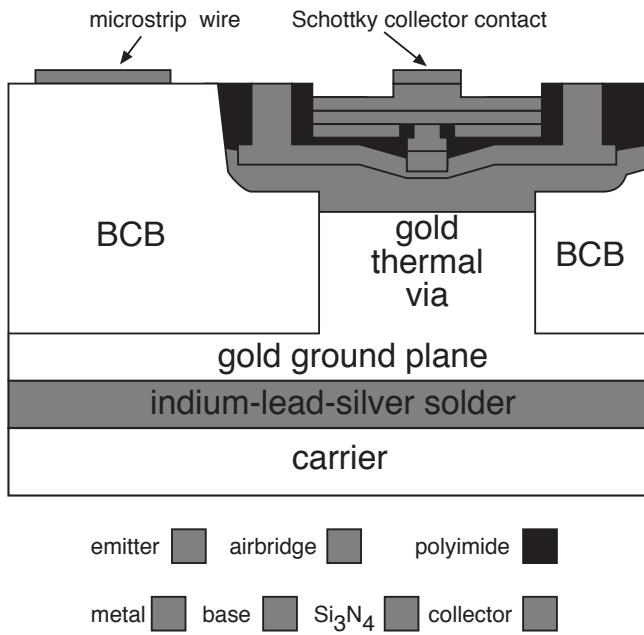


Fig. 1 Schematic cross-section

InAs 250 Å 3·10 <sup>19</sup> Si	emitter
GaInAs 250 Å 3·10 <sup>19</sup> Si	
GaInAs 500 Å 1·10 <sup>19</sup> Si	
Grade 67 Å	
AllnAs 834 Å 1·10 <sup>19</sup> Si	graded base
AllnAs 500 Å 8·10 <sup>17</sup> Si	
Grade 300 Å	
GaInAs 400 Å 5·10 <sup>19</sup> Be	collector
GaInAs 100 Å 3·10 <sup>19</sup> Be	
GaInAs 400 Å 2·10 <sup>16</sup> Si	
GaInAs 50 Å 1·10 <sup>18</sup> Si	buffer
GaInAs 2300 Å 1·10 <sup>16</sup> Si	
AllnAs 1000 Å	
S. I. InP	

Fig. 2 Layer Structure

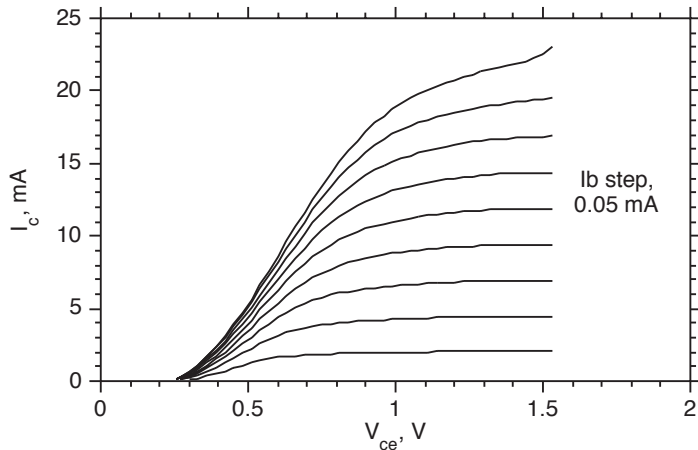


Fig. 3 DC common-emitter characteristics of device with 0.6 X 25 μm<sup>2</sup> emitter and 0.8 X 29 μm<sup>2</sup> collector

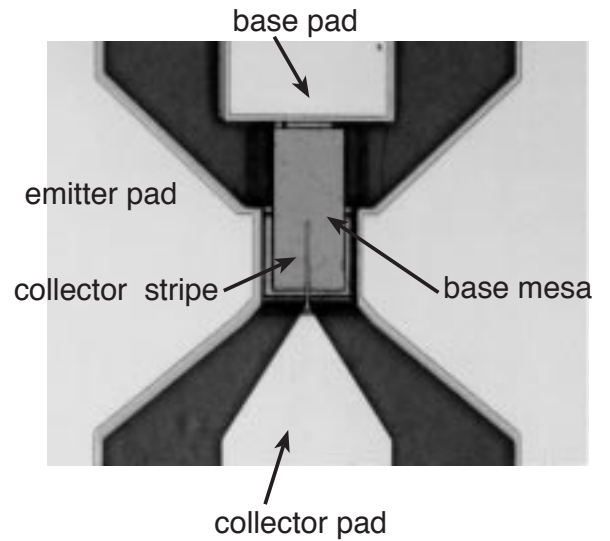


Fig. 4 Photograph of HBT

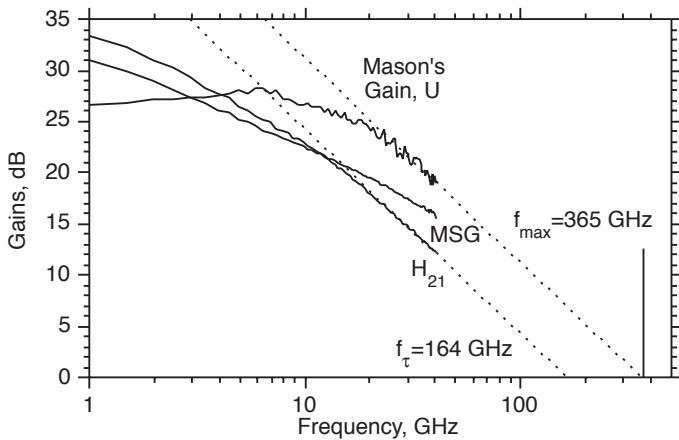


Fig. 5 RF characteristics of 0.6 X 25 μm<sup>2</sup> emitter, 1.8 X 29 μm<sup>2</sup> collector device biased at I<sub>c</sub> = 18 mA and V<sub>ce</sub> = 1.0 V

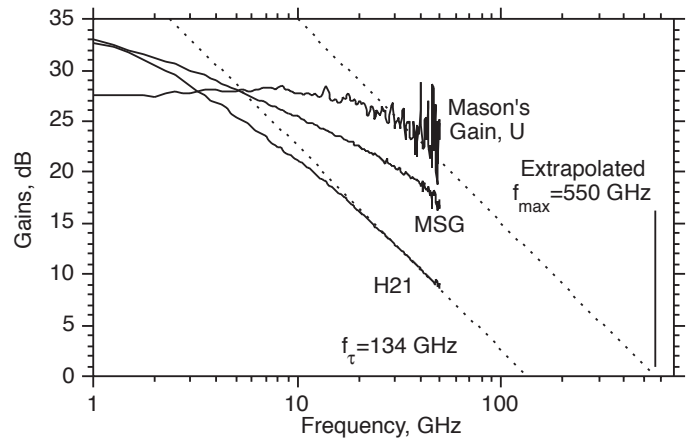


Fig. 6 RF characteristics of 0.6 X 25 μm<sup>2</sup> emitter, 0.8 X 29 μm<sup>2</sup> collector device biased at I<sub>c</sub> = 12 mA and V<sub>ce</sub> = 1.0 V