An InP HBT Low Power Receiver IC Integrating AGC Amplifier, Clock Recovery Circuit and Demultiplexer

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I. Introduction

There has been a growing importance of digital approach in implementing communication systems such as cellular phone, satellite-based data and video links. In addition to improving signal to noise ratio, digital implementation lends itself readily to monolithic integration which reduces system size and increases functionality. A typical digital receiver for a fiber optic data link, for example, is shown in Fig. 1. It consists of several functional blocks, each of which is conventionally implemented in one or more ICs [1]. It is highly desirable to integrate these functional blocks on one chip to reduce power and increase functionality.

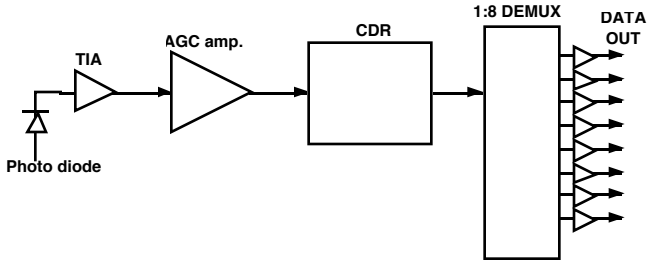

Figure 1. Functional block diagram of generic receiver for optical link.

We have developed a 2.5 Gb/s digital receiver IC in InP HBT technology that achieved a new level of functional integration and low power consumption. Our receiver IC monolithically integrates most of the blocks in Fig. 1, including an automatic-gain-control(AGC) amplifier, a digital clock and data recovery (CDR) circuit, and an 1:8 demultiplexer (DEMUX). It consumes only 340 mW power including nine CMOS-compatible output buffers, significantly lower than that of comparable functions implemented in Si-based technology [2]. This IC is uniquely suitable for satellite-based communication applications where low power and potential for higher data rate are important.

II. Circuit Design

The circuit was implemented with a very high speed InP-based HBT technology [3] utilizing 2 μm wide emitters. This technology allows us to implement both analog and digital circuits on the same substrate and from a single 3.3V supply. The AGC amplifier was designed with analog techniques for high sensitivity and high dynamic range requirements. The rest of the circuit was designed with digital techniques utilizing common mode logic. Differential signal lines were maintained throughout the whole circuit except between the loop filter and the voltage controlled oscillator (VCO), and at the data outputs.

A. AGC Amplifier

The integrated receiver included a wideband AGC amplifier, its schematic as shown in Fig. 2. The first stage was a variable gain-stage in the Gilbert-cell configuration. The second and third gain stages were DC-coupled emitter-coupled pairs with emitter-follower buffers, with the second stage employing transimpedance loading to increase the stage bandwidth. A full differential signal path was used.

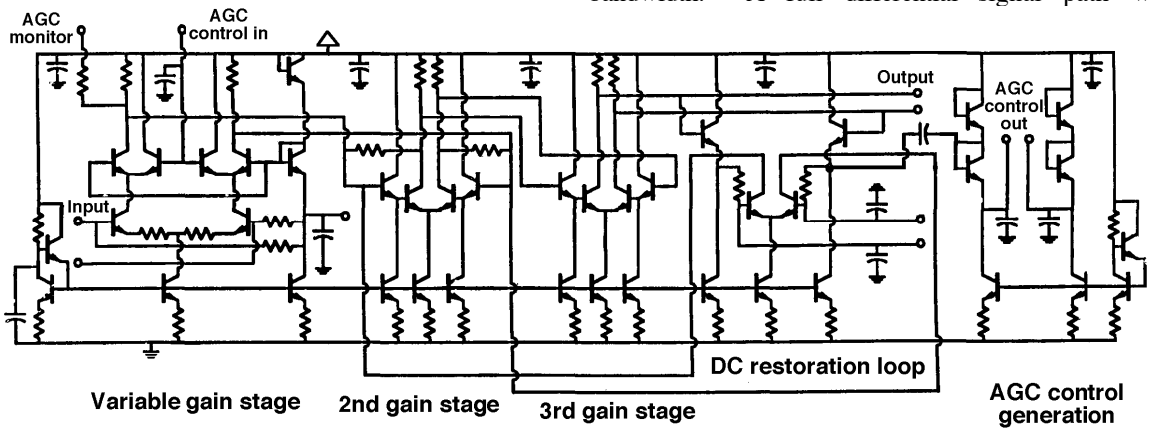

Figure 2. Schematic of AGC Amplifier.

DC balance in the circuit was maintained using a DC restoration loop between the output of the third stage and the input of the second stage. Control voltage for the variable-gain stage was provided by a differential full-wave rectifier implemented using four diode-connected transistors; the diodes were biased at 10 μA, reducing the AGC detector deadzone to 2kT/q. Bypass capacitors required in the AGC detector, the AGC loop, and the DC restoration loop were implemented off-wafer, with 1 pF per capacitor on the IC. To minimize power consumption, all gain transistors were operated at a low $2x10^4$ A/cm^2. This reduced transistor f_T and hence stage bandwidth.

B. CDR

The CDR consisted of a digital phase lock loop (PLL) and a decision circuit, as shown in Fig. 3. The PLL contained a phase detector, a loop amplifier/filter and a VCO [4]. The phase detector was the "bang-bang" type that consisted of two flip-flops, one for sampling the clock at the rising edges of the data and the other at the falling edges. No frequency detector was included in this design. The VCO, as shown in Fig. 4, was the multivibrator design that required no external tuning elements. An external tuning port was included that can vary the VCO frequency over a wide operating range. Fig. 5 shows the loop filter we used which was slightly different than the one in [4]. It had an active stage where the gain could be tuned to optimize the loop gain. Only one off-chip filter capacitor was needed to set the loop bandwidth. The decision circuit was made up of a single flip-flop. This CDR design used devices very efficiently, containing less than 90 transistors total.

C. DEMUX and Output Buffers

The DEMUX employed the tree-type architecture for low power consumption. Power was saved when the clock rate was halved for every stage the data moved through. The output buffers were designed for CMOS levels using a totem-pole configuration, as shown in Fig. 6. The output stage had its own power supply pad to isolate any switching noise from coupled back to the rest of the circuit. There were nine such output buffers, eight for the data and one for the clock.

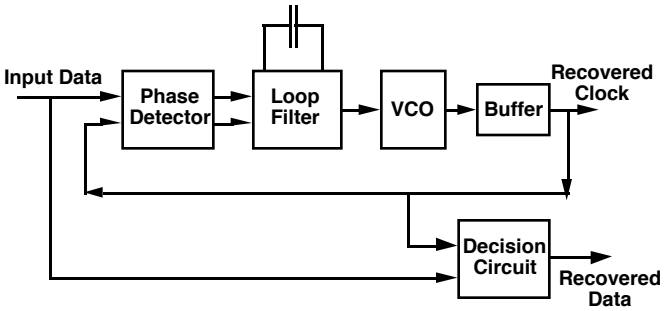

Figure 3. Block diagram of CDR.

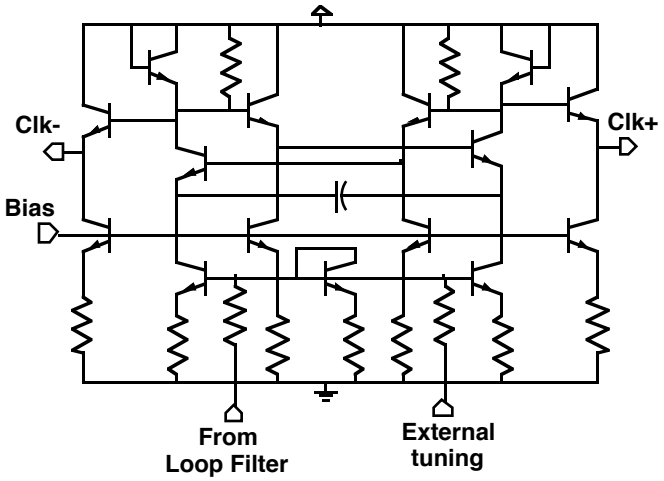

Figure 4. Schematic of VCO.

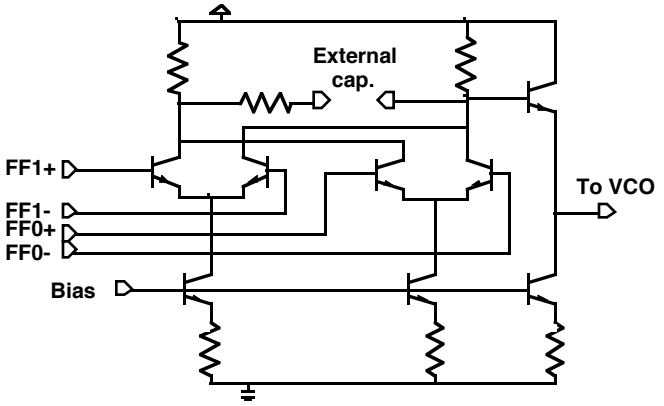

Figure 5. Schematic of loop filter.

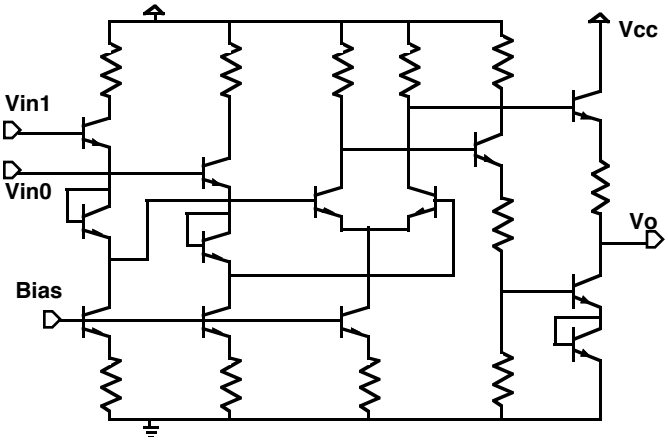

Figure 6. Schematic of Output Buffer.

III. EXPERIMENTAL RESULTS

The receiver IC has been successfully fabricated. Its photomicrograph is shown in Fig. 7. It measured 2.8 x 2.35 mm^2 and consisted approximately 550 transistors. Two

thirds of the area were occupied by the DEMUX and the output buffers. We have measured the performance of the receiver IC. The frequency response of the AGC amplifier is shown in Fig. 8. Maximum gain of about 28 dB and 2 GHz bandwidth were observed. Resonance between the external capacitors and probe inductance resulted in in-band resonance; these must be eliminated by damping resistors in subsequent design iterations. Power consumption of the AGC amplifier was about 20 mW.

The CDR exhibited satisfactory locking behavior. It had a lock-in range of about 30 MHz when locked at a 2.1 Gb/s data stream. Moreover, the locking frequency could be externally tuned over more than a 1-GHz span. When tested with a 2^7 -1 pseudo-random bit stream, the recovered data achieved a bit-error-rate of less than 10^{-12} with 9.6 ps rms jitters. The eye diagram of these recovered data is shown in Fig. 9. The CDR portion of the chip consumed about 90 mW power.

The rest of the IC also performed properly. The data output voltage swing was about 800mV at 262 Mb/s. The power consumption of the whole chip was only 340 mW.

We have also obtained preliminary CDR results from another fab run where the transistor was shrunk to 45% and the resistors adjusted accordingly. The circuit functioned with power consumption reduced by a factor of more than 3.

IV. SUMMARY

We have successfully designed and fabricated a highly integrated and very low power receiver IC for 2.5 Gb/s optical communication application. It consisted of an AGC amplifier, a clock and data recovery circuit and a demultiplexer, and consumed only 340 mW power. The measured data have validated our design approach and have demonstrated the potential of the InP HBT technology to integrate analog and digital functions for low power and high speed applications. Achieving even lower power is feasible through device scaling. Additional functionality such as multiple data rate, frequency detection, lock indicator and data decoder can be included in future integration.

REFERENCE

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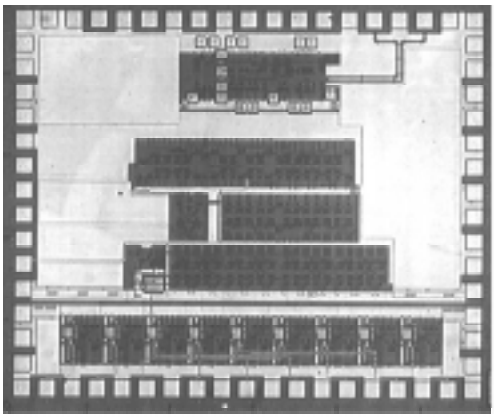

Figure 7. Photomicrograph of integrated receiver IC

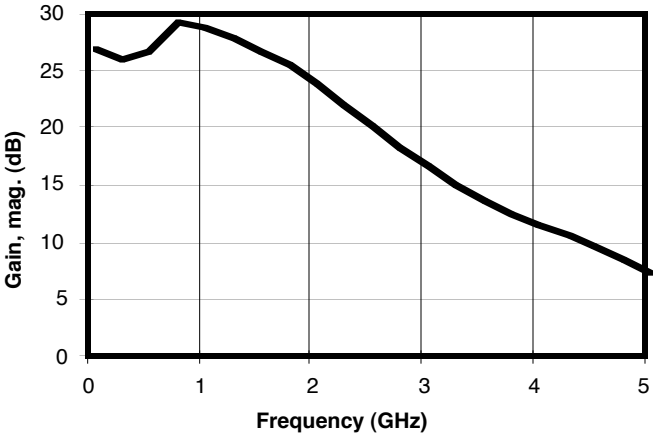

Figure 8. Frequency response of AGC Amplifier

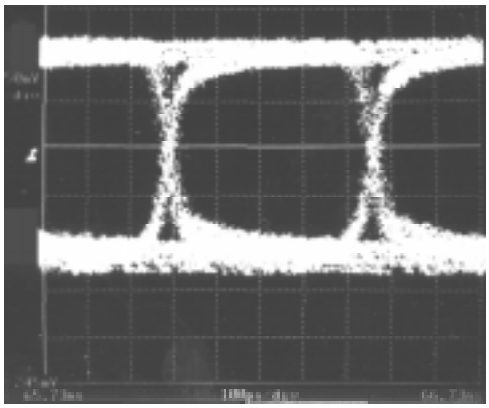

Figure 9. Eye diagram of recovered 2^7 -1 PRBS data of CDR with 9.6ps rms jitters