InP-Based High Sensitivity *pin* / HEMT / HBT Monolithic Integrated Optoelectronic Receiver

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Abstract

We report the first successful demonstration of a *pin* diode/HEMT/HBT monolithic integrated optoelectronic receiver lattice-matched on InP substrates for multi-gigabit long wavelength applications. Our approach utilizes a stacked single layer MBE growth of HEMTs and HBTs after which the HBT layers are patterned and selectively wet etched to expose the HEMT layers. The subsequent process steps feature HEMTs with 0.12 µm T-gates, HBTs with 2 µm emitter fingers, TaN thin-film resistors, SiN MIM capacitors, and photodetector antireflection coatings. The *pin* photodiodes comprise the base-collector junctions of the HBTs and thus are fabricated at the same time as the HBTs. The receiver circuit utilizes a high-gain three stage amplifier within the transimpedance feedback loop with a HEMT front end. The high f_T of the HEMT and the fully monolithic fabrication together with the photodiode and the HBTs result in a very small input node capacitance and low noise. A flat transimpedance gain of ~ 6 kΩ with a bandwidth of 2.5 GHz is observed for supply voltages between 2.8 - 3.0 V. Circuit operation up to 7 Gb/s is obtained with an input PRBS length of 2^7-1. At 10^{-9} *BER*, sensitivities of -24.7, -21.2 and -18.5 dBm are observed for 2.5, 4 and 7 Gb/s operation respectively. At 2.5 Gb/s, a very good photocurrent sensitivity (ηP) of -27.9 dBm is measured.

I. Introduction

There has recently been a great deal of interest in achieving high performance, high bit-rate optoelectronic receivers in a monolithically integrated form [1-4]. We hereby pursue an approach to such a receiver by integrating a *pin* diode, a HEMT and HBTs in a transimpedance amplifier configuration. Previous approaches to HEMT/HBT integration have used selective MBE [5, 6] and pre-patterned substrates before MBE growth [7]. In the process reported here, however, HBT layers are patterned and selectively wet etched to expose the HEMT layers after the MBE growth is completed [8].

II. Growth and Fabrication

The stacked layers were grown in a Perkin Elmer 430 MBE system, where the growth temperatures were adjusted in order to obtain a good mobility in the HEMTs and to avoid Be diffusion in the HBTs (Fig. 1). The process starts with defining the HEMT areas by first etching the HBT layers with a citric acid solution into the AlInAs buffer and then selectively etching the AlInAs buffer with an HCl solution to stop on the GaInAs cap of the HEMTs. Subsequent steps are a combination of our standard HEMT and HBT processes [9-11]. First, discrete, 0.12 x 50 µm^2, T-gate HEMTs are processed and passivated. This is followed by the HBTs and

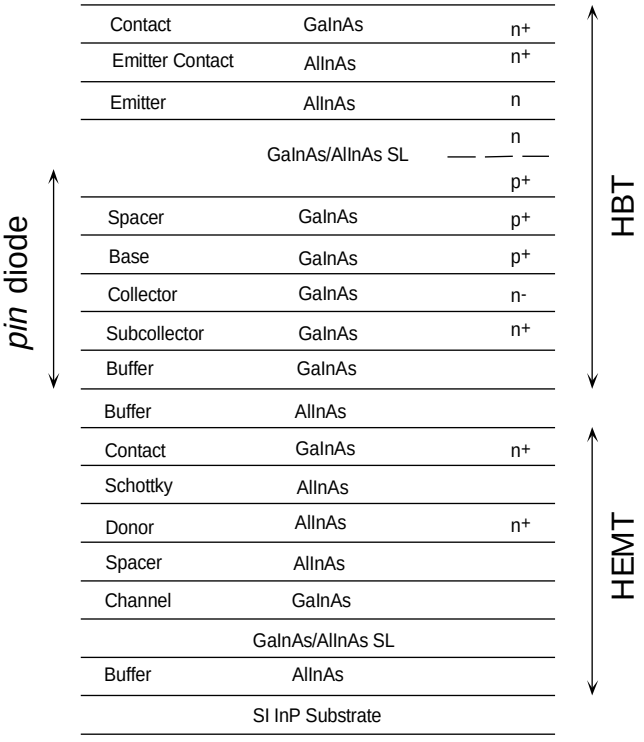


Fig. 1. HEMT/HBT stacked layer structure.

the passive elements (TaN thin-film resistors, SiN MIM capacitors). The *pin* diodes comprise the base-collector junctions of the HBTs and thus are fabricated at the same time as the HBTs. After the second interconnect metalization, photodiode windows are etched (15 µm in diameter) and SiO_x is deposited to provide an anti-reflective coating (Fig. 2).

Both the HEMTs and the HBTs showed dc and microwave performance comparable to our stand-alone discrete devices. HEMTs exhibited $g_{m,\,max}$ = 800 mS/mm and HBTs showed β = 50. S-parameter measurements performed during the fabrication on HEMTs within the receiver chip before final metalization yielded f_T = 110 GHz. 2 x 20 µm^2 HBTs biased at J_C = 25 kA/cm^2 had f_T = 75 GHz and f_{max} = 100 GHz. Standalone photodiodes fabricated on a control HBT-only wafer were also measured (Fig. 3). 15 µm photodiodes exhibited a responsivity (R) of 0.4 A/W and a 3 dB optical bandwidth of 16 GHz.

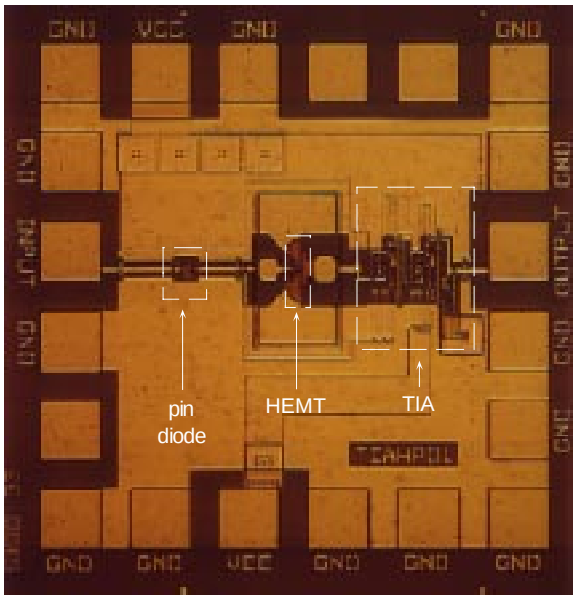


Fig. 2. Photograph of the integrated receiver chip.

III. Integrated Receiver

The receiver circuit utilizes a high-gain three stage amplifier within a transimpedance feedback loop (Fig. 4). The high f_T of the HEMT and the fully monolithic fabrication together result in a very small input node capacitance and low noise. The subsequent two Darlington feedback HBT amplifier stages set a sufficiently high gain to enable a 6 kΩ feedback resistance to be used, with the resistor's noise contribution minimized. Two HBT diodes are utilized in the feedback path for dc level shifting. An additional negative supply voltage is required to set the feedback bias as the HEMTs have a negative pinch-off voltage.

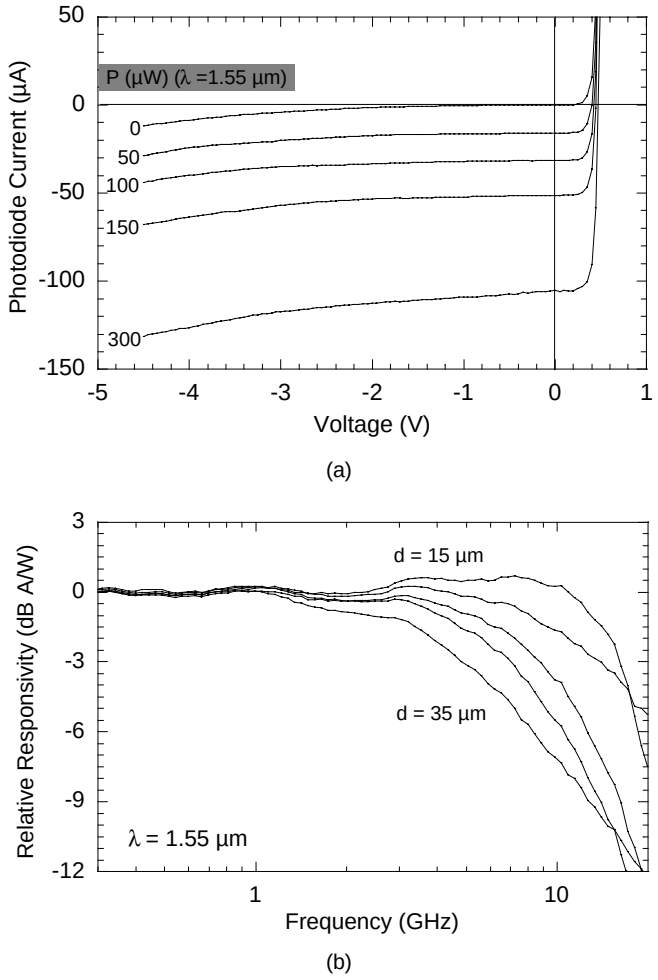


Fig. 3. (a) IV characteristics of an integrated *pin* diode (15 µm diameter) for varying intensities of received optical power (λ = 1.55 µm). (b) Frequency response of *pin* diodes with diameters of 15, 20, 25, 30 and 35 µm (-4 V bias, λ = 1.55 µm, both of the diode terminals terminated in 50 Ω).

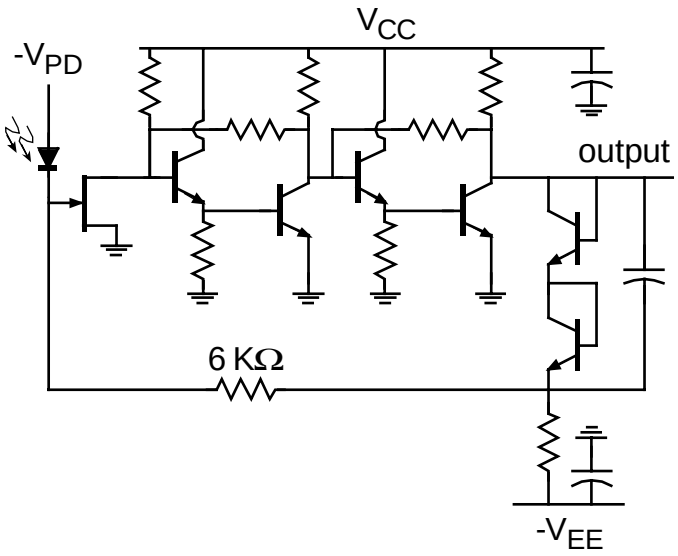


Fig. 4. Circuit diagram of the integrated receiver.

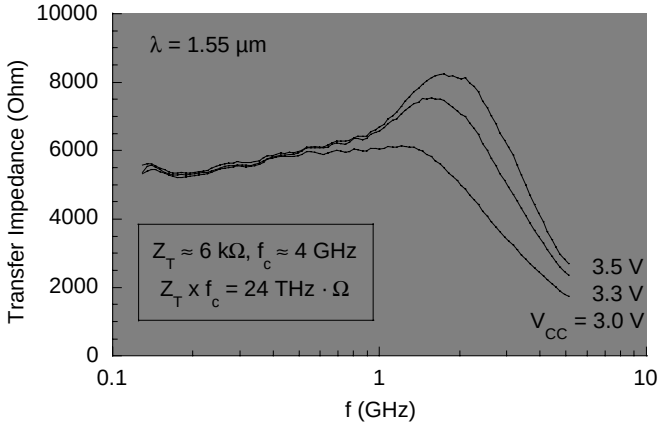
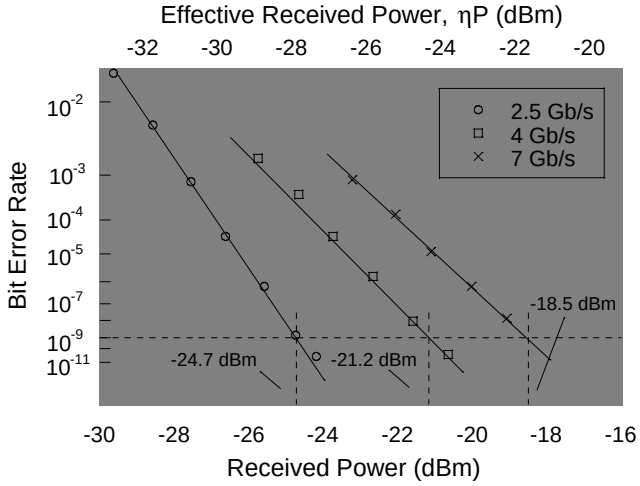


Fig. 5. Measured Z_T (= $Z_0 \cdot R_{out} / R_{diode}$) of the receiver.

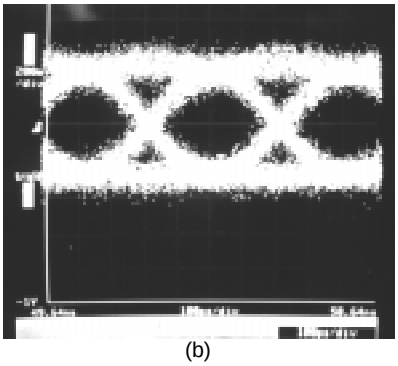
The transimpedance of the receiver was measured with an HP 8703A Optical Network Analyzer operating at 1.55 µm. A flat response and a bandwidth of 2.5 GHz was obtained for supply voltages (V_{CC}) between 2.8 - 3.0 V. When biased higher, high frequency peaking and a 4 GHz bandwidth was observed (Fig. 5). Bit error rate testing (BERT) was done on the receiver with an HP 79843A Error Performance Analyzer used in conjunction with a Lucent Technologies modulated laser diode. The output of the receiver was fed to a non-inverting 80 kHz - 6 GHz post-amplifier followed by a band-limiting filter. Circuit operation up to 7 Gb/s was obtained with an NRZ input PRBS length of 2^7-1 (Fig. 6). At 10^{-9} *BER*, sensitivities of -24.7, -21.2 and -18.5 dBm were observed for 2.5, 4 and 7 Gb/s operation respectively. At 2.5 Gb/s, a very good photocurrent sensitivity (ηP) of -27.9 dBm was also measured. We also observe that the slope of the *BER* vs. P_{rec} curves is lower than expected for a Gaussian distribution for the higher data rates. This is indicative of a data pattern dependent eye closure. Indeed, noting that the overall receiver is inverting and examining the eye pattern for the 7 Gb/s transmission, we observe that the eye closure predominantly occurs for an optical 1. We therefore suspect that this eye closure is due to the laser/modulator and not the receiver. The receiver was also tested with longer word lengths of 2^{15} -1 and 2^{31} -1 (Fig. 7). The small penalty that is paid in the sensitivity is likely due to gain variations in the overall transfer function of the system (receiver, post-amplifier and filter).

IV. Conclusion

In summary, we have shown the first demonstration of an optical receiver in InP system that, based on stacked layer MBE growth, monolithically integrates a *pin* diode, a HEMT and HBTs in a high sensitivity transimpedance amplifier configuration. With *pin*/HEMT/HBT integration, the receiver has the high loop gain required for a large feedback resistance and has very low input node capacitance. These are the parameters needed for high sensitivity. With reduction of HEMT gate and photodiode leakage currents and improved photodiode quantum efficiency, sensitivity is expected to be improved by 3-6 dB.



(a)



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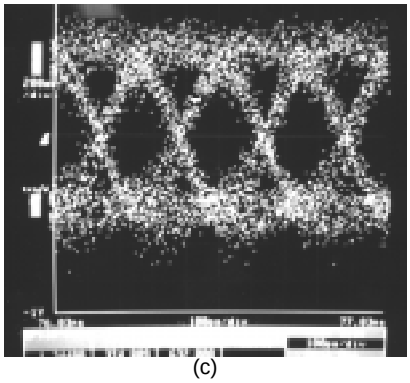
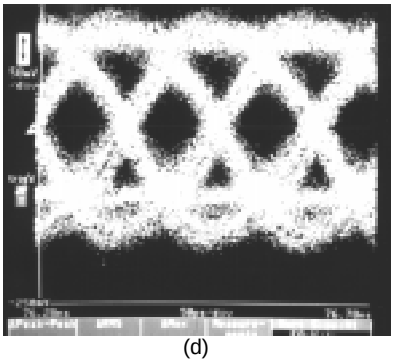


(c)



(d)

Fig. 6. (a) Receiver sensitivity curves for various bit rates for a PRBS length of 2^7 - 1 (λ = 1.55 µm). Eye diagrams for error-free operation at the bit rates of (b) 2.5 Gb/s, (c) 4 Gb/s and (d) 7 Gb/s are also shown.

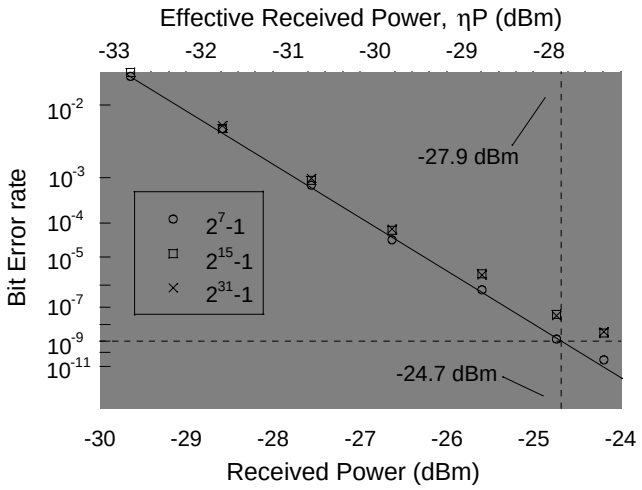


Fig. 7 Receiver sensitivity curves at 2.5 Gb/s transmission for varying PRBS word lengths.

V. Acknowledgment

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