Transferred-Substrate HBT Integrated Circuits

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Abstract— **Using substrate transfer processes, we have fabricated heterojunction bipolar transistors with submicron emitter-base and collector-base junctions, minimizing RC parasitics and increasing f_{max} to 500 GHz. The process also provides a microstrip wiring environment on a low-ϵ_r dielectric substrate. Demonstrated small-scale ICs in the process include lumped and distribute amplifiers with bandwidths to 85 GHz, 48 GHz static frequency dividers, and 50GHz AGC / limiting amplifiers.**

Keywords— **heterojunction bipolar transistor, HBT, transferred-substrate**

I. Introduction

APPLICATIONS –present & potential– for heterojunction bipolar transistors (HBTs) include RF/ microwave analog-digital conversion, microwave direct digital frequency synthesis, and fiber-optic transmission in the range of 40–120 Gigabits/second.

The motivation for high circuit bandwidth varies with the application. In fiber-optic transmission, fast ICs will directly enable increased time-division-multiplexed transmission rates, complementing increases in channel capacity provided by wavelength-division-multiplexing. For oversampled ($\Delta-\Sigma$) analog-digital converters, in-band quantization noise power decreases in proportion to the 5th power of the oversampling ratio (2nd-order modulators). Very high speed IC technologies offer the potential of $\Delta-\Sigma$ ADCs with clock frequencies in the 10's of GHz, providing high dynamic range –and large instantaneous bandwidth– over radio-frequencies and lower microwave frequencies. In direct digital frequency synthesis (DDS), increases in logic IC clock rates and DAC bandwidths will result in increased synthesizer bandwidth. Used in radar transmitters, modulation bandwidths can then be increased and frequency agility improved.

A 100 GHz clock rate IC technology would permit significant advances in the performance of such signal conversion ICs. To permit clock rates exceeding 100 GHz, significant issues in transistor design, interconnects, packaging, and thermal design must be addressed. The transistor current gain (f_τ) and power gain (f_{max}) cutoff frequencies must be several hundred GHz. Wiring parasitics must be minimized. The interconnects must have small inductance and capacitance per unit length, and the wire lengths, hence transistor spacings, must be small. Given that fast HBTs operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then essential. To provide predictable performance, interconnects of more than a few ps length must have a controlled characteristic impedance. To prevent circuit-circuit interaction through ground-circuit common-lead inductance ("ground loops"), the IC technology must provide an integral ground plane for ground-return connection. Similarly, to prevent circuit-circuit interaction between the IC's input and output lines, common-lead inductance between the IC and package ground systems must be made vanishingly small.

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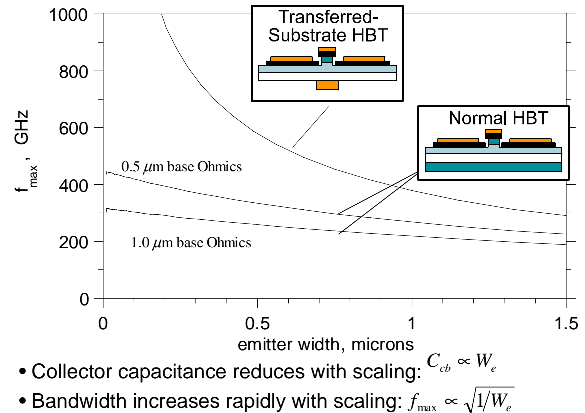

Fig. 1. Scaling of transferred-substrate and triple-mesa HBTs.

II. Transferred-Substrate HBTs

Transferred-substrate HBT ICs [3] offer high transistor bandwidth, low wiring capacitance, and low wiring inductance. In this process a substrate transfer step permits two-side processing of the device epitaxial layers, allowing definition of a transistor with narrow and aligned emitter-base and collector-base junctions.

In HBTs, f_τ is primarily determined by the base transit time τ_b, the collector transit time τ_c, and the emitter charging time $C_{je}(kT/qI_e)$. Increases in f_τ are obtained by thinning the collector, by thinning and grading the base, and by increasing the emitter current density. Unfortunately, thinning the base and collector epitaxial layers increases the collector capacitance C_{cb} and the base resistance R_{bb}, decreasing $f_{max}=(f_\tau/8\pi R_{bb}C_{cbi})^{1/2}$. The base-collector junction is a distributed network and $R_{bb}C_{cbi}$ represents an effective, weighted time constant [4]. *For a fixed emitter stripe length* , decreasing the width W_e of the emitter-base junction decreases the base spreading resistance, but does not decrease the base contact resistance. Scaling W_e

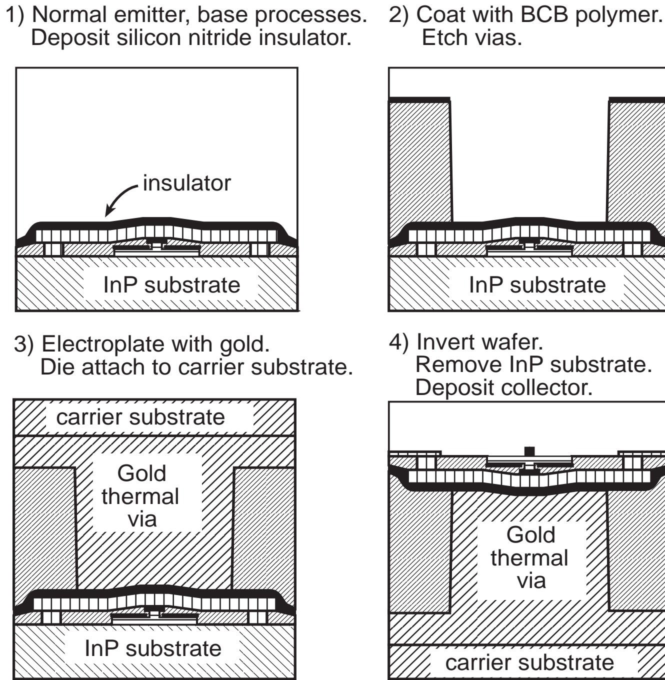

Fig. 2. Transferred-substrate HBT process flow.

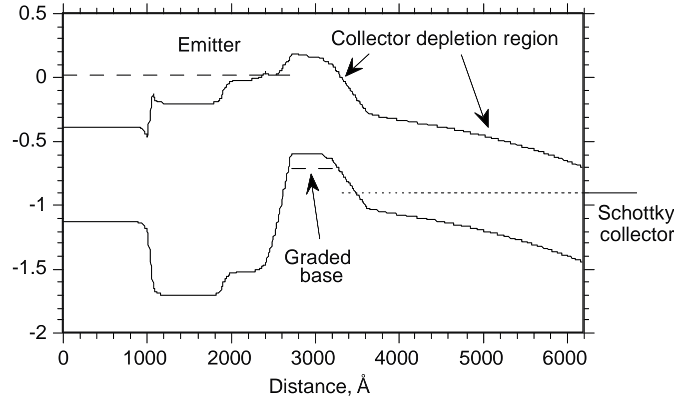

Fig. 3. Band diagram, under bias, of a typical device.

reduces R_{bb} towards a minimum set by the contacts. Decreasing the width of the base-collector junction W_c decreases C_{cb}.

In normal double-mesa HBTs (fig. 1), the collector-base junction and base Ohmic contact are defined in a single process step. The Ohmic contacts must be at least one contact transfer length, setting a minimum collector junction width, and a minimum collector capacitance. $R_{bb}C_{cb}$ has a minimum value, independent of lithographic limits, and f_{max} does not improve with scaling. In the transferred-substrate device, the collector width need only be larger than the emitter width. Reducing W_c and W_e progressively reduces $R_{bb}C_{cb}$, and f_{max} increases rapidly with scaling (fig. 1). With lateral scaling alone, f_{max} should approach 1 THz as dimensions are scaled to ~0.1 μm. Subsequently thinning the base and collector layers increases f_τ at the expense of f_{max}. Simultaneous high values for both f_τ and f_{max} are thus obtained.

III. Growth and Fabrication

Fig. 3 shows the band diagram associated with a typical transferred-substrate HBT layer structure. The InGaAs base is nominally 400-500 Å thick, has kT–$2kT$ bandgap grading, and is Be-doped at $5{\cdot}10^{19}/\text{cm}^3$. The InGaAs collector is 2500 Å thickness. A collector N^+ pulse-doped layer placed 400 Å from the base delays the onset of base pushout at high collector current densities. Devices typically use Schottky collector contacts [6], although HBTs with N+ subcollector layers (Ohmic-collector devices) have also been fabricated. While Ohmic-collector devices have non-zero collector series resistance, hence lower f_{max} [4], the 0.2 V barrier present in the Schottky-collector device increases the V_{ce} required to suppress base pushout at high current densities. Ohmic-collector devices thus show higher f_{max} under the low-V_{ce} conditions associated with current-mode-logic (CML). Schottky-collector devices are used for emitter-coupled-logic (ECL), where the operating V_{ce} is higher.

Figure 2 shows the process flow. Standard fabrication processes [2] define the emitter-base junction, the base mesa, polyimide planarization, and the emitter contacts. The substrate transfer process commences with deposition of the PECVD Si_3N_4 insulator layer and the Benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness). Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metalize the vias and to form the ground plane. Subsequently, the wafer is Indium-bonded to a GaAs carrier substrate, and the InP substrate removed in HCl. Schottky collectors are then deposited, completing the process.

The transferred-substrate process permits high device bandwidths f_{max} through simultaneous scaling of emitter and collector junctions. For the emitter-base junction, deep submicron scaling requires tight control of lateral undercutting during the base contact recess etch. To form the emitter, reactive-ion etching in CH_4 / H_2 / Ar, monitored with a HeNe laser, first removes the N^+ GaInAs emitter contact layer. A HCl/HBr/Acetic selective wet etch then removes the AlInAs emitter, stopping on the AlInAs/GaInAs emitter-base grade. By etching at 10° C, the etch rate is slowed, and a controlled emitter undercut is formed. The undercut both narrows the emitter and serves (as normal) to define the liftoff edge in the self-aligned base contact deposition. A timed 30 s non-selective wet Citric/H_3PO_4/H_2O_2 etch then removes the base-emitter grade. Etch selectivity in both the RIE and HCl/HBr/Acetic etches aids in etch-depth control, and we are able to reproducibly etch ~100 $\AA$ into the base without use of surface contact resistance probing as a process monitor. Figure 4 shows the cross-section of a 0.15-μm emitter-base junction.

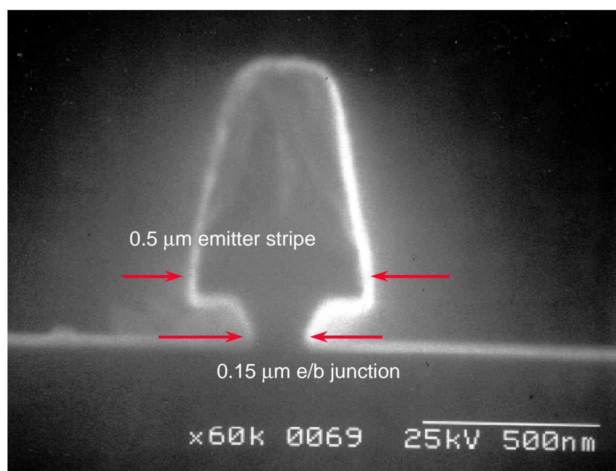

Fig. 4. Cross-section of emitter-base junction. The 0.5 μm emitter metal was defined with a projection lithography system.

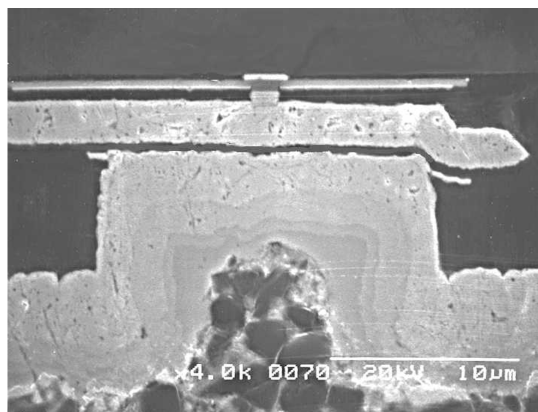

Fig. 5. Cross-section of a transferred-substrate HBT showing the thermal via..

In defining submicron collector-base junctions, use of the Schottky-collector contact eliminates the need for an etch of similar precision through an N^+ collector Ohmic contact layer. The collector junction is defined by the stripe width of the deposited metal. Subsequent to collector deposition, a self-aligned wet etch of ~1000 Å depth removes the collector junction sidewalls (eliminating fringing fields) and reduces the collector junction width by ~2000 Å. The step, intended to reduce C_{cb}, generally provides a greater increase f_{max} than would be expected from the observed reduction in collector junction width.

In addition to HBTs with narrow emitter and collector stripes, the process provides thermal vias for HBT heatsinking, NiCr resistors, Si_3N_4 MIM capacitors, and microstrip wiring on a ϵ_r=2.7 dielectric with vias, ground plane, and 3 levels of interconnects. To tolerate high power densities, the NiCr resistors must have thermal vias, which results in significant parasitic capacitance. Pull-up resistors in ECL do not require the thermal via.

A significant missing feature is in packaging. In the present process the microstrip ground plane is isolated from the wafer back surface by the GaAs transfer substrate, increasing thermal resistance and preventing low-inductance connections between the IC and package ground. A modified process with a fully metallic electroplated copper substrate is in development [5]. This will provide highly effective heatsinking (395 W/M · K for Cu vs. 74 for InP) and, with a package-IC ground interface over the full IC back surface, very low package-chip ground inductance. Presently, devices have been fabricated in the copper-substrate process (fig. 6) but difficulties with residual stress limit IC yield.

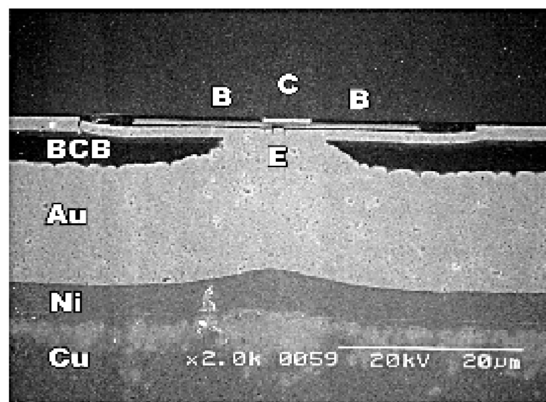

Fig. 6. Cross-section of a transferred-substrate HBT with a electroplated copper substrate.

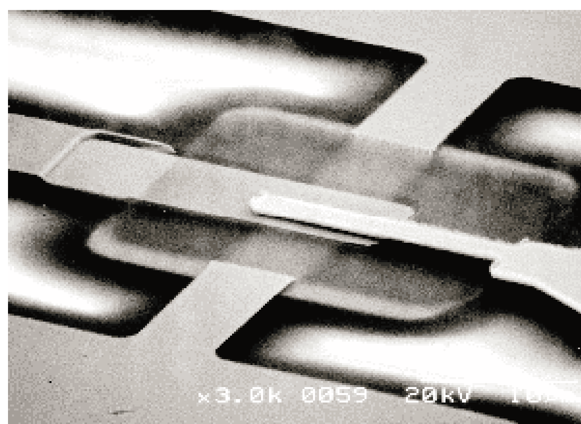

Fig. 7. Transferred-substrate HBT defined by contact lithography

IV. Device Performance

Devices have been fabricated using contact lithography at 1–2 μm resolution, using a 0.5 μm stepper, and using electron-beam lithography. Fig. 7 shows a device with a 0.6μm by 8μm emitter and a 1.6μm by 12μm collector. The device exhibits 215 GHz peak f_τ, and peak f_{max} above 400 GHz. Figure 8 shows HBT emitter-base and collector-base junctions defined by electron-beam lithography. Submicron devices fabricated by E-beam lithography (fig. 9) exhibit 500 GHz. f_{max} [7]. Neither contact lithography nor electron-beam lithography is suitable for fabrication of

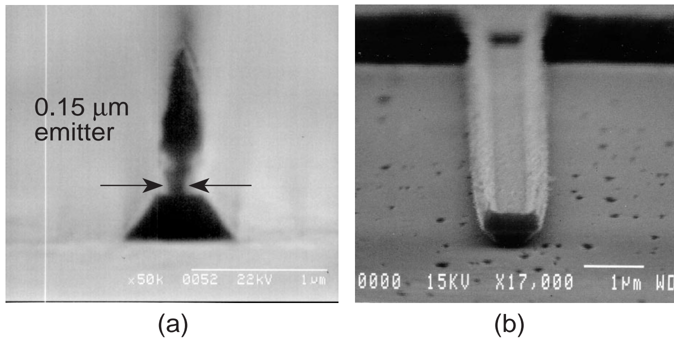

Fig. 8. E-beam HBT: test structure with 0.15 μm emitter-base junction (a), and 0.4 μm Schottky collector stripe (b)

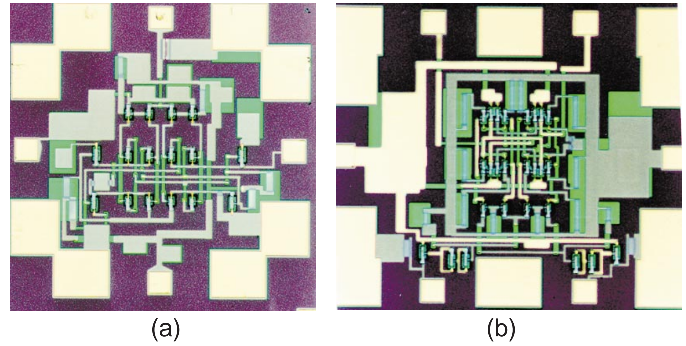

Fig. 10. CML (a) and ECL (b) master-slave D-flip-flops.

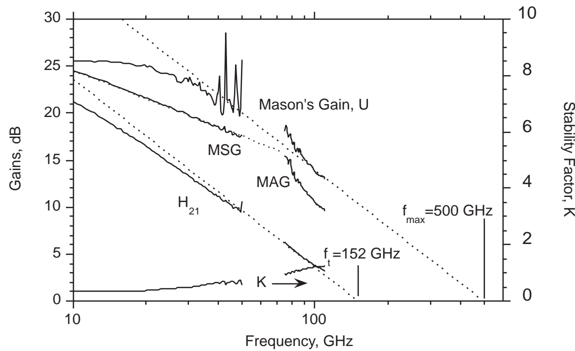

Fig. 9. W-band gains of device with a 0.4 μm × 25 μm emitter and a 1.0 μm × 29 μm collector.

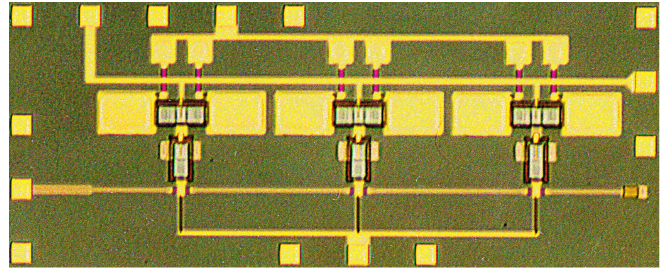

Fig. 11. Distributed amplifier in the transferred-substrate process. The amplifier exhibits 7 dB gain and 85 GHz bandwidth

large ICs. We have recently fabricated HBT ICs using a 0.5 μm projection lithography system, and have obtained microwave gains (and f_{max}) somewhat higher than that shown in fig. 9.

With the exception of reactively-tuned circuits, for which f_{max} is the sole determinant of circuit bandwidth, circuit design generally requires high values for both f_τ and f_{max}. Examining significant terms in $1/2\pi f_\tau$, with base bandgap grading, $\tau_b + \tau_c$ is small at 0.4–0.5 ps, while the Schottky collector eliminates $R_c C_{cb}$. At peak f_τ bias, $(C_{je} + C_{cb})/g_m \simeq 0.1$ps. Presently $R_{ex} C_{cb} \simeq 0.1$ ps, and has significant impact upon f_τ. To obtain $>$ 300 GHz f_τ, base bandgap grading must be increased, the collector thinned, and InAs emitter Ohmic contact layers employed.

Device scaling also reduces D.C. current gain and breakdown voltage. Base current in narrow-emitter InAlAs/InGaAs HBTs is predominantly due to conduction on the exposed InGaAs base surface between the emitter mesa and the base Ohmic contact. β decreases with emitter width, but increases as the base is thinned, as base bandgap grading is increased, and (at the expense of f_{max}) as the emitter-base spacing is increased. $\beta > 50$ has been obtained with 0.2 μm emitters. The 2500 Å InGaAs collectors have very low breakdown, 1.5 V BV$_{ceo}$, 2 V BV$_{cbo}$ *at* 1–2 $\cdot 10^5$ A/cm^2 *current density.* Clearly, InP collectors should be used for highly scaled devices.

V. Integrated Circuits

As first digital ICs demonstrations, we fabricated ECL and CML master-slave D flip-flops, configured as 2:1 static frequency dividers [8]. Circuits were fabricated using contact lithography, producing devices with 0.6 μm × 8μm emitters and 1.6 μm × 12 μm collectors. The devices operate at 1.25 mA/μm^2. The differential logic swing is 600 mV. The collector pull-up resistors are 50 Ω, hence the divider outputs directly drive 50 Ω output lines without buffering. Circuit design is entirely standard. The CML divider uses series-gated master and slave latches. Emitter-follower buffers are added to the CML clock and data ports to form the ECL divider. The ICs are shown in fig. 10

The CML and ECL static frequency dividers operated at maximum clock frequencies of 47 and 48 GHz. The circuits dissipate 380 mW (ECL) or 75 mW (CML) from a -5 V supply, and have pad-limited 0.6 mm × 0.6 mm die areas. The peak ECL clock speed of 70 GHz predicted from SPICE simulation (in which efforts were made to model all significant device and interconnect parasitics) does not correlate with the measured 48 GHz. We suspect this discrepancy arises from strong emitter-follower gain peaking at 50 GHz. We have observed very strong ∼ 50 GHz gain peaking –inconsistent with SPICE simulation– in resistive feedback amplifiers [9],[10], and have suppressed it with shunt resistive loading at the emitter-follower output [11]. Design studies now in progress suggest the feasibility of 100 GHz clock rates with the present HBTs, but the device models –and the circuits– remain to be validated.

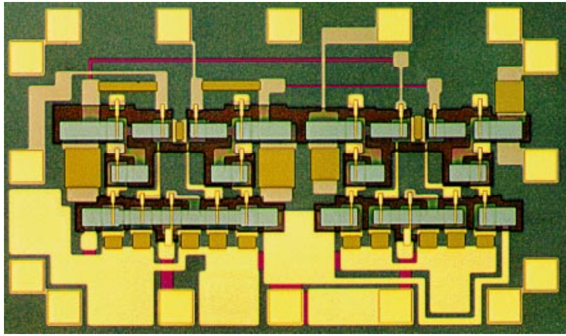

Fig. 12. DC-50 GHz, 11 dB broadband differential amplifier

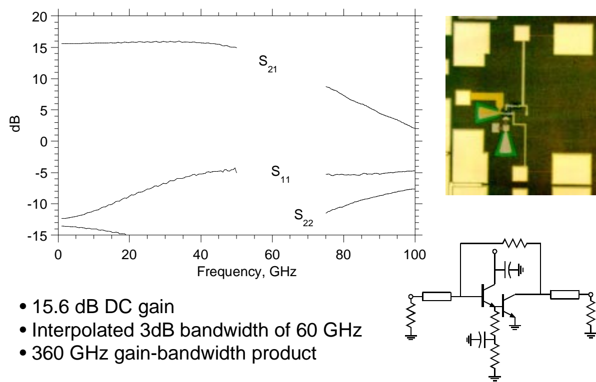

Fig. 13. Broadband Darlington feedback amplifier.

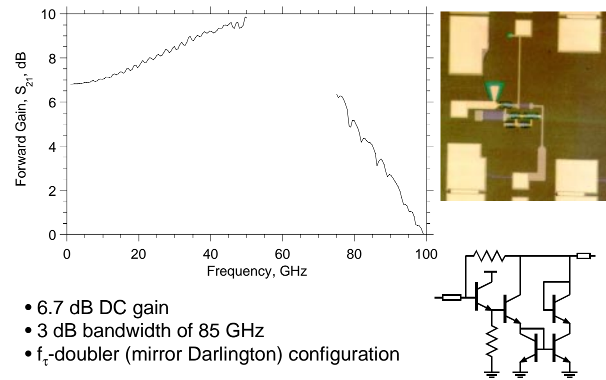

Fig. 14. Broadband feedback amplifier. The amplifier consists of a mirror f_τ doubler and emitter-follower input buffer.

Various analog ICs have been demonstrated in the process, including 85 GHz distributed amplifiers (fig. 11), 50 GHz broadband differential amplifiers for optical fiber receivers (fig. 12), broadband Darlington feedback amplifiers (fig. 13), and very broadband f_τ - doubler feedback amplifiers. (fig. 14).

VI. Conclusions

100 GHz digital ICs require a high-bandwidth transistor, low-parasitic interconnects, and effective heatsinking. Using substrate transfer processes, HBTs can be fabricated with highly scaled lithographic and epitaxial dimensions, giving both high f_τ and high f_{max}. With further scaling and improved circuit design, 100 GHz digital ICs will be feasible.

Acknowledgments

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