Transferred-Substrate HBTs with 250 GHz Current-Gain Cutoff Frequency

D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan, and M. J. W. Rodwell

Abstract—**We report improved current gain characteristics in the transferred-substrate HBTs, demonstrated by record current gain cutoff frequency f_τ of 254 GHz. This work compares device results from three wafers and points out the relative importance of the factors affecting f_τ and their impact on f_{max}.**

I. Introduction

ADVANCES in device technology for heterojunction bipolar transistors (HBTs) are necessary to further improve the performance of associated high speed analog and digital circuitry. The most commonly quoted figures of merit for these devices are current gain cutoff frequency, f_τ, and power gain cutoff frequency, f_{max}. The transferred-substrate process has already yielded very high f_{max}[1] HBTs, but has not yet offered record f_τ. While applications such as reactive tuned amplifiers and distributed amplifiers immediately benefit from high f_{max}, f_τ and f_{max} must both be considered for digital systems as well as many analog systems[2].

We herein report the simultaneous achievement of record f_τ and high f_{max} on one device, and compare that layer structure and process to two other recent device results in this process. The device parasitics can then be compared, and inferences made about the relative value of various approaches toward further improvements in f_τ and f_{max}.

The transferred-substrate process renders the HBT scalable, with device bandwidth that improves as the device area is scaled. A common concern in submicron bipolar technologies is the rapid loss of DC current gain as further scaling is performed. Improvements in current gain are therefore important as well as frequency performance. The ultimate utility of a highly scaled device should not be determined by DC current gain, but instead should only be limited by the capabilities of existing lithographic systems. We have achieved a significant increase in DC current gain of relatively conservative 1 μm emitter stripe geometry devices, which will translate to more useful values of current gain in highly scaled devices.

II. Processing and Fabrication

The wafers were grown on a Varian Gen II MBE system at UCSB on Fe-doped semi-insulating (100) InP substrates. The layer structures are as shown in Table 1. After completion of the collector growth sequence at 470°C, the wafer is cooled to 380°C to reduce beryllium outdiffusion during and after growth of the base[3]. A high As_2 flux

The authors are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA.

Layer	Material	Doping (cm^{-3})	Thickness (nm)	InGaAlAs %Ga/%Al
Cap				
	n InGaAs	1×10^{19}	100	47/0
	n InGaAs	1×10^{19}	6.6	47/0→0/48
	n InAlAs	1×10^{19}	83.4	0/48
Emitter				
	n InAlAs	8×10^{17}	50	0/48
A	n InGaAlAs	5×10^{17}	23.3	0/48→
B	n InGaAlAs	8×10^{17}	23.3	0/48→
C	n InGaAlAs	4×10^{17}	23.3	0/48→
	p InGaAlAs	2×10^{18}	6.6	→55/0
Base				
	p InGaAs	5×10^{19}	50(A)	55/0→47/0
	p InGaAs	5×10^{19}	40(B)	55/0→47/0
	p InGaAs	5×10^{19}	40(C)	58/0→47/0
Collector				
A	n InGaAs	1×10^{16}	25	47/0
B,C	n InGaAs	1×10^{16}	40	47/0
A	n InGaAs	5×10^{17}	5	47/0
B,C	n InGaAs	1×10^{18}	5	47/0
A	n InGaAs	1×10^{16}	170	47/0
B	n InGaAs	1×10^{16}	255	47/0
C	n InGaAs	1×10^{16}	155	47/0
Buffer	i InAlAs	UID	250	0/48

TABLE I
MBE Layer Structure. A, B, C refer to wafers A, B, C as discussed in text.

is also used to maximize beryllium as well as silicon incorporation. The compositional grading of the 400Å base is accomplished by eight 50Å "stairstep", referring to the downward steps seen by electrons in the conduction band as they traverse the base. After each 50Å step of base growth, the temperature of the gallium cell is increased to give a slightly wider bandgap $In_xGa_{1-x}As$ composition, followed by a two minute delay to allow stabilization of the gallium flux. The change in the bandgap is calculated assuming constant density of states and neglecting the effects of the tensile strain[4]. The base-emitter grade is an InGaAs/InAlAs superlattice[5], which the table represents as an average effective composition. The composition of the InGaAs in the grade is the same as that at the base-emitter edge, the base-emitter grade is therefore strained. After growth of the InAlAs emitter and heavily doped InAlAs transition layer, there is a short superlattice to smooth out the conduction band discontinuity at the interface between the InAlAs and the InGaAs cap.

The details of the transferred-substrate process have been enumerated in previous publications[1]. The motivation for the transferred substrate process is the freedom to process both sides of the epitaxial film, allowing lithographic definition of the emitter and the collector. This

yields rapid improvement in f_{max} as the emitter and collector dimensions are scaled. This lateral scaling can be accompanied by an appropriate vertical scaling, thinning of the semiconductor layers to reduce transit time. In this way, a reasonable f_{max}/f_τ ratio can be maintained.

This transferred-substrate process provides a microstrip-wiring environment via a plated ground plane and the low-loss, low dielectric constant (ϵ_r=2.7) spin-on dielectric benzocyclobutene (BCB). In this work, two different thicknesses of BCB were used, with wafer A using a 9 μm thick layer and wafers B and C using a 4.7 μm thick layer. The thinner BCB allows more densely packed interconnect lines and transistors, and is also easier to pattern and etch. Benchmark circuits such as the Darlington amplifiers often require minimal parasitic capacitance from the input/output pads and interconnect lines, and for this reason the thicker BCB is sometimes used[6]. NiCr resistors are used in the circuits with a 50 Ω/square sheet resistance. SiN based MIM capacitors are realized with a 0.45 μm thick SiN giving an estimated 0.128 fF/μm^2. A schematic of a completed transferred substrate process HBT is shown in figure 1.

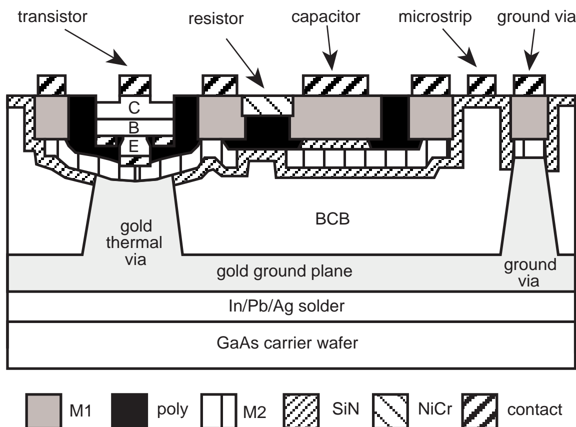

Fig. 1. Schematic of completed transferred-substrate process

Two performance-enhancing aspects of the process warrant discussion. These are the undercut of the emitter and the collector recess etch. The base contact etch, described elsewhere, is a methane/hydrogen/argon RIE etch, followed by a selective wet etch and a nonselective wet etch. The emitter has lithographic dimensions of 1 × 8 μm. The 1 μm emitter width is substantially undercut during the selective wet etch, as the etch attacks the InAlAs emitter but not the InGaAs in the cap layer. The amount of undercut is controlled by the time the wafer is immersed in the selective etch. For this work the intrinsic emitter is undercut to dimensions close to 0.6 × 8 μm. The reduced intrinsic emitter dimensions result in a lower base-emitter depletion capacitance (C_{je}). For this work the reduced C_{je} results in higher f_τ since the maximum useful current densities are limited by Kirk effect in the collector. The extrinsic emitter resistance R_{ex} is affected little by the undercut because it is dominated by the contact resistance at the metal-semiconductor interface. Excessive emitter undercut would reduce f_{max}, however, due to increased sheet resistance for holes traveling between the base contact and the intrinsic emitter.

The final step in the process is the self-aligned recess etch of the collector. The collector semiconductor is blanket etched in nonselective citric acid solution in order to remove collector semiconductor to some depth surrounding the collector contact. This recess etch of the collector is done to allow the microstrip like fringing fields between the narrow collector contact and the base to pass through low dielectric constant material (air) instead of the high dielectric constant semiconductor.

An improvement over previous designs is the reduction in the size of the base mesa. As a result of this, the overlap of the M1 and M2 layers, which contributes to C_{be}, has been reduced by a factor of 4. The M1 and M2 layers are separated by approximately 8000Å of polyimide. For the mesa associated with a 1 × 8 um device, the reduction of C_{be} due to decreased overlap is from 8 fF to about 2 fF. This is a substantial improvement considering the active mode Cje usually lies between 25 and 45 fF for this size of a device. The smaller mesa is possible due to the switch from plated airbridges to evaporated airbridges. A large mesa was required for the plated airbridge process in order to accomodate the post layer and the airbridge layer as well as alignment tolerances for each of them. The incorporation of evaporated airbridges has eliminated the need for this post layer.

Accurate determination of device parameters such as C_{je} requires knowledge of the parasitics introduced by the GSG probe pads. Measurement of similar open pad test structures allows determination of this pad capacitance. This capacitance is then subtracted off of the measured S-parameters allowing calculation of device parameters. The input and output pads on devices fabricated with the thinner BCB have capacitances on the order of 25 fF, while those with thicker BCB have 5-10 fF capacitance. The pad capacitance varies somewhat between process runs due to small changes in the thickness of BCB spun on and the etch time. The pad capacitance is therefore measured on each wafer with test structures consisting only of pads of the same shape, size and spacing as they appear on a device. The pad capacitance is not simply inversely proportional to the BCB thickness because some pad capacitance is present on the cal standards used in calibration of the network analyzer. This amount of capacitance is calibrated out for subsequent measurements.

III. Device Results and Discussion

A simplified hybrid-pi model for the bipolar transistor is shown in figure 2. The parameters R_{bb} and the split between $C_{cb,intrinsic}$ and $C_{cb,extrinsic}$ are discussed elsewhere[1]. The terms in the expression for f_τ are compared and discussed. All devices in this work are comprised of 1 × 8 μm emitter contacts prior to the base contact etch and 2 × 12 μm Schottky collector contacts. For this reason, the contribution to delay from R_{coll} has been neglected.

The values of these terms are summarized for the three

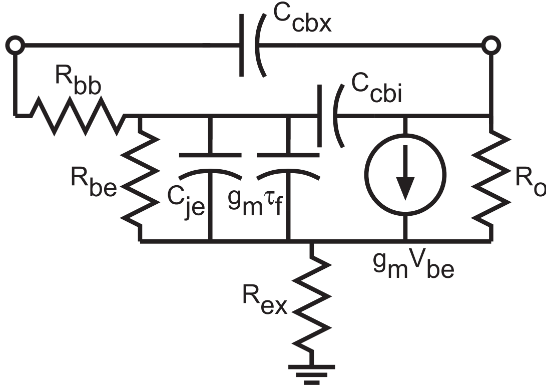

Fig. 2. Hybrid-Pi model of bipolar transistor.

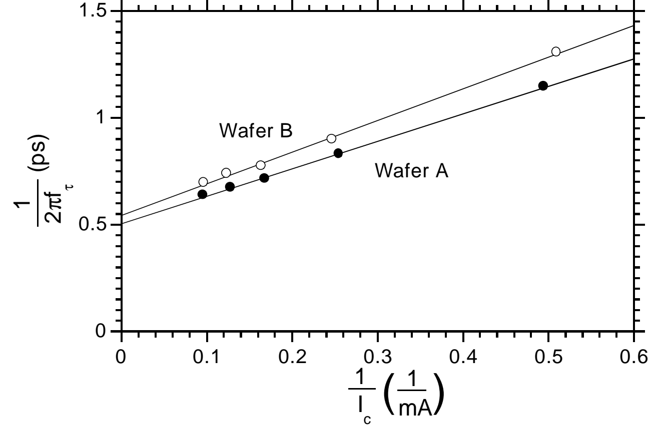

Fig. 3. Forward Delay vs inverse emitter current. Calculation of transit time and Cje.

wafers in table 2, and for those terms that depend on r_e, the emitter current taken was 10 mA for Wafers A and B, and 8 mA for Wafer C since it exhibited significant Kirk effect at 10 mA. C_{cb} has been extracted from the slope of the imaginary part of Y_{12}. R_{ex} was taken from the zero intercept of the plot of $1/\mathrm{Re}(Y_{21})$ vs $1/I_e$. $\tau_b + \tau_c$ was determined from the zero intercept of $1/(2\pi f_\tau)$ vs $1/I_e$ with $R_{ex}C_{cb}$ subtracted off, and C_{je} was determined from the slope of that plot with C_{cb} subtracted off. The data for extraction of forward transit time and C_{je} is plotted in figure 3 for Wafers A and B. The reduced forward transit time and C_{je} for Wafer A as opposed to Wafer B are readily seen. The reduction in C_{je} is expected due to the lighter doping in the base-emitter grade.

	$\tau_b + \tau_c$	r_eC_{cb}	r_eC_{je}	$R_{ex}C_{cb}$	peak f_τ
A	0.41 ps	.045 ps	.084 ps	.092 ps	254 GHz
B	0.49 ps	.022 ps	.13 ps	.052 ps	229 GHz
C	0.41 ps	.059 ps	.09 ps	.11 ps	236 GHz

TABLE II
Comparison of terms in f_τ.

The RF results for the device on Wafer A are shown in figure 4. This bias point yielded the highest simultaneous values of f_τ and f_{max}. The value of 254 GHz for f_τ is the highest yet for a bipolar transistor. The peak f_{max} is 233 GHz. Wafer B yielded somewhat lower f_τ, peaking at 229 GHz, but peak f_{max} was over 400 GHz. This is expected as Wafer B had a thicker collector, resulting in lower C_{cb}, but higher τ_c, collector transit time. Wafer C showed a peak f_τ of 236 GHz at $V_{ce} = 1$V and $I_c = 8$mA, and peak f_{max} of 244 GHz at that same bias point. Increasing the current beyond 8 mA for this device did not increase f_τ and decreased f_{max}. The degradation in f_{max} beyond 8 mA can be explained by the rise in C_{cb} with current, due to base pushout. This device appears to exhibit a lower Kirk threshold (about 8 mA) than Wafers A and B, which exhibited Kirk effect at about 11 and 12 mA, respectively. This was not expected since Wafer C effectively has strong pulse doping in the collector and a thin (2000A) collector depletion region. The pulse doping in the collector introduces a strong electric field near the base which should delay the onset of Kirk effect. It is possible that this electric field introduced by the pulse doping is sufficient to transfer electrons to the L valley, decreasing the electron velocity. Analysis of the Kirk effect threshold current density is complicated by the fact that the beryllium diffusion profile from the base into the collector is unknown, and may vary from growth to growth.

F_τ is generally increased by thinning the semiconductor layers to reduce the transit time. In addition to the increase in R_{bb} expected with a thinner base layer, the base thickness cannot be arbitrarily reduced without incurring serious processing and yield penalties. Thinning the collector semiconductor from several thousand angstroms to 1000 Å presents little processing difficulty. However, the above data shows that this reduction in transit time comes with a serious reduction in f_{max}. The f_{max} drops much faster as the collector is thinned than $C_{cb} = \epsilon A/d$ would predict.

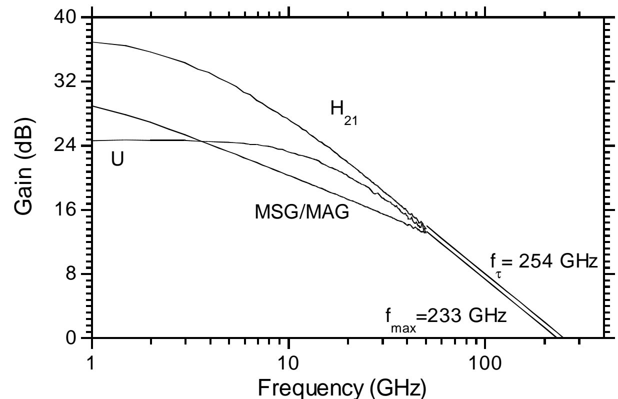

Fig. 4. Current Gain, Maximum Stable Gain, and Mason's Unilateral gain for device from Wafer A. Vce=1.0 V, Ic = 10 mA.

Additionally, as the collector semiconductor is thinned, increases in f_τ due to reduced τ_c are offset by an increasing $R_{ex}C_{cb}$ time constant.

The transferred-substrate process allows for narrowing the collector finger to reduce C_{cb}. Proportionally reducing the widths of the collector and emitter stripes reduces $R_{bb}C_{cb}$, allowing high f_{max} to be obtained in device layer structures that have the thin collectors necessary for high f_τ. *Decreasing* the ratio of collector to emitter stripe widths reduces $R_{ex}C_{cb}$, as well as further increasing f_{max}. But decreasing this ratio will reduce the Kirk effect threshold; this will lead to a compromise in which sufficient Kirk threshold must be maintained to support high current density with a narrow enough collector to provide high f_{max}.

IV. Results and Conclusions

The transferred-substrate process has yielded devices with record current gain cutoff frequency as well as high f_{max}, and is in a unique position to realize more dramatic improvements. The next step to further improve both f_τ and f_{max} is to reduce the ratio of the width of the collector finger to the width of the emitter finger. Further reduction in C_{je} is under investigation. The acquisition of a stepper alignment tool will allow for reduction in the base mesa size and all alignment tolerances. With this lithographic capability the transferred-substrate HBT should advance markedly in frequency performance.

Acknowledgments

These results would not have been possible but for the guidance of Bipul Agarwal, now at Rockwell Semiconductor Systems in Newport Beach, and Raja Pullela, now at Lucent Technologies. This work was supported by the ONR under grant N00014-98-1-0068.

References

[1] Q. Lee, B. Agarwal, D. Mensa, R. Pullela, J. Guthrie, L. Samoska, and M. J. W. Rodwell, "A > 400 GHz f_{max} transferred-substrate heterojunction bipolar transistor IC technology", *IEEE Electron Dev. Lett.*, vol. 19, pp. 77-79, 1998.

[2] E. Sano, M. Yoneyama, S. Yamahata, and Y. Matsuoka, "InP/InGaAs double-heterojunction bipolar transistors for high-speed optical receivers", *IEEE Transactions on Electron Devices*, vol. 43, No. 11, pp. 1826-1832, 1996.

[3] M. Hafizi, R. Metzger, and W. Stanchina, "Dependence of DC current gain and fmax of AlInAs/GaInAs HBTs on Base Sheet Resistance", *IEEE Electron Dev. Lett.*, vol. 14, No. 7, pp. 323-325, 1993.

[4] K. Kurishima, H. Nakajima, S. Yamahata, T. Kobayashi, Y. Matsuoka, "Effects of a Compositionally Graded $In_xGa_{1-x}As$ Base in Abrupt-Emitter InP/InGaAs Heterojunction Bipolar Transistors", *Japanese Journal of Applied Physics*, vol. 34, pp. 1221-7, 1995.

[5] M. Hafizi, C. Crowell, L. Pawlowicz, and M. Kim, "Improved current gain and f_τ through doping profile selection in linearly graded heterojunction bipolar transistors", *IEEE Transactions on Electron Devices*, vol. 43, No. 11, pp. 1826-1832, 1998.

[6] D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan, and M.J.W. Rodwell, "Baseband amplifiers in transferred-substrate HBT technology", *to be presented at GaAs IC Symp. 1998.*