Highly Integrated InP HBT Optical Receivers

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***Abstract*—This paper presents two highly integrated receiver circuits fabricated in InP heterojunction bipolar transistor (HBT) technology operating at up to 2.5 and 7.5 Gb/s, respectively. The first IC is a generic digital receiver circuit with CMOS-compatible outputs. It integrates monolithically an automatic-gain-control amplifier, a digital clock and data recovery circuit, and a 1 : 8 demultiplexer, and consumes an extremely low 340 mW of power at 3.3 V, including output buffers. It can realize a full optical receiver when connected to a photo detector/preamplifier front end. The second circuit is a complete multirate optical receiver application-specific integrated circuit (ASIC) that integrates a photo diode, a transimpedance amplifier, a limiting amplifier, a digital clock and data recovery circuit, a 1 : 10 demultiplexer, and the asynchronous-transfer-mode-compatible word synchronization logic. It is the most functionally complex InP HBT optoelectronic integrated circuit reported to date. A custom package has also been developed for this ASIC.**

***Index Terms*—Heterojunction bipolar transistor, indium phosphide, optical receiver, optoelectronic integrated circuit.**

I. Introduction

THERE is a growing need for high-performance and low-power optical receiver circuits in order to exploit the ever increasing bandwidth offered by fiber-optic communication in both terrestrial and spaceborne applications. InP-based IC technology is well suited to implement these circuits because of the inherent high device speed and the compatibility of the material system with the 1.3–1.55-μm wavelength fiber systems that exhibit low loss and low dispersion. InP heterojunction bipolar transistor (HBT) IC technology, for example, has achieved device f_T exceeding 150 GHz and divider circuit speed of 44 GHz [1]. InP pin-HBT optoelectronic integrated circuits (OEIC's) have demonstrated bandwidth of 23 GHz [2]. Fig. 1 shows the block diagram of a typical optical receiver. It consists of several functional blocks, each of which is commonly implemented in one or more IC's [3], [4]. The recognition that a higher level of integration of these functional blocks could lead to better performance, lower system cost, and better reliability was the driving force behind the whole arena of OEIC and integrated receiver development in recent years [5]–[7]. Many integration efforts, however, were directed toward multiple channels of the relatively simple front-end blocks (photo diode and amplifiers) [8], [9]. No InP-based IC result has been published on integrating the clock and data recovery (CDR) circuit and the demultiplexer to the front end.

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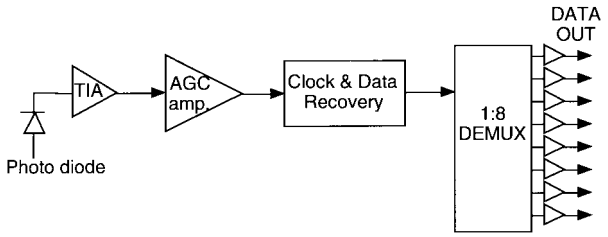

Fig. 1. Functional block diagram of a generic optical receiver.

Part of the reason was believed to be the relative immaturity of the fabrication technology, which limited circuit yield.

We developed two highly integrated receiver IC's in InP HBT technology that achieved a new level of functionality and performance. The first [10] was a 2.5-Gb/s generic receiver IC that consumed extremely low power with high functional integration. It monolithically integrated a wide-band automatic-gain-control (AGC) amplifier, a digital CDR circuit, and a 1 : 8 demultiplexer (DEMUX). It consumed only 340 mW power at 3.3 V, including nine CMOS-compatible output buffers. As a comparison, a somewhat similar circuit implemented in SiGe technology consumes more than 1 W of power [11]. Our receiver IC could realize a full optical receiver system when connected to a photo detector/preamplifier front-end OEIC. It is especially suitable for satellite-based communication applications where low power and high data rate are important.

The second IC [12] achieved an even higher level of performance and integration: a 7.5-Gb/s complete optical receiver consisting of a photo diode, a transimpedance amplifier (TIA), a limiting amplifier (LAMP), a digital CDR circuit, a 1 : 10 DEMUX, and the word synchronization logic. It consisted of 2100 transistors and was the most functionally complex InP HBT OEIC reported to date. This application-specific integrated circuit (ASIC) had multirate capability and was designed specifically for the current and next-generation spaceborne fiber-optic data bus (SFODB) environment [13], which required small size, low power, and radiation hardness. This data bus was encoded with the 8-B/10-B coding scheme and adopted the asynchronous transfer mode (ATM) data structure.

II. Design of the 2.5-Gb/s IC

The circuit was implemented with a very-high-speed InP-based HBT technology [14]. This technology allows us to implement both analog and digital circuits on the same substrate operating off a single 3.3-V supply. The AGC amplifier was designed for high sensitivity and high dynamic range requirements. Common-mode logic (CML) was used in all the digital circuit blocks. Differential signal lines were maintained

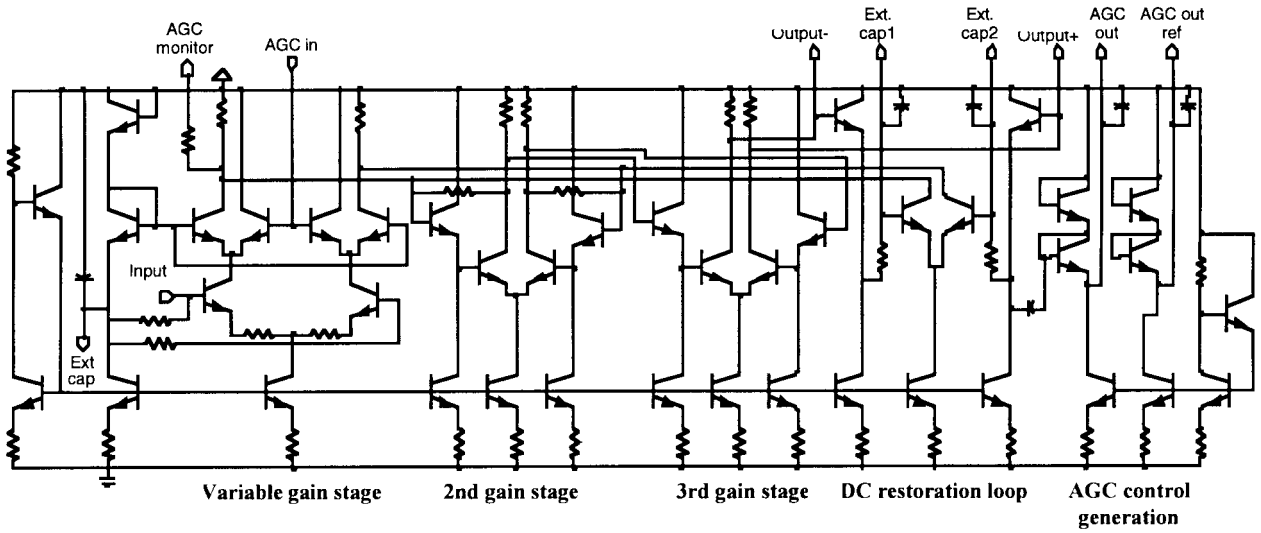

Fig. 2. Schematic of the AGC amplifier.

throughout the whole circuit except between the loop filter and the voltage-controlled oscillator (VCO) and at the CMOS-compatible outputs.

A. AGC Amplifier

The integrated receiver included a wide-band AGC amplifier. The first stage was a variable-gain stage in the Gilbert-cell configuration as shown in Fig. 2. The second and third gain stages were dc-coupled emitter-coupled pairs with emitter-follower buffers, with the second stage employing transimpedance loading to increase the stage bandwidth. A full differential signal path was used. DC balance in the circuit was maintained using a dc restoration loop between the output of the third stage and the input of the second stage. Control voltage for the variable-gain stage was provided by a differential full-wave rectifier implemented using four diode-connected transistors. The diodes were biased at 10 μA, reducing the AGC detector dead zone to $2kT/q$. Bypass capacitors required in the AGC detector, AGC loop, and dc restoration loop were implemented both on- and off-wafer to cover the wideband. To minimize power consumption, all gain transistors were operated at a low 5×10^3 A/cm^2 current density. This reduced transistor f_T to about 20 GHz from the peak value of 75 GHz (at 7×10^4 A/cm^2). The amplifier was designed for a target of 30-dB gain and 2.5-GHz bandwidth.

B. CDR

The CDR consisted of a digital phase-locked loop (PLL) and a decision circuit, as shown in Fig. 3. The PLL contained a phase detector, a loop amplifier/filter, and a VCO [15]. The phase detector was the "bang-bang" type that consisted of two flip-flops, one for sampling the clock at the rising edges of the data and the other at the falling edges. No frequency detector was included in this design. The VCO, as shown in Fig. 4, was the multivibrator design that required no external passive components. In addition to being controlled by the output of the loop filter, the VCO was designed to be externally tuned with a dc voltage over the frequency range from 2 to 3 GHz.

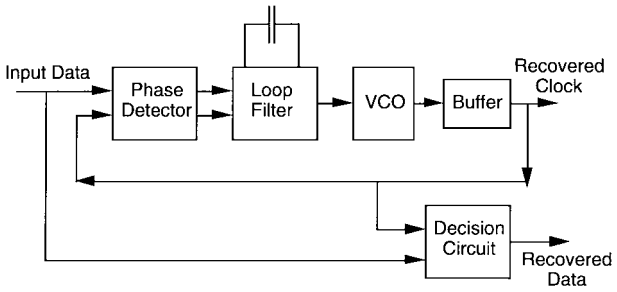

Fig. 3. Block diagram of CDR.

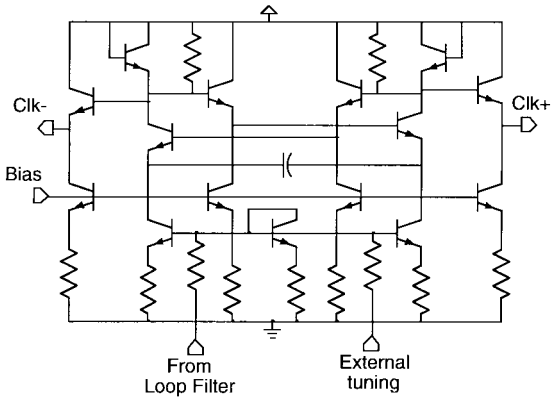

Fig. 4. Schematic of the multivibrator VCO.

This coarse tuning was designed to offset the effects of process and device variations. Fig. 5 shows the loop filter we used, which was slightly different than the one in [15].
It had an active stage where the gain could be optimized for the best loop performance. Only one off-chip filter capacitor was needed to set the loop bandwidth. The targeted pole and zero frequencies of the loop filter were 0.5 and 15 MHz, respectively. Extensive SPICE simulation of the loop was performed to verify the locking characteristics of the PLL. The decision circuit was made up of a single flip-flop. This CDR design used devices very efficiently, containing fewer than 90 transistors total.

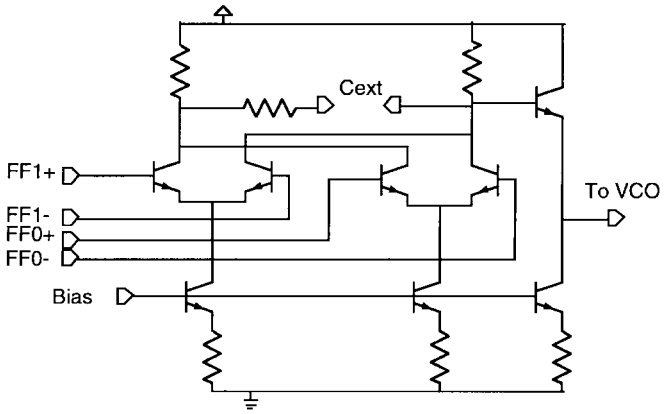

Fig. 5. Schematic of the loop filter.

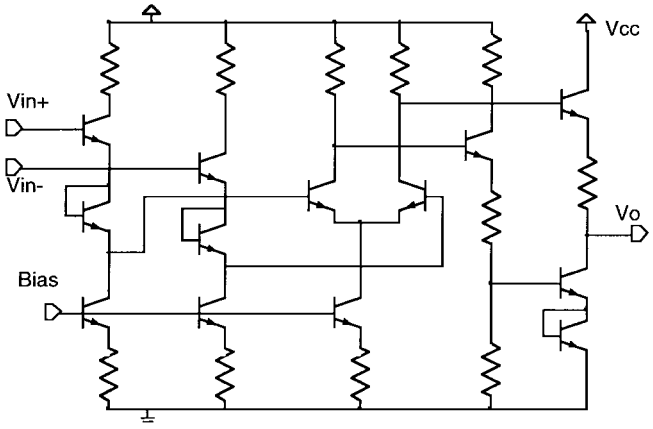

Fig. 6. Schematic of the CMOS-compatible output buffer of the 2.5-Gb/s receiver IC.

C. DEMUX and Output Buffers

The DEMUX employed the tree-type architecture for low power consumption. Power was saved when the clock rate was halved for every stage through which the data moved. The output buffers were designed for CMOS levels using a totem-pole configuration, as shown in Fig. 6. The output stage had its own power-supply pad to isolate any switching noise from coupling back to the rest of the circuit. There were nine such output buffers, eight for the data and one for the clock.

III. Design of the 7.5-Gb/s ASIC

The functional block diagram of the 7.5-Gb/s optical receiver ASIC is shown in Fig. 7. This circuit shared many basic building blocks with the 2.5-Gb/s circuit, with appropriate size modifications for higher speed operation. Only design considerations with topological differences with the 2.5-Gb/s design are discussed below.

A. Application-Specific Architecture

The current SFODB operates at the SONET OC-48 rate of 2.48 Gb/s. It is expected that the data rate of future SFODB's will continue to increase. The next rate up will be the OC-96 environment of 4.96 Gb/s. Accounting for the coding scheme and other communication overheads associated with the ATM protocol, an overhead factor of 1.458 is needed,

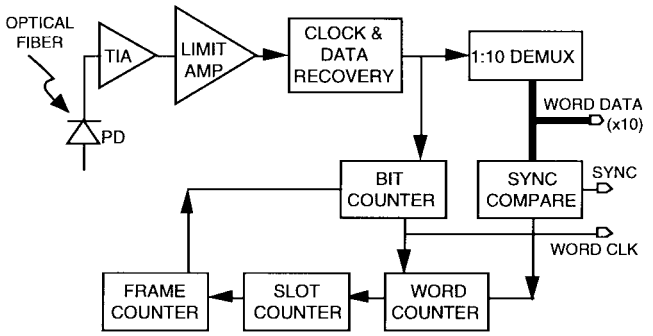

Fig. 7. Functional block diagram of the 7.5-Gb/s integrated optical receiver ASIC.

bringing the physical bit-rate requirement of the receiver to 7.23 Gb/s. Our receiver was designed to operate at multiple rates, from a maximum of 7.5 Gb/s down through 3.6, 1.8, and 0.9 Gb/s (divided by two, four, and eight, respectively). The data format was in 8-B/10-B code, in which two extra bits were incorporated to each 8-bit byte to make up a 10-bit word. This code provided better dc-balance by limiting the maximum run length to five. Another important benefit of coding the data was to support nondata sync word for word synchronization.

The SFODB [13] has a simple time division multiple access frame structure. The basic "payload" data cell has been chosen to be the ATM cell with 48 bytes of data and five bytes of header, for a total cell length of 53 bytes. Three bytes of frame overhead are attached before each ATM cell to form a slot. Thirty-two slots constitute an SFODB master frame. The very first three frame overhead bytes include the frame sync word (K28.5 or K28.7 in 8-B/10-B code). This is summarized in Fig. 8. Our receiver design would be able to detect these two word patterns (and their complements) for word-synchronization purpose.

B. Photo Diode, Transimpedance, and Limiting Amplifiers

A PIN photo diode was integrated on-chip using the base-collector junction of the HBT structure. The diode area was 15 μm in diameter, optimized for bandwidth and alignment requirements. Since the photo diode shared the same base-collector layers as the HBT structure, a tradeoff had to be made for the collector thickness. A thicker collector would improve the responsivity of the photo diode but degrade the frequency response of the HBT device. As the SFODB was a short-haul fiber communication environment, the sensitivity requirement of the receiver was on the order of 0 dBm. This allowed us to use our baseline HBT process with a 0.7-μm-thick collector.

Signal amplification was provided by a TIA and a LAMP to reduce the dynamic range seen by the CDR circuit. The TIA, as shown in Fig. 9, was a single-ended common emitter gain stage with collector-to-base feedback. Its output fed both the differential inputs of the LAMP with a low-pass filter inserted along one but not the other input. This connection scheme provided a single-to-differential signal conversion for signal frequency above the cutoff frequency of the low-pass filter. The LAMP input with the low-pass filter was effectively grounded above the cutoff frequency. Signals along the other input path therefore got amplified. Below the cutoff frequency,

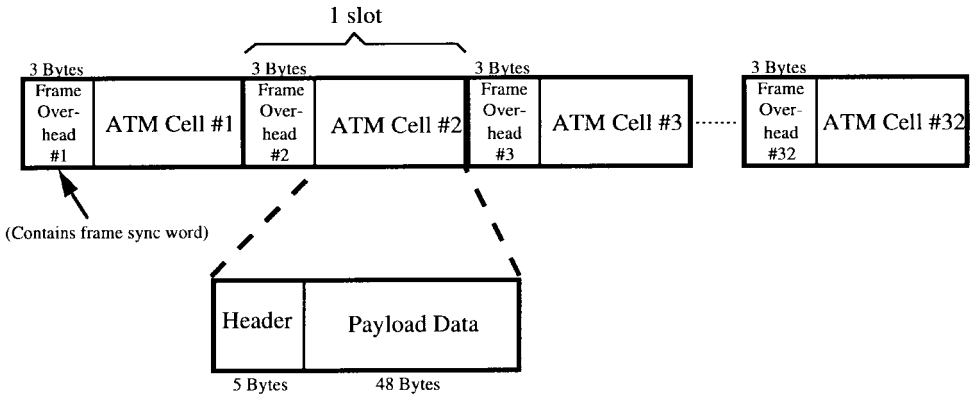

Fig. 8. SFODB frame structure showing one frame of data.

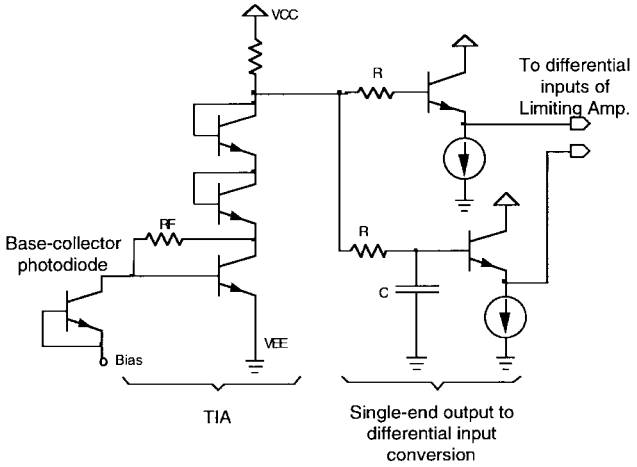

Fig. 9. Schematic of the transimpedance amplifier and its interface to the limiting amplifier.

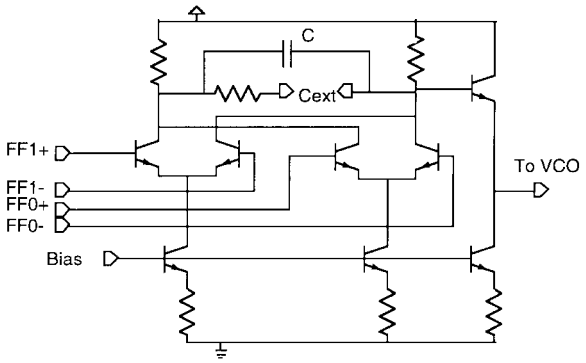

Fig. 10. Schematic of the loop filter for the 7.5-Gb/s circuit with the extra on-chip capacitor C.

the low-pass filter had little effect on the signal passing through it. As a result, the differential input paths of the LAMP saw the same signal, which canceled each other. This coupling scheme required only one blocking capacitor instead of two. The short run length in the data stream called for a cutoff frequency that could be as high as 10 MHz, which allowed the capacitor to be implemented on-chip. The result was the saving of two bonding pads (and the external passive elements associated with them) and of significant chip area.

The LAMP incorporated only the first and last gain stages and the dc restoration loop of the AGC amplifier of the 2.5-Gb/s design, with modification to the bias current to reflect a higher bandwidth but lower gain requirements. The AGC circuit portions were not needed in this amplifier because the data stream had a relatively small dynamic range of 10 dB.

C. CDR

The block diagram of the CDR circuit was similar to that of the 2.5-Gb/s design except a digital prescalar was inserted after the buffer in the PLL to enable multirate operation. Two CMOS-compatible inputs selected one of four possible prescalar ratio—divided by one, two, four, and eight—allowing the PLL to operate at the corresponding four data rates. Learning from test data collected from the 2.5-Gb/s design, we added an on-chip capacitor in parallel with the serial $R \cdot C_{\text{ext}}$ branch in the loop filter, as shown in Fig. 10. It in effect added a pole to the loop filter response, compensating for the zero generated by the parasitic inductance on the leads of the external capacitor.

D. DEMUX and Bit Counter

The recovered bit data were converted into word data by a 1:10 (due to the 8-B/10-B data coding) DEMUX. Fig. 11 shows the schematic of the DEMUX, which had a serial-in, parallel-out and a parallel-in, parallel-out shift registers instead of the tree structure of flip-flops because the word length was not an integral power of two. It required two clocks: the recovered bit clock and a "narrow" word clock with the same pulse width as the bit clock but with only 5% duty cycle. The narrow word clock was converted from the recovered clock by the bit counter, which also generated the output word clock of 50% duty cycle. The schematic of the bit counter is shown in Fig. 12. It had a bit-slip mode that counted up to 11 bit clock pulses before the two word clocks were generated. This mode was used to shift the boundary of the word until a sync word was detected.

E. Sync Logic

The digital sync logic consisted of the sync compare and three resettable counters (word, slot, and frame counters), which counted according to the ATM cell protocol, as described above. The word counter could count up to 53 or 56, the slot counter to 32, and the frame counter to a programmable

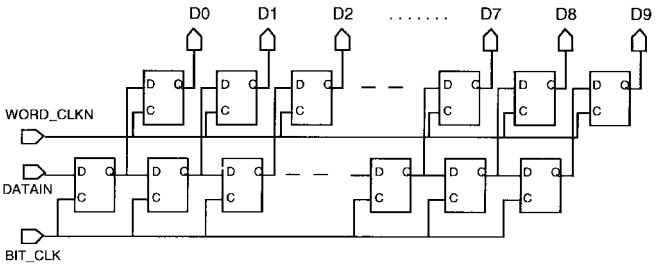

Fig. 11. Schematic of the demultiplexer for 8-B/10-B coded data.

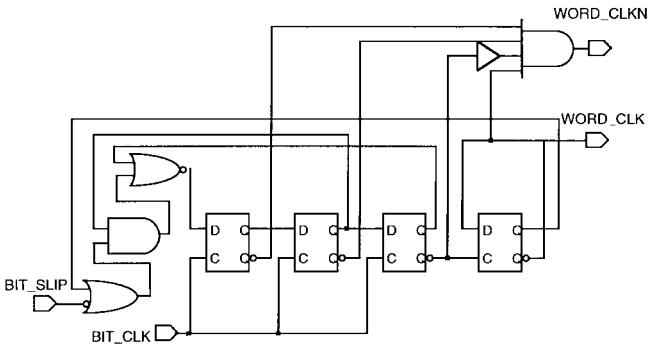

Fig. 12. Schematic of the bit counter.

number between one and 16, all of which used the same toggle flip-flop as the basic building block. The schematic of the frame counter is shown in Fig. 13. The other two counters had similar schematics with minor modifications reflecting the difference in the number of stages (five for the slot and six for the word counters), the decoding logic, and the programmable feature (one select control for the word counter and none for the slot counter). The output of the frame counter was the bit-slip signal, which caused the bit counter to slip a bit when no sync word was detected in the sync compare circuit within the specified frames of data. Upon detection of a sync word, the sync compare circuit would send out a sync signal to reset the three counters. To take advantage of the slower operating speed of these counters, part of their logic was implemented with single-ended NOR gate for saving chip area.

F. Interconnects and I/O

To maintain signal integrity over on-chip long interconnects, differential signal lines were routed adjacent to each other. Source and load termination that matched the metal line impedance (about 90 Ω) were also incorporated at selected long, high-speed signal paths, such as those between the CDR and the DEMUX, which ran for about 4 mm. All control inputs were CMOS compatible except that the polarity of the power supply had to be reversed, i.e., a logic "1" is near 0 V while a logic "0" is near −3.3 V. All outputs had differential CML drivers capable of delivering 400-mV_{pp} signals to a 50-Ω load.

IV. Fabrication

Both receiver IC's were successfully fabricated in our in-house 3-in IC line utilizing the baseline InP HBT technology [14], which employed a 2×2 μm^2 emitter size transistor with a peak f_T of 75 GHz. Two layers of metal were used for interconnect. For the 7.5-Gb/s IC, the integrated photo diode was implemented with the same base-collector junction as the HBT structure. Two additional masking steps were needed to define and coat the photo diode.

The photomicrograph of the 2.5-Gb/s receiver IC is shown in Fig. 14. It measured 2.8×2.35 mm^2 and consisted of approximately 550 transistors. Two-thirds of the area was occupied by the DEMUX and the output buffers.

The photomicrograph of the 7.5-Gb/s optical receiver ASIC is shown in Fig. 15. It consisted of about 2100 transistors and was pad-limited to an area of 4.15×3.1 mm^2. Defect control was a critical requirement for yielding this relatively large circuit. We have grown epi wafers that have random defect density of less than 100 per cm^2. In our first fabrication lot, a best wafer yield of 10% was achieved. This yield level represented a progressively maturing InP HBT fabrication process that allowed us to continue to develop IC's of increasing complexity.

V. Experimental Results and Discussion

A. 2.5-Gb/s IC

We have performed on-wafer tests of the receiver IC. Test results of individual functional blocks were obtained from drop-in test cells. The frequency response of the AGC amplifier is shown in Fig. 16. Maximum gain of about 28 dB with 2-GHz bandwidth was observed. These results were within about 20% from simulation. Resonance between the external capacitors and probe inductance resulted in in-band resonance. This was subsequently eliminated by damping resistors in the 7.5-Gb/s design. The power consumption of the AGC amplifier was about 20 mW.

The CDR exhibited satisfactory locking behavior. It had a lock-in range of about 30 MHz when locked at a 2.1-Gb/s data stream. Moreover, the locking frequency could be externally tuned over more than a 1-GHz span. When tested with a $2^7 - 1$ pseudorandom bit stream (PRBS), the recovered data achieved a bit error rate (BER) of less than 10^{-12} with 9.6-ps rms jitters. The eye diagram of the recovered data is shown in Fig. 17. The CDR portion of the chip consumed about 90 mW of power.

The rest of the IC also performed properly as measured from the integrated receiver chip. The data output voltage swing, when measured with a high-impedance scope with 20-pF capacitive loading, was 900 mV_{pp} at 310 Mb/s and 1.5 V_{pp} at 60 Mb/s. In the realistic multichip-module environment where a CMOS load was about 5 pF, a factor of four speedup was expected for the same voltage swing. So the IC was expected to provide a 1.5-V_{pp} output swing at 240 Mb/s, or 1.92-Gb/s input bit rate. The nine output buffers consumed only 80 mW of power.

The power consumption of the whole chip was only 340 mW. This extremely low power level reflected the intrinsic high bandwidth of the InP HBT technology as well as its capability to trade speed for power. In fact, all transistors in the receiver were operating at current densities significantly below their maximum f_T point. Efficient implementation of the CDR such as using a multivibrator instead of a ring oscillator VCO also contributed to the low power. The CMOS-compatible output buffers employed the push–pull-style circuits to further conserve power.

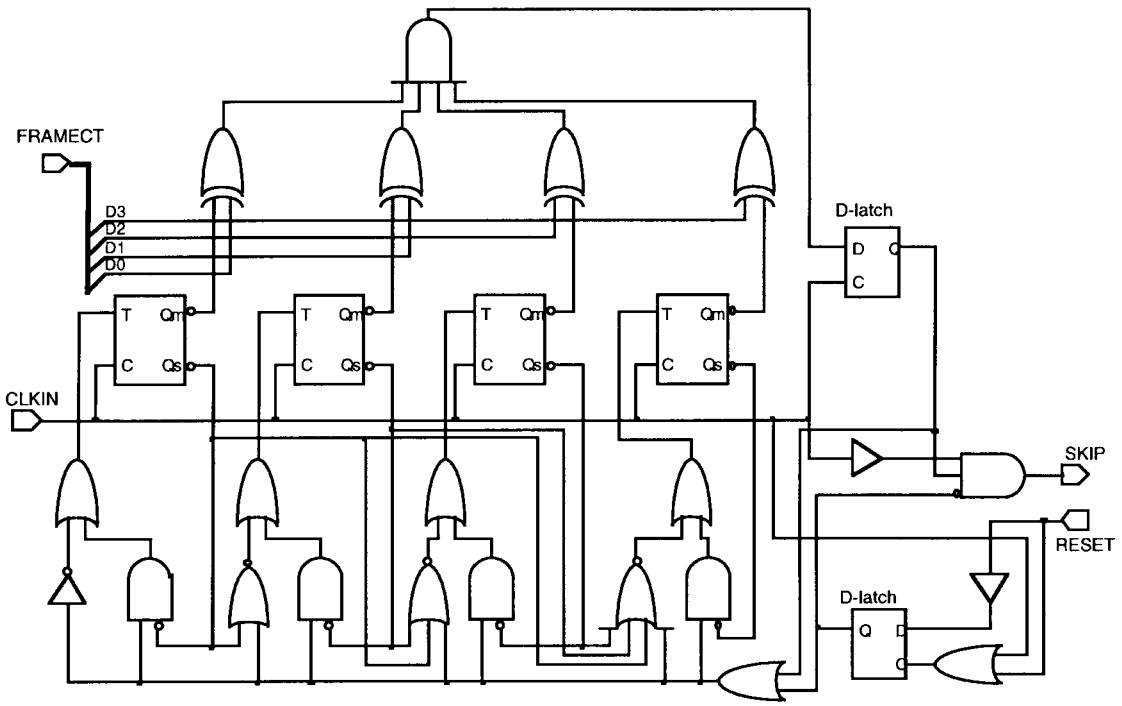

Fig. 13. Schematic of the frame counter.

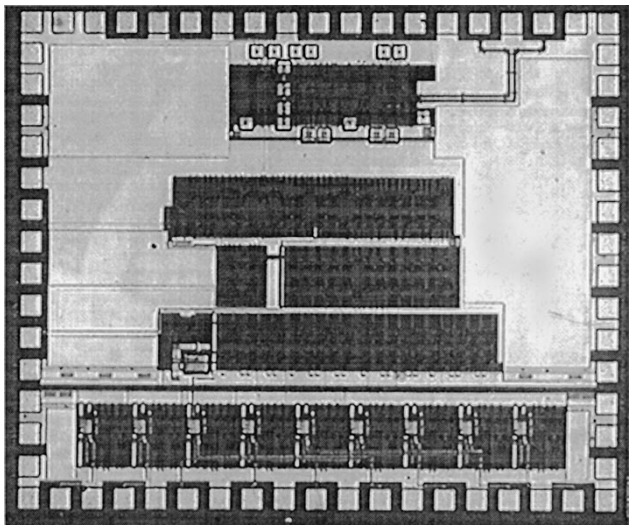

Fig. 14. Photomicrograph of the 2.5-Gb/s integrated receiver IC.

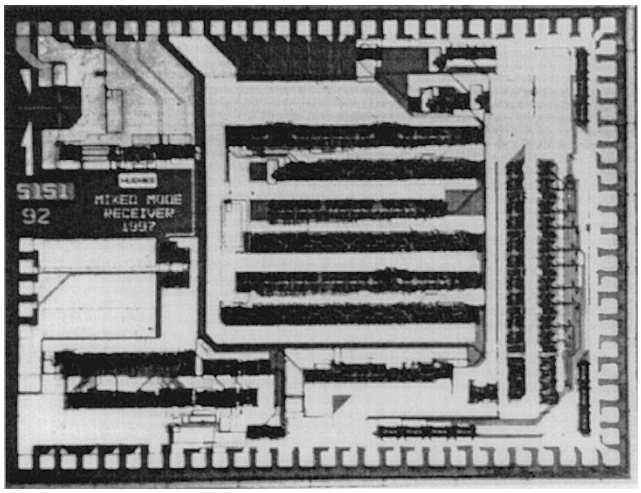

Fig. 15. Photomicrograph of the 7.5-Gb/s integrated optical receiver ASIC.

B. 7.5-Gb/s IC

We have performed extensive on-wafer tests on the 7.5-Gb/s receiver ASIC. By segmenting the power-supply nets to the various functional blocks and providing intermediate I/O points to the full ASIC, we eliminated the need to include drop-in test cells on the wafer. The performance of each functional block could be measured directly from the full ASIC itself. An optical signal of 1550 nm was fed through a single-mode fiber, which was mounted slightly tilted from the vertical on a micromanipulator and was aligned over the photo diode by monitoring the photo diode bias current. The frequency response of the front-end circuits, which included the photo diode, the TIA, and the LAMP, was measured using an HP 8703A lightwave component analyzer. Measured responsivity, transimpedance gain, and bandwidth were 0.51 A/W, 650 Ω, and 4.4 GHz, respectively, as shown in Fig. 18. The measured gain and bandwidth were within 20% from simulation, the discrepancy being primarily attributable to the circuit parasitics. For testing the rest of the circuit, a laser diode modulated by a BER test set was used as the input signal source. The VCO of the CDR could be externally tuned with a dc voltage over more than 15% frequency span. The BER of the recovered data at 7.6 Gb/s was measured to be less than 10^{-11}, with a 2^7- 1 PRBS input of 0-dBm power. The eye diagrams of the LAMP output and the recovered data are shown in Fig. 19. Very open eye is observed for the recovered data. Optical sensitivity of the CDR recovered data (not just at the output of the LAMP) was -4.2 dBm at a BER of 10^{-9}. We expected the sensitivity at the 1300-nm wavelength to be

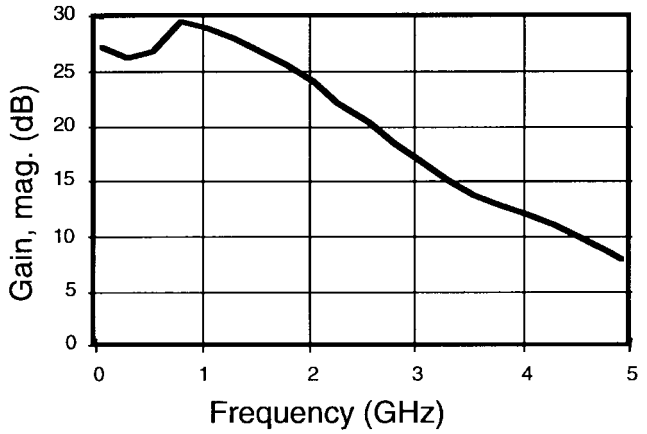

Fig. 16. Frequency response of the AGC amplifier.

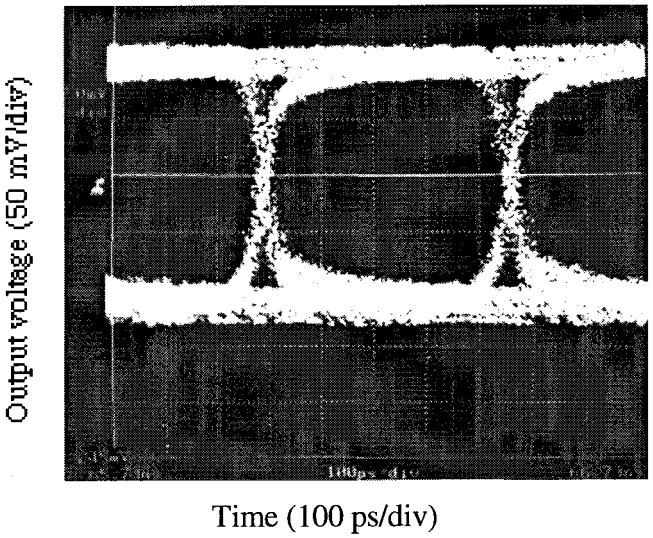

Fig. 17. Eye diagram of recovered data of CDR with 2.1 Gb/s, $2^7 - 1$ PRBS input; waveform had 9.6-ps rms jitters.

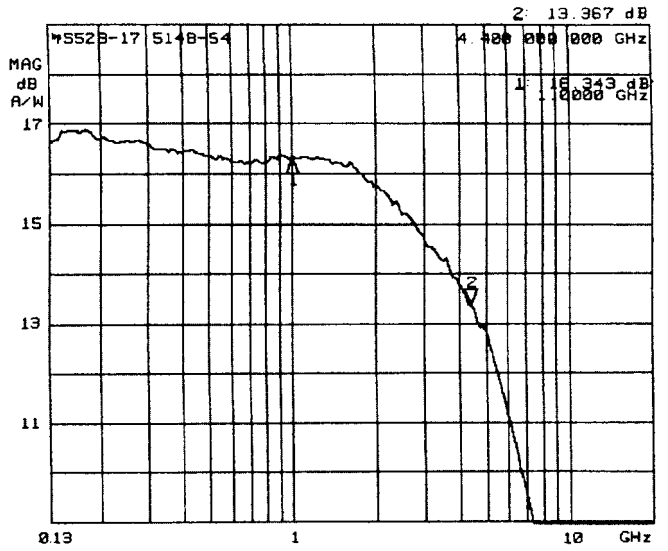

Fig. 18. Frequency response curve (measured current at output of LAMP normalized to input optical power) of front-end circuits of the 7.5-Gb/s optical receiver ASIC.

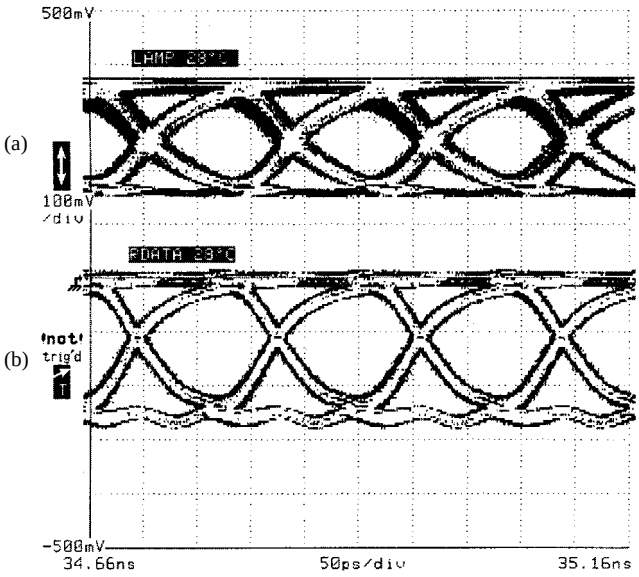

Fig. 19. Eye diagram of the (a) output of LAMP and (b) CDR recovered data with a $2^7 - 1$ PRBS input at 7.61 Gb/s.

better because of the higher responsivity of the photo diode. The relatively low sensitivity of this receiver did not reflect the inherent capability of the technology [6] but rather the input specifications of the ASIC, which did not require amplifiers with high gain. In other words, the sensitivity was not noise limited but rather gain limited. The demultiplexed data and word clock output waveforms are shown in Fig. 20, with about 400-mV_{pp} swing. The chip consumed about 3 W of power, a relatively low budget considering the high functionality and performance of the circuit.

A custom package has been developed for the optical receiver ASIC, as shown in Fig. 21. The optical fiber was horizontally mounted with optical signal reflected at an angle cut over the photo diode. A 2.7-dB fiber link loss was measured. No other significant performance loss due to the packaging was measured. Further environmental tests will be performed on the packaged units.

VI. Conclusion

We have successfully designed, fabricated, and tested two highly integrated receiver IC's in InP HBT technology for 2.5- and 7.5-Gb/s optical communication applications. The first IC consisted of an AGC amplifier, a clock and data recovery circuit, and a demultiplexer, and consumed only 340 mW of power. The measured data have validated our design approach and have demonstrated the potential of the InP HBT technology to integrate analog and digital functions for low-power and high-speed applications. The second IC was a fully integrated optical receiver ASIC that monolithically integrated all the critical components, including the photo diode, the amplifier stage, the clock and data recovery circuit, the demultiplexer, and the word-synchronization logic. It consumed 3 W of power and consisted of 2100 transistors. The capability and level of maturity of the InP HBT technology in implementing mixed-mode, high-speed, and complex optoelectronic circuits has been demonstrated. Achieving even lower power is feasible

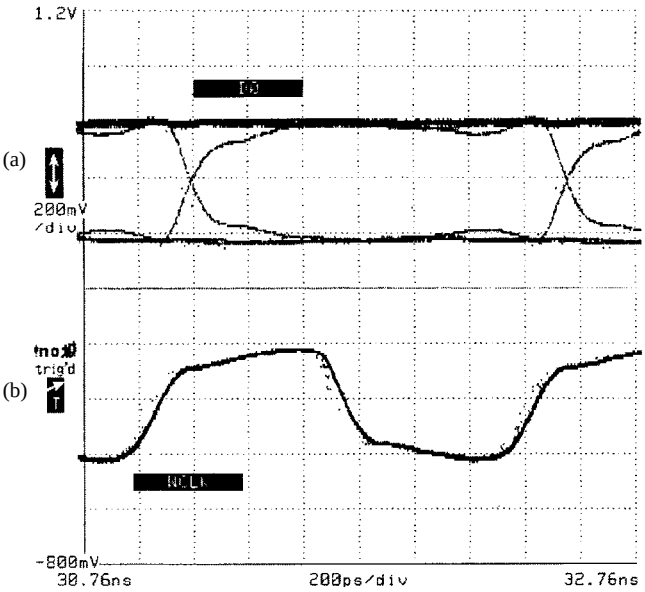

Fig. 20. Demultiplexed (a) data and (b) word clock output waveforms at 731 MHz.

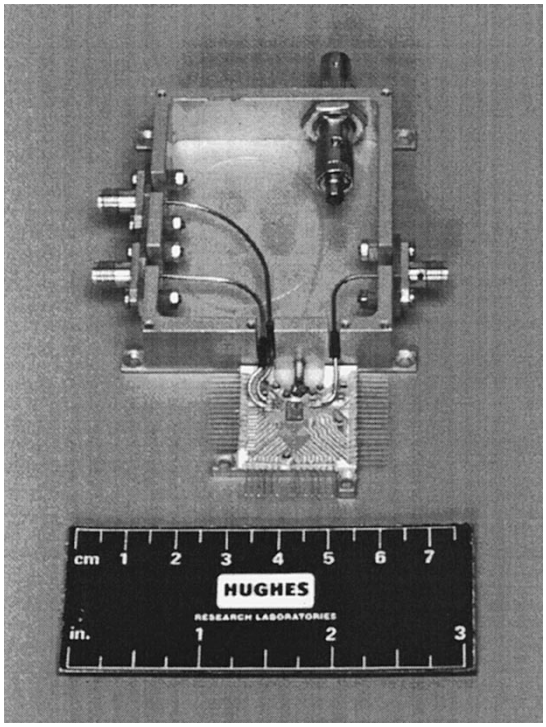

Fig. 21. Packaged optical receiver ASIC with lid removed.

through device scaling. Additional functionality such as frequency detection, lock indication, and data decoding can be included in future integration.

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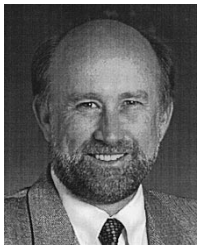

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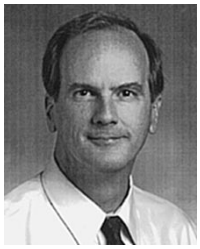

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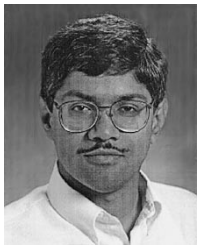
Dr. Rodwell received a 1989 National Science Foundation Presidential Young Investigator award. He received the 1997 IEEE Microwave Prize for his work on submillimeter-wave diode IC's.



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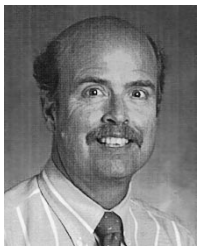

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