CASCODE-DELAY-MATCHED DISTRIBUTED AMPLIFIERS FOR EFFICIENT BROADBAND MICROWAVE POWER AMPLIFICATION

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Abstract — We present a broadband distributed power amplifier topology capable of providing efficiencies approaching 50%. Unlike tapered-drain-line power TWAs, high- Z_o lines are not required, greatly improving realizability in MMIC implementation. An experimental hybrid achieved bandwidth 25% of f_{τ} with ~15 dB gain and 30 ± 5 % power-added-efficiency.

I. INTRODUCTION

2-20 GHz phased-array-radars, now in development under ONR support, will require power amplifiers having high output power and high power-added efficiency (PAE) over a 10:1 bandwidth. AlGaN / GaN HEMTs have high $f_{\tau}V_{br}$ products [1], and can provide high output power within this bandwidth. Efficient broadband circuits are also required.

Distributed or traveling-wave amplifiers (TWAs) are broadband circuits whose gain-bandwidth product substantially exceeds the device current-gain cutoff frequency f_{τ} [2-5]. High bandwidth is obtained by

absorbing the transistor input capacitances (C_{gs}) into a synthetic input (gate) transmission line. This input synthetic line introduces relative delays between the drive voltages of the various transistors within the TWA. A similar synthetic output (drain) transmission line provides compensating delays in the output circuit, so that AC drain currents of the individual transistors add in-phase at the load. While the transistor output capacitance (C_{ds}) is also absorbed into the output synthetic line, HEMTs typically have $C_{ds} \ll C_{gs}$, and the high bandwidths observed with TWAs results from incorporation of C_{es} into the input synthetic line. The output synthetic line is present primarily for delay equalization.

In TWAs with synthetic output transmission lines, the AC drain current of each transistor contributes equally to forward and reverse waves on the output line. Half the AC output current of each transistor is wasted, and efficiency is below 25%. Reported monolithic power TWAs typically have 10-15% PAE.

The tapered-drain-line *TWA* [4] eliminates the drain-line reverse wave, and has theoretical class-A efficiency

approaching 50%. The Ginzton / Hewlett tapered-drain-line TWA is difficult to realize in monolithic form. A TWA with N cells and load Z_a requires output line sections of impedance NZ_a. A 4-cell TWA with 50Ω loading requires 200 Ω microstrip lines. On III-V substrates, such transmission-lines have only a few μ m width, resulting in high skin-effect losses and (with ~ 5 mA/ μ m electromigration limit), very low current-carrying capability. TWAs using GaN HEMTs must produce RF output currents approaching 1 A. Partially tapering of the drain-line impedance [6,7] reduces the required line impedances below NZ_0 at the expense of lower efficiency. PAE is usually below 20%.

We demonstrate a distributed amplifier having no output synthetic transmission line. The drain-line reverse wave is eliminated, and class-A efficiencies can approach 50%. Delay equalization is instead provided by impedance-matched line sections between common-source (CS) and common-gate (CG) devices within the TWA. High-impedance line sections are not required. An experimental hybrid

achieved bandwidth 25% of f_{τ} with ~15 dB gain and 30 ± 5 % power-added-efficiency.

II. CIRCUIT DESIGN

In the cascode-delay-matched TWA (fig. 1) delay matching is provided by transmission-line sections between CS and CG transistors within a cascode cell. The equalizing line sections have delay increments of τ , the loaded per-section delay on the gate line. To avoid resonances, the equalizing delay lines must be terminated in their characteristic impedance $Z_{o,dl}$. As the large-signal input impedance of a CG HEMT is V_P/I_{dys} , the delay-equalizing line impedances must be $Z_{o.dl} = V_P / I_{dss}$. For a TWA with N HEMTs of breakdown V_{br} driving load Z_a , output loadline matching requires $I_{dss} = V_{br} / NZ_o$, and hence an equalizing impedance line $Z_{o,dl} = V_p / I_{dss} = N Z_o V_p / V_{br}$.

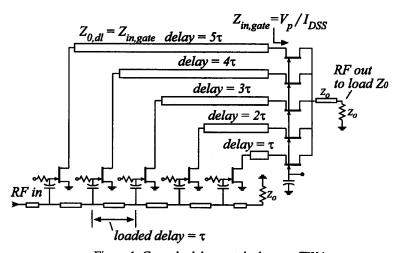


Figure 1: Cascode-delay-matched power TWA

For both GaAs and GaN HEMTs, $V_{br}/V_p \approx 10$, hence in a 4-cell TWA driving a 50 Ω load the equalizing lines must have 20 Ω characteristic impedance. 20 Ω -impedance lines are readily realized on MIMICs. Other circuit design details are similar to previously reported TWAs [2,3].

III. EXPERIMENTAL RESULTS

As a first demonstration, a 3-cell hybrid amplifier was constructed using discrete L-band packaged GaAs FETs (Fujitsu FSU01LG) mounted on a 20-mil Duroid microstrip substrate. Smallsignal gain is 10 dB and bandwidth is 3.5 GHz (fig. 2). Fig. 3 shows output power and PAE for 10-dBm input. The output power is > 23 dBm and the PAE is 30 ± 5 % between 0.2 - 2.5 GHz. Fig. 4 shows PAE at frequencies of 0.5, 1.5 and 2.5 GHz. The peak PAE at these frequencies are 44%, 36% and 28% respectively. The roll-off in the output power and PAE is attributed to the FET output capacitance C_{ds} . Circuits with improved output broad-band matching should provide improved PAE at the upper band-edge.

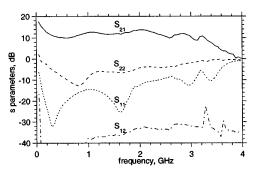


Figure 2: Small-signal S-parameters

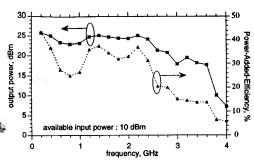


Figure 3: PAE and gain vs. frequency at 10 dBm available input power

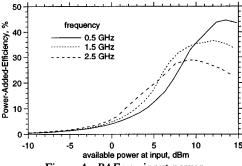


Figure 4: PAE vs. input power

Performance is also limited by parasitics arising from hand assembly.

IV. CONCLUSION

The cascodedelay -matched distributed amplifier topology is a realizable distributed physically amplifier capable of providing class-A limited efficiency. This topology is suitable for efficient high power broadband MMIC amplifiers. An experimental hybrid achieved gain-bandwidth product of $1.4 \cdot f_{\tau}$, with $30 \pm 5 \%$ power-addedefficiency. The efficiency at higher frequencies can be improved further by using improved broad-band output matching networks. Monolithic amplifiers using GaN HEMTs are now in design.

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V. REFERENCES

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