A 50mm Copper/Polymer Substrate HBT IC Technology for >100GHz MMICs

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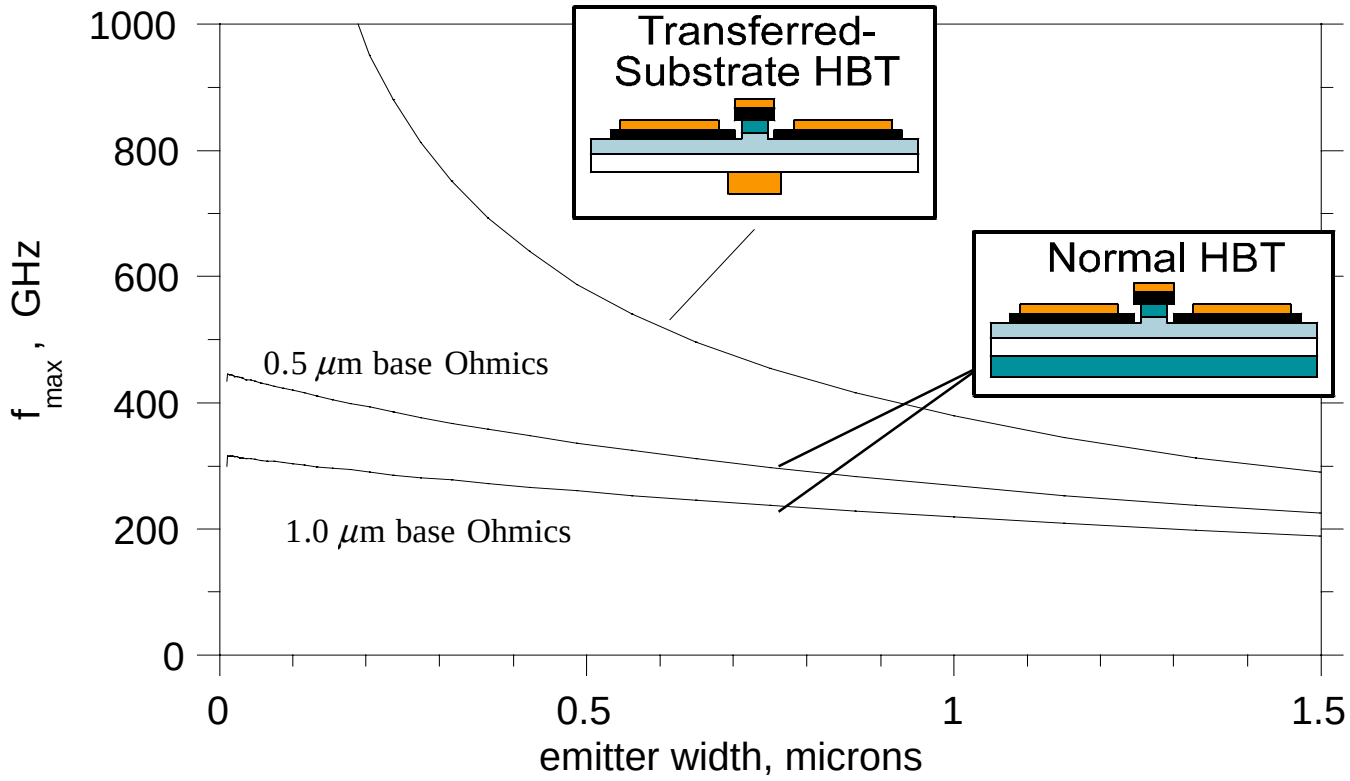
Introduction

100+GHz integrated circuits require:

- Better active devices
- Appropriate, controlled impedance wiring environment
- Packageability
- Complex, delay sensitive circuits will require dense integration

Faster Transistors



- UCSB “transferred substrate” process allows lateral scaling of HBT. Record f_{max} more than doubled.
- Most circuits demand high f_t. Laterally scalable device allows f_{max} to be retained when f_t is improved by vertical scaling.

Substrate Engineering

For Packaging

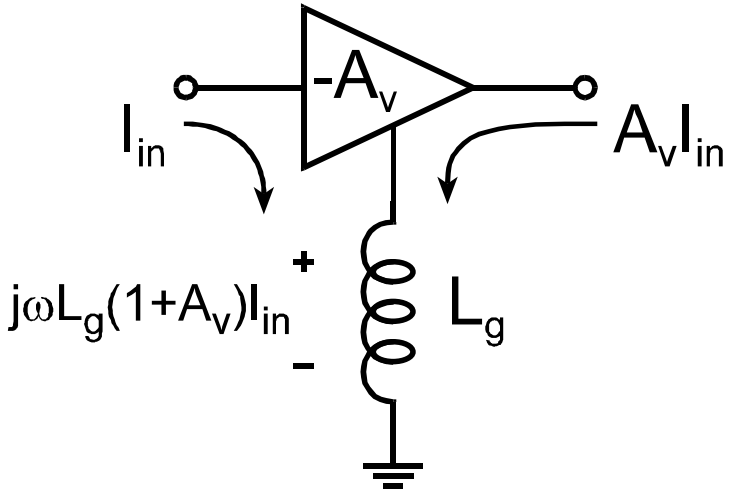
- parasitic ground lead inductance
- heatsinking of densely integrated active devices

For Wiring

- minimize shared parasitic inductance to ground
- suppress coupling between lines
- high group velocities benefit delay sensitive circuits

Package Grounding Parasitics

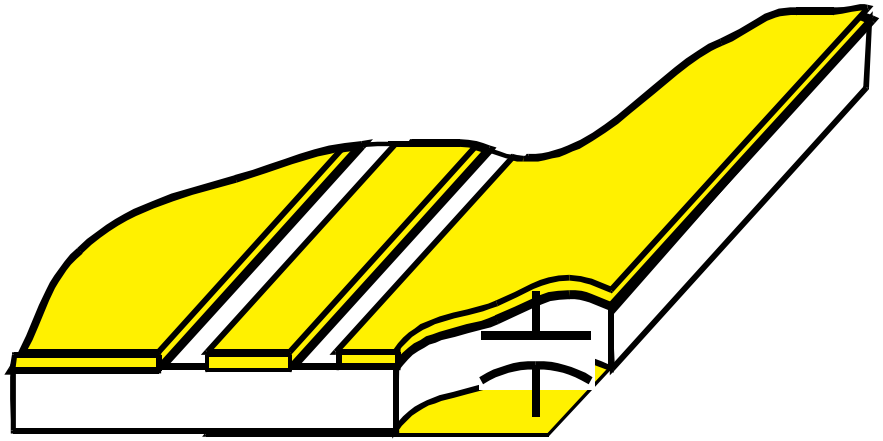
- Shared ground return inductance couples sub-circuits
- peripheral wire/ribbon bond grounding introduces substantial inductance

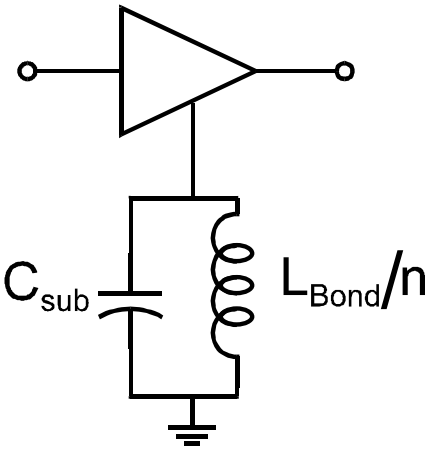


Miller Multiplication

100GHz ICs demand low ground return inductance

CPW Ground Planes Form Capacitor to Package



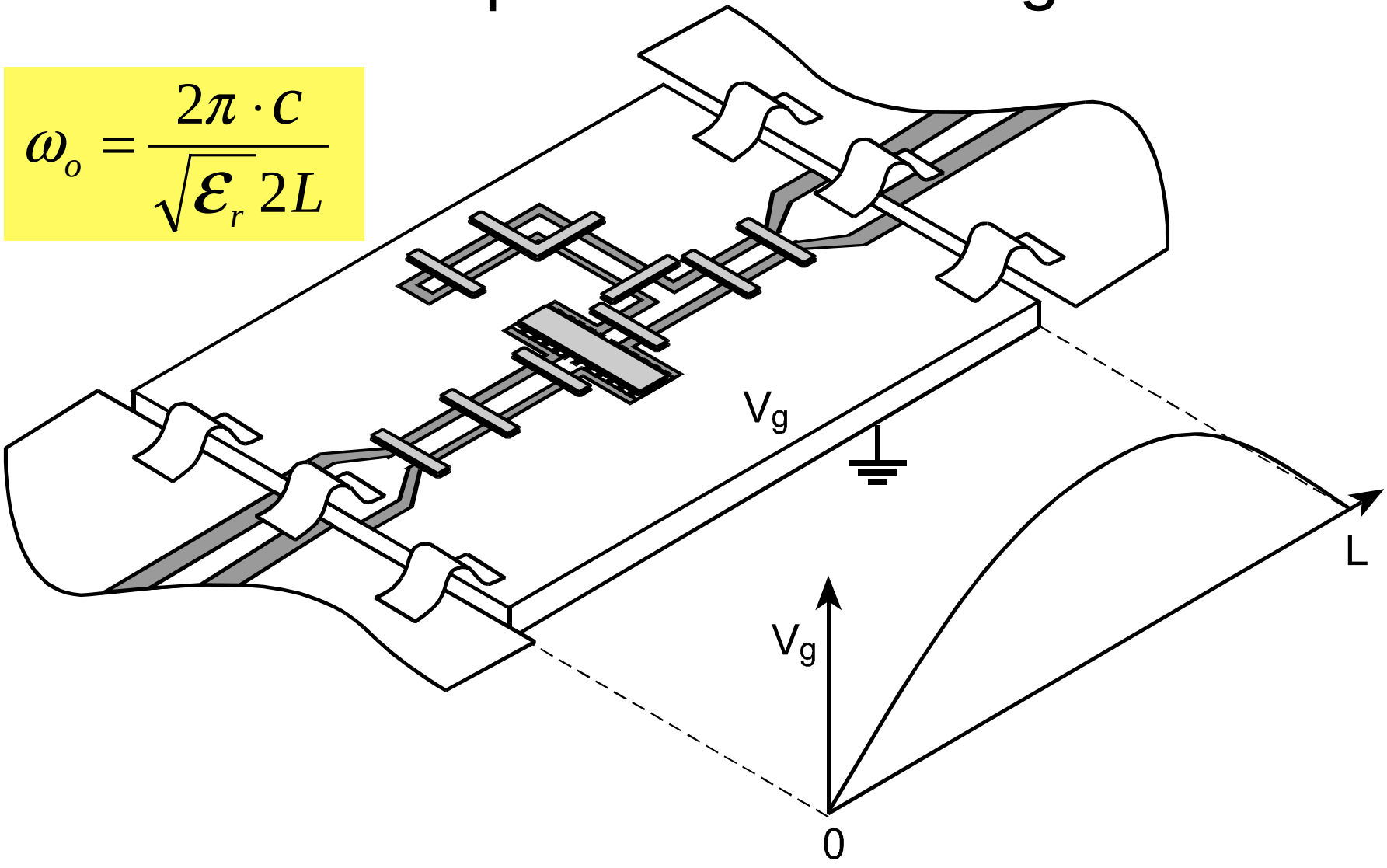


$$\omega_o = \frac{1}{\sqrt{C_{sub} L_b / n}}$$

Bond wire inductance resonates with parallel plate capacitance

Peripheral Grounding

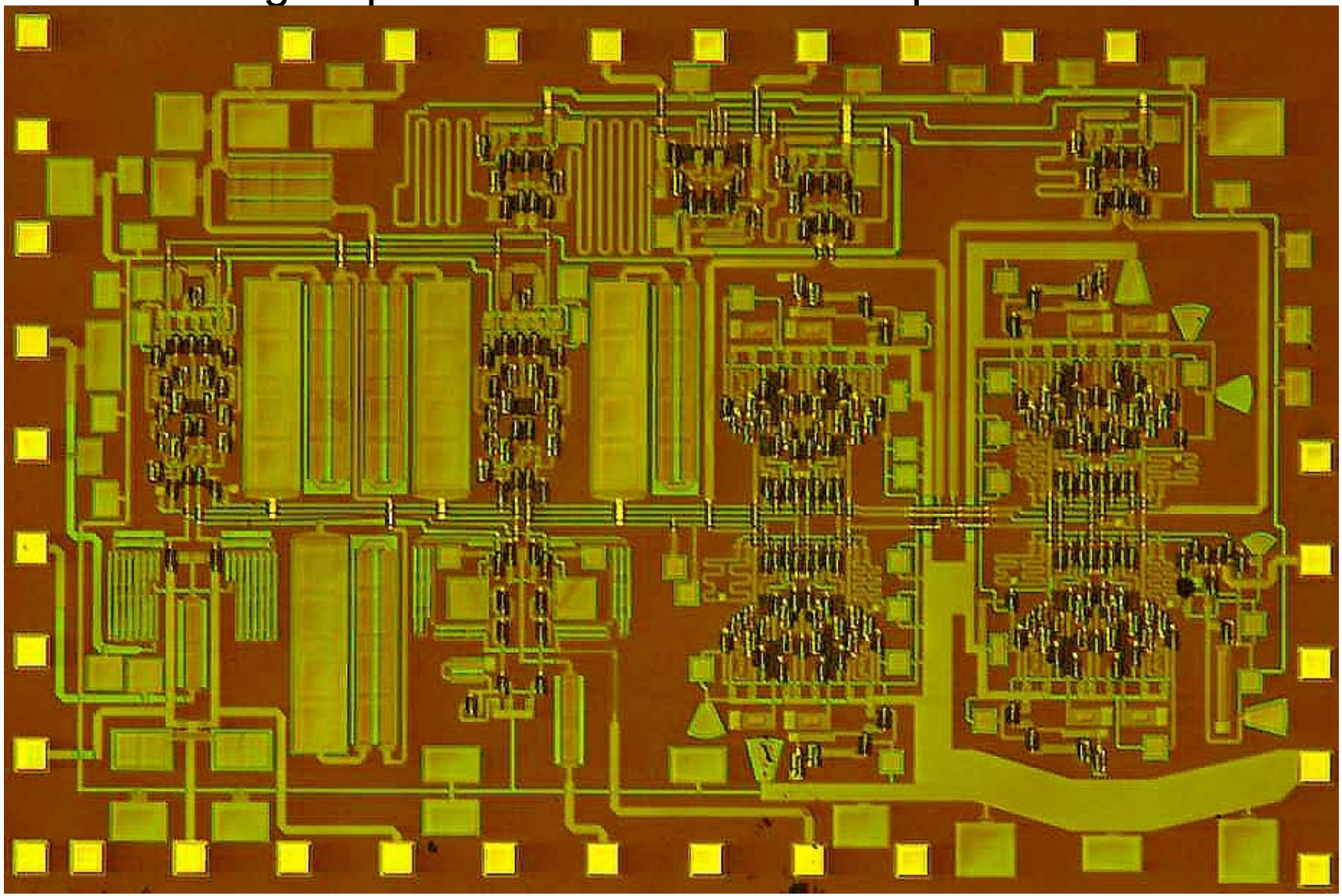
$$\omega_o = \frac{2\pi \cdot c}{\sqrt{\varepsilon_r}\, 2L}$$



Peripheral grounding allows parallel plate mode resonance
InP die dimensions must be <0.4mm at 100GHz

Problem:Fast ICs will be bigger than c/2nL

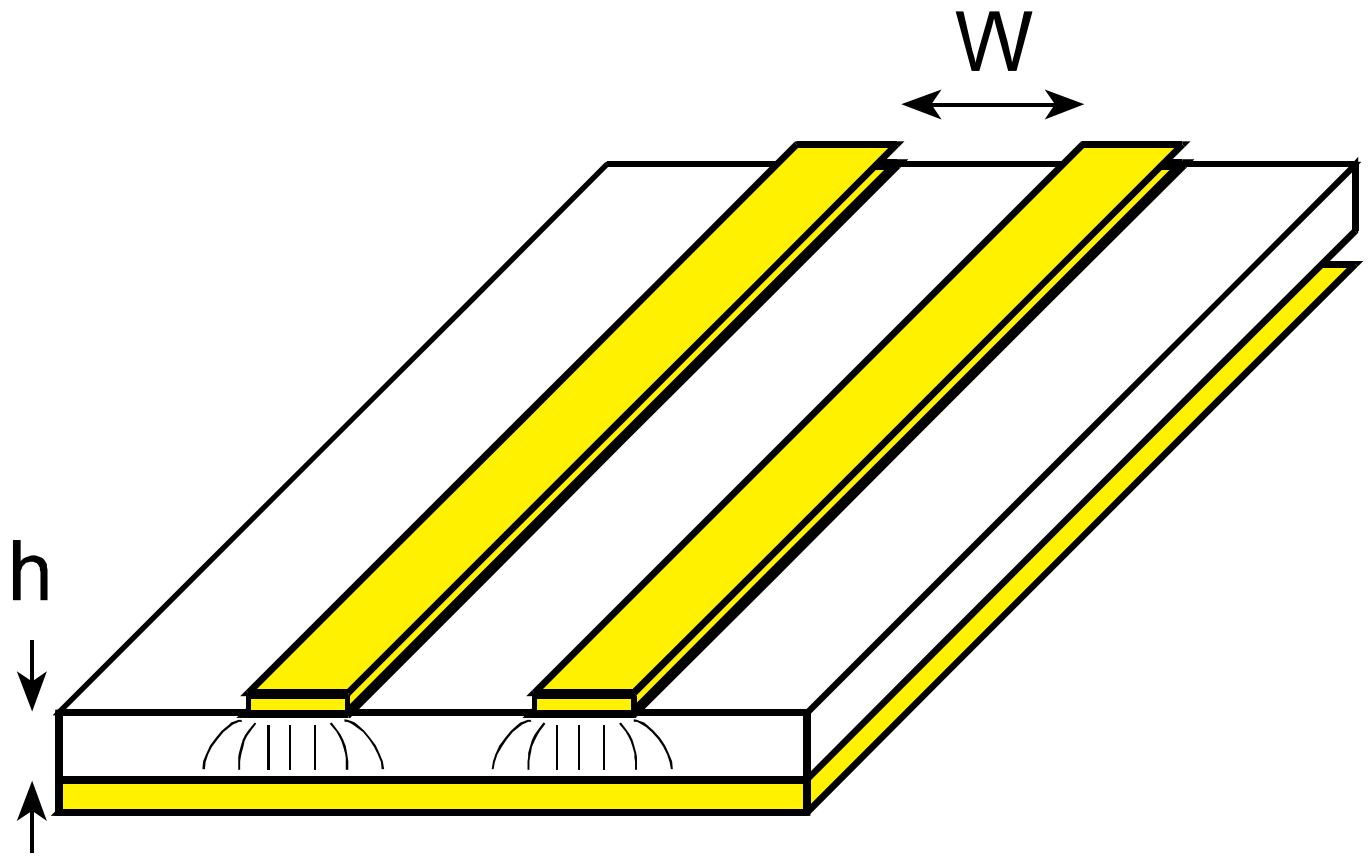
High Speed Σ–Δ ADC in development



Wiring Environment for 100+GHz

- complex ICs require densely packed transmission lines, controlled Z_o
- Must suppress: line-line coupling
  substrate modes
  radiation
  crosstalk via shared L_{ground}
- Low ε_r transmission line dielectric for short delays

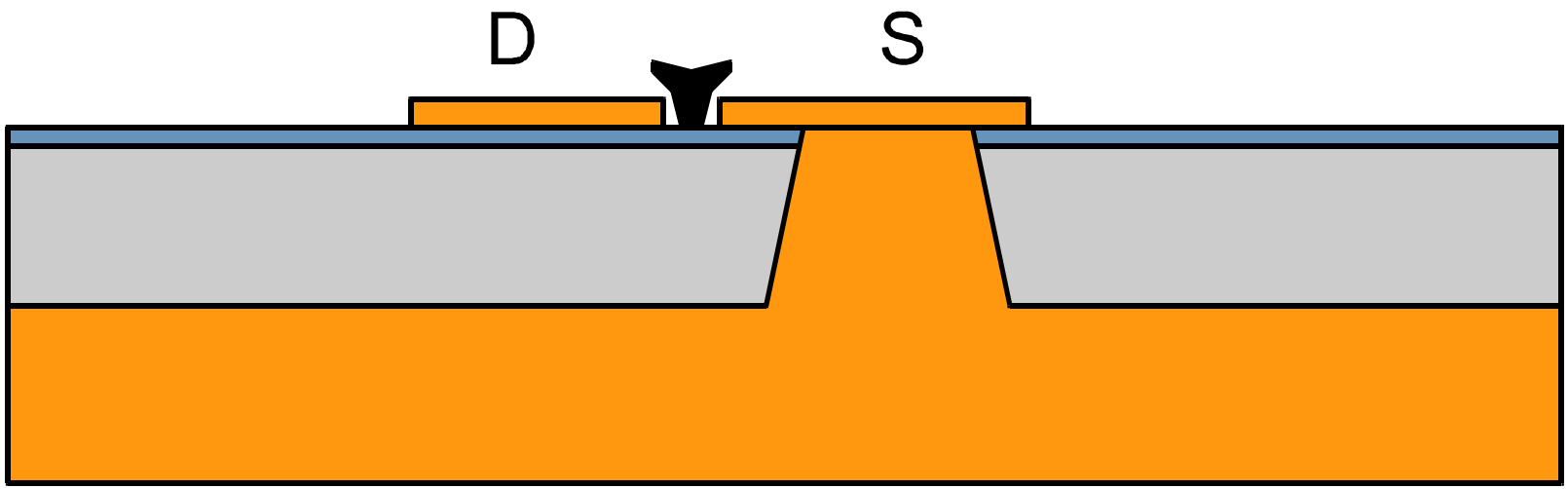
Dense wiring demands thin microstrip



Fringing fields couple adjacent lines.

Line separation, $W \geq 3h$ typically required.

The microstrip via inductance problem



12 pH via inductance for 100 micron MIMIC substrate

j7.5 Ohms at 100 GHz, j15 Ohms at 200 GHz

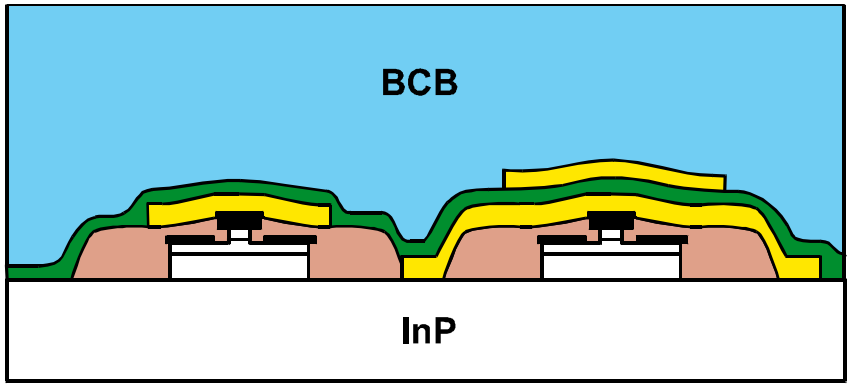
A formidable difficulty for > 100 GHz IC design

At 100 um substrate thickness, via spacing must be > 100 um

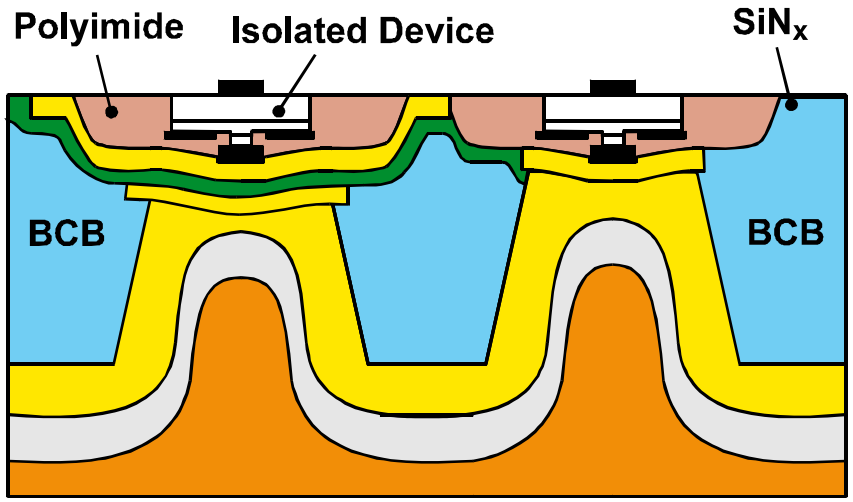
Solutions include “masterslice”, flip-chip, substrate transfer

Cu/Polymer Substrate Process

- InAlAs/InGaAs HBT
- HBTs, passive elements, interconnects fabricated on InP
- Microstrip substrate deposited
- InP removed
- Collectors formed

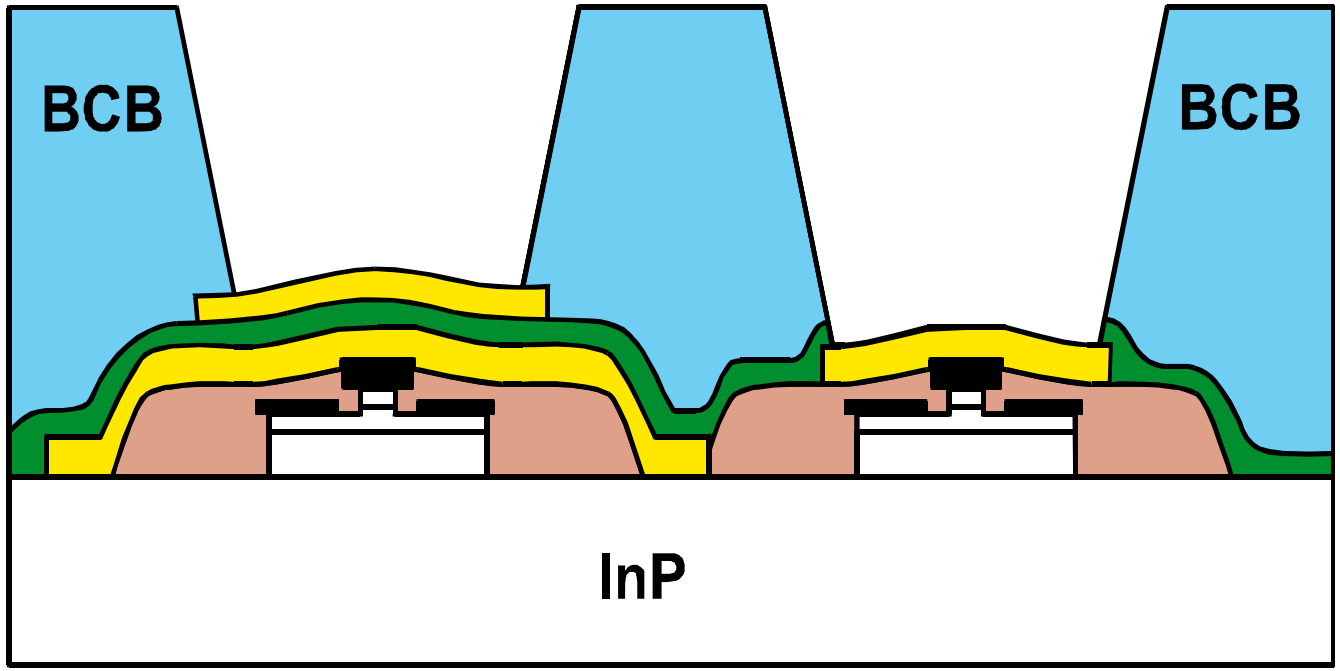


HBT's, passives, interconnect on InP



Electroplated Cu surrogate substrate formed, InP removed

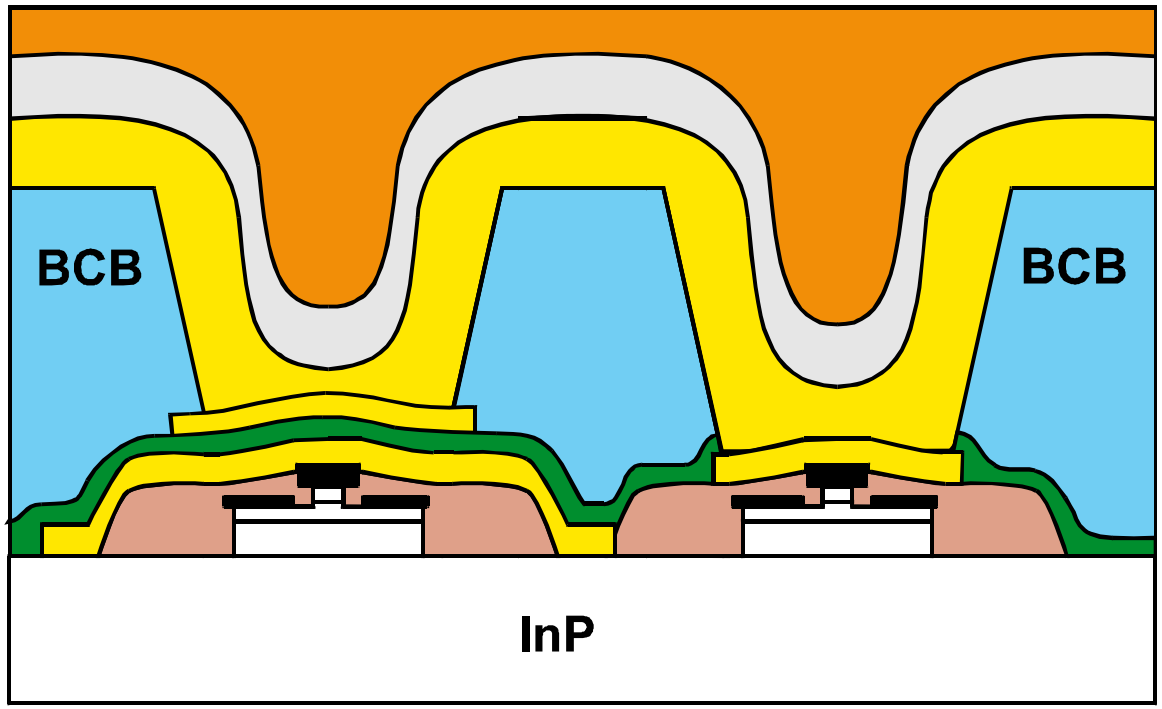
Deposit Microstrip Dielectric



Deposit BCB polymer dielectric
microstrip can be made arbitrarily thin

Dry etch ground vias
vias are short, small, aligned to active areas

Electroplate the Surrogate Substrate

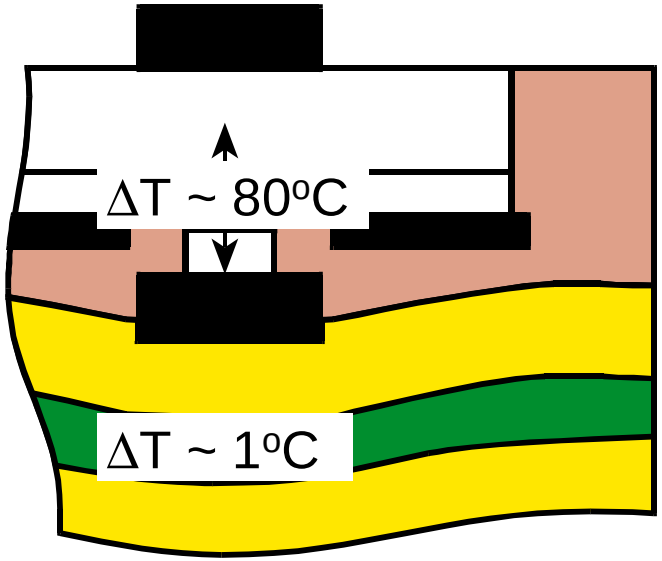


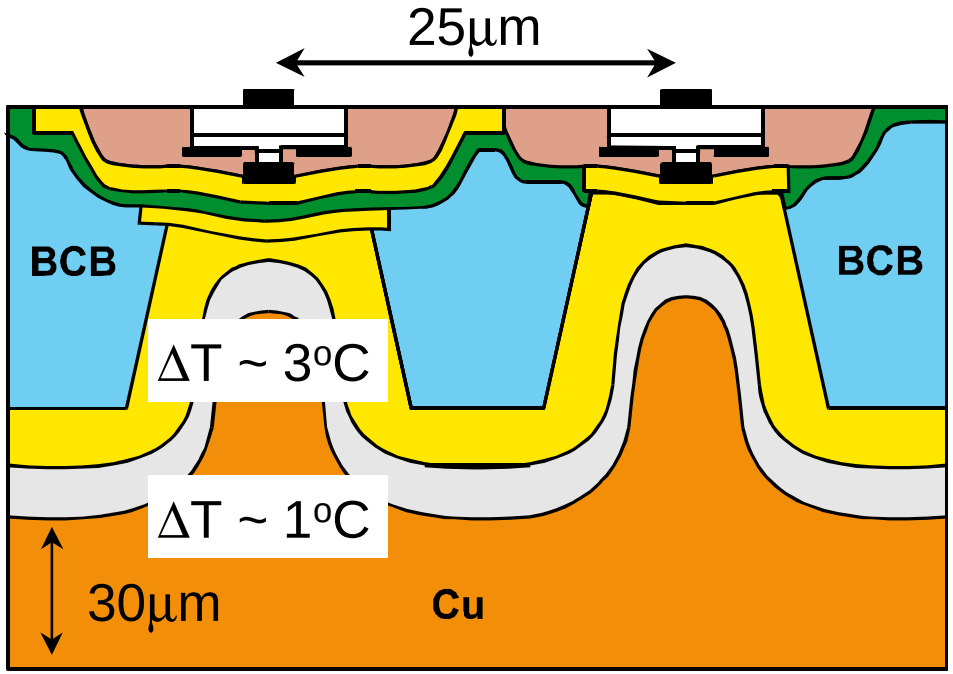
Electroplate thick ground plane to serve as surrogate substrate

Au, Ni plated from commercial chemistry

~30μm of Cu from simple $CuSO_4$, H_2SO_4 solution

Thermal Resistance of Cu MMIC Technology

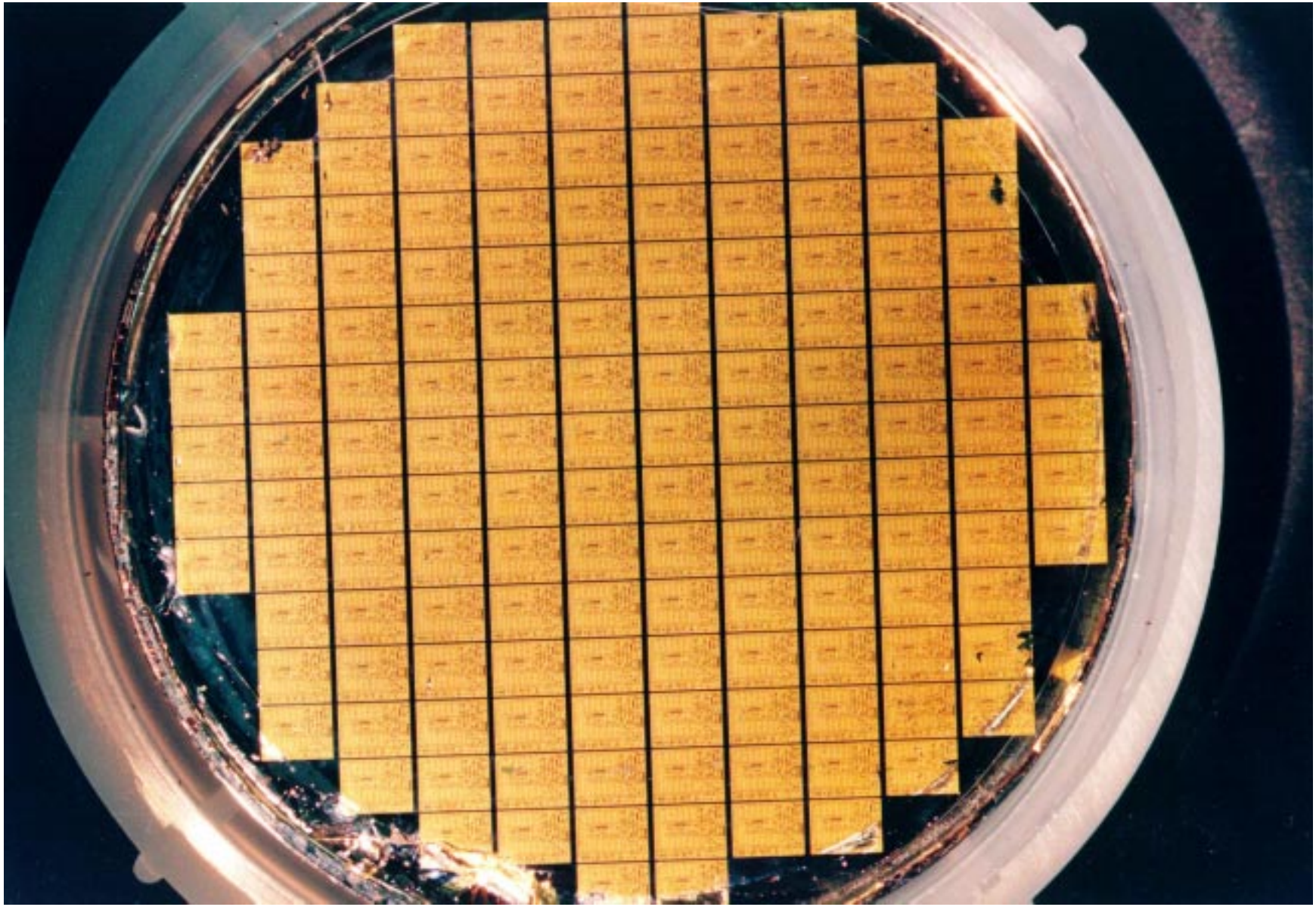




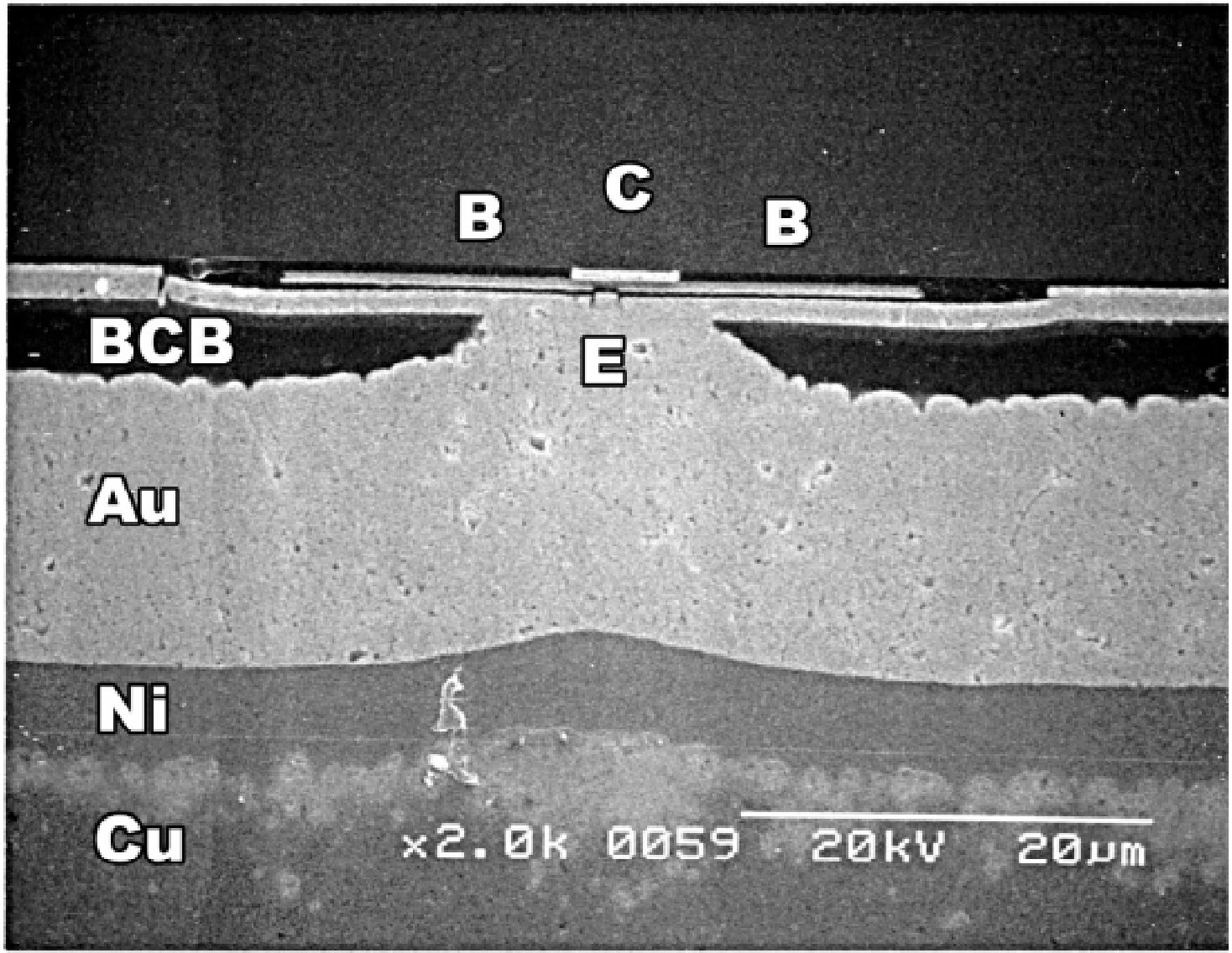
J_E ~10^5 Acm^{-2}, V_{CE} ~ 1V

- InAlAs/InGaAs emitter: large thermal resistance
- Need InP emitter with its 15:1 better κ_{th}
- Cu substrate affords κ_{th} 5:1 better than InP

Transfer of Entire 2” HBT MMIC Wafer

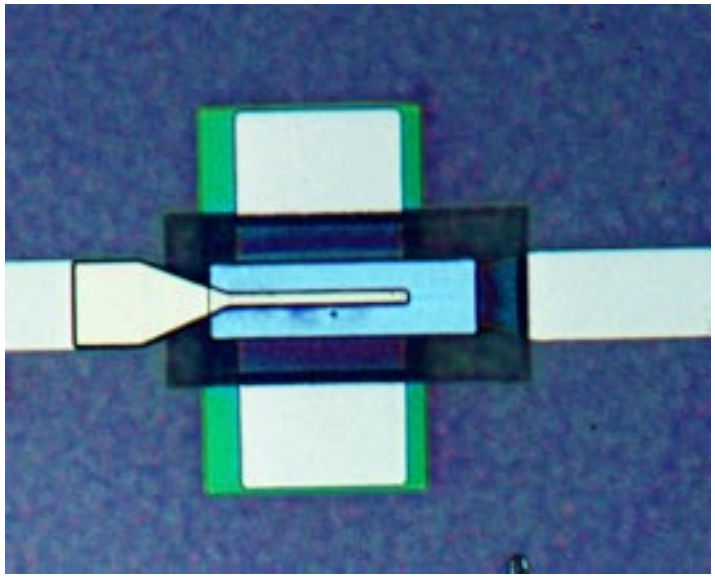


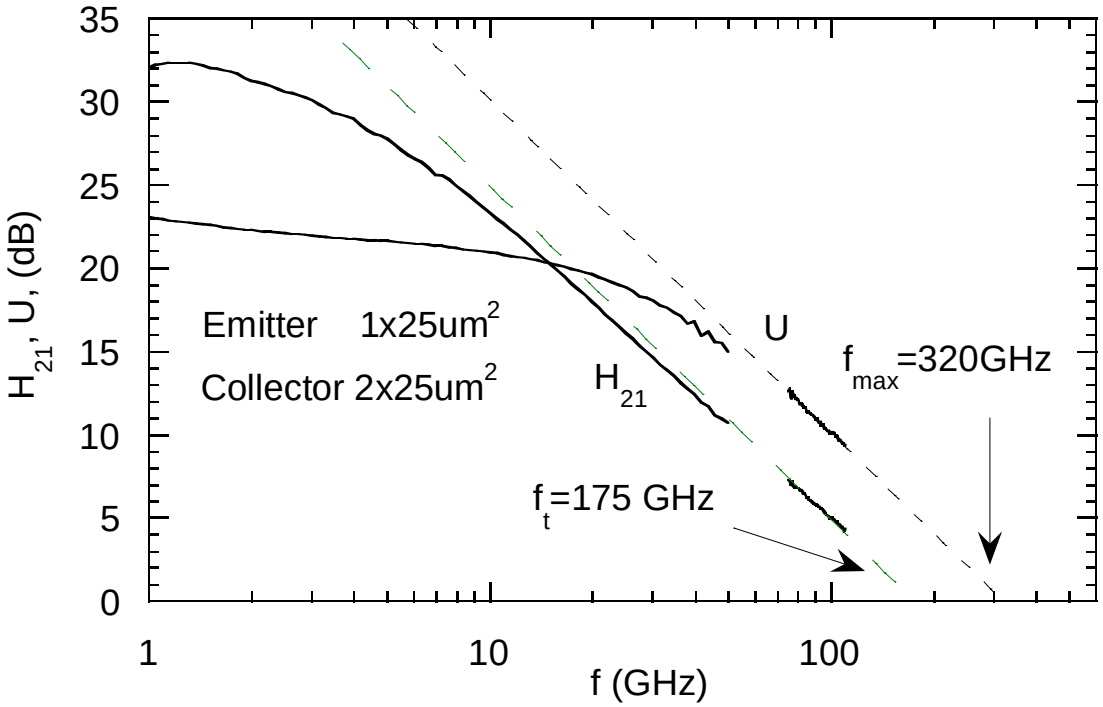
Cu Surrogate Substrate



Cross sectional SEM of test wafer

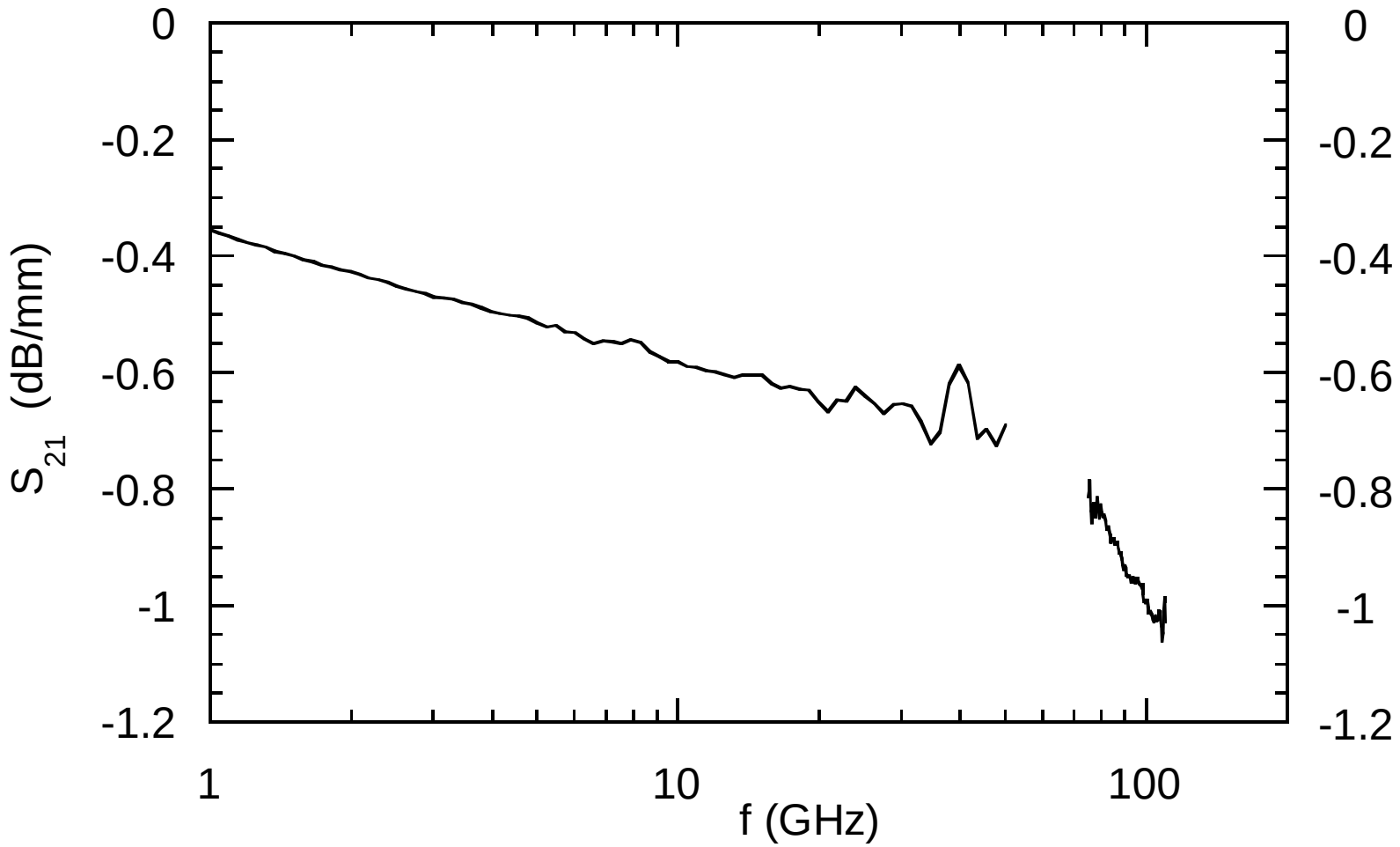
Discrete HBT from 50mm Wafer



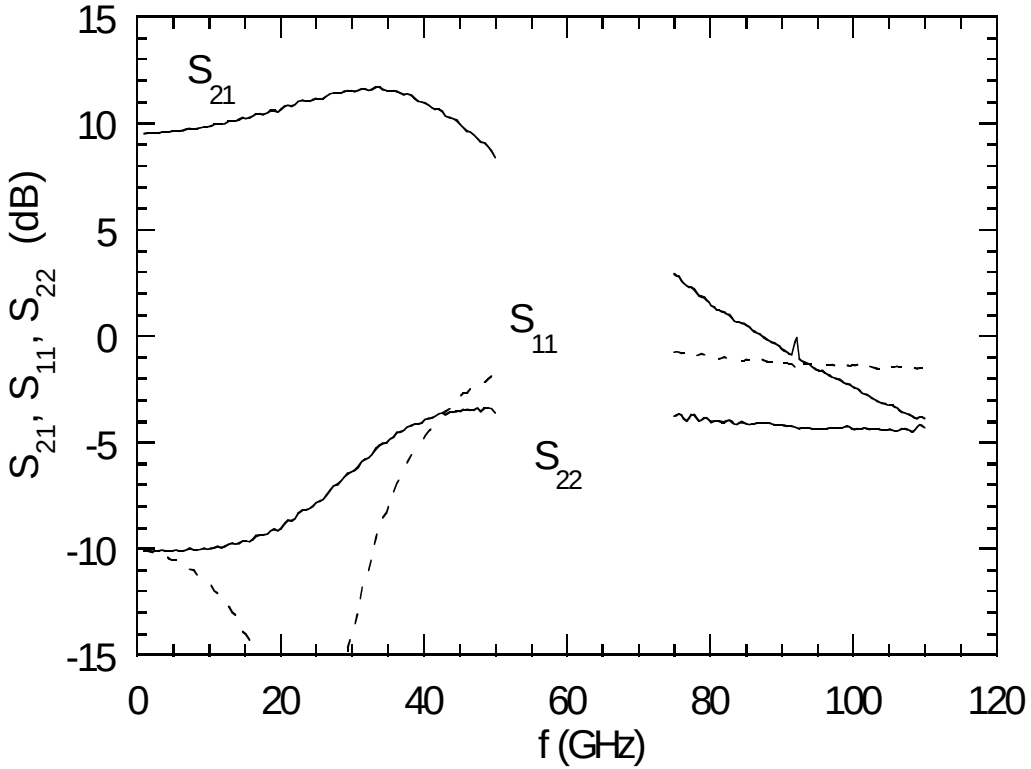


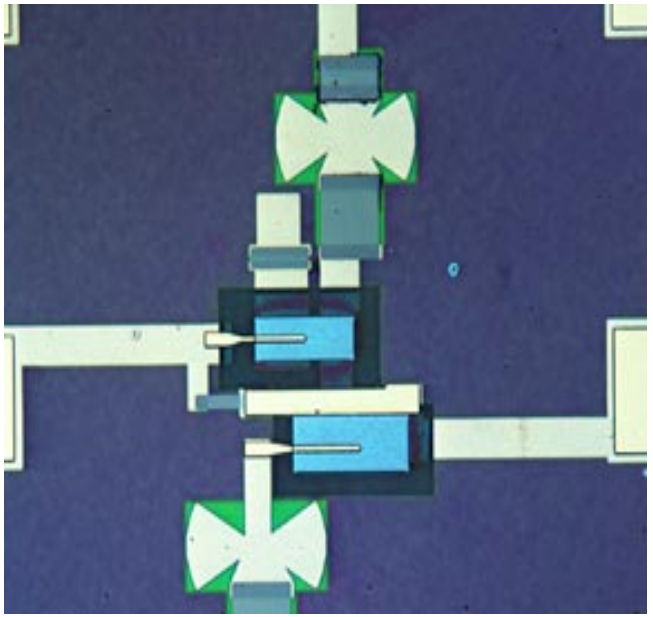
- Transistors in this work had relaxed geometry
- f_{max} of transferred substrate HBTs improves with lithographic scaling
- f_t over 250GHz, f_{max} over 800GHz demonstrated with transferred substrate HBTs

Low loss wiring at 100GHz



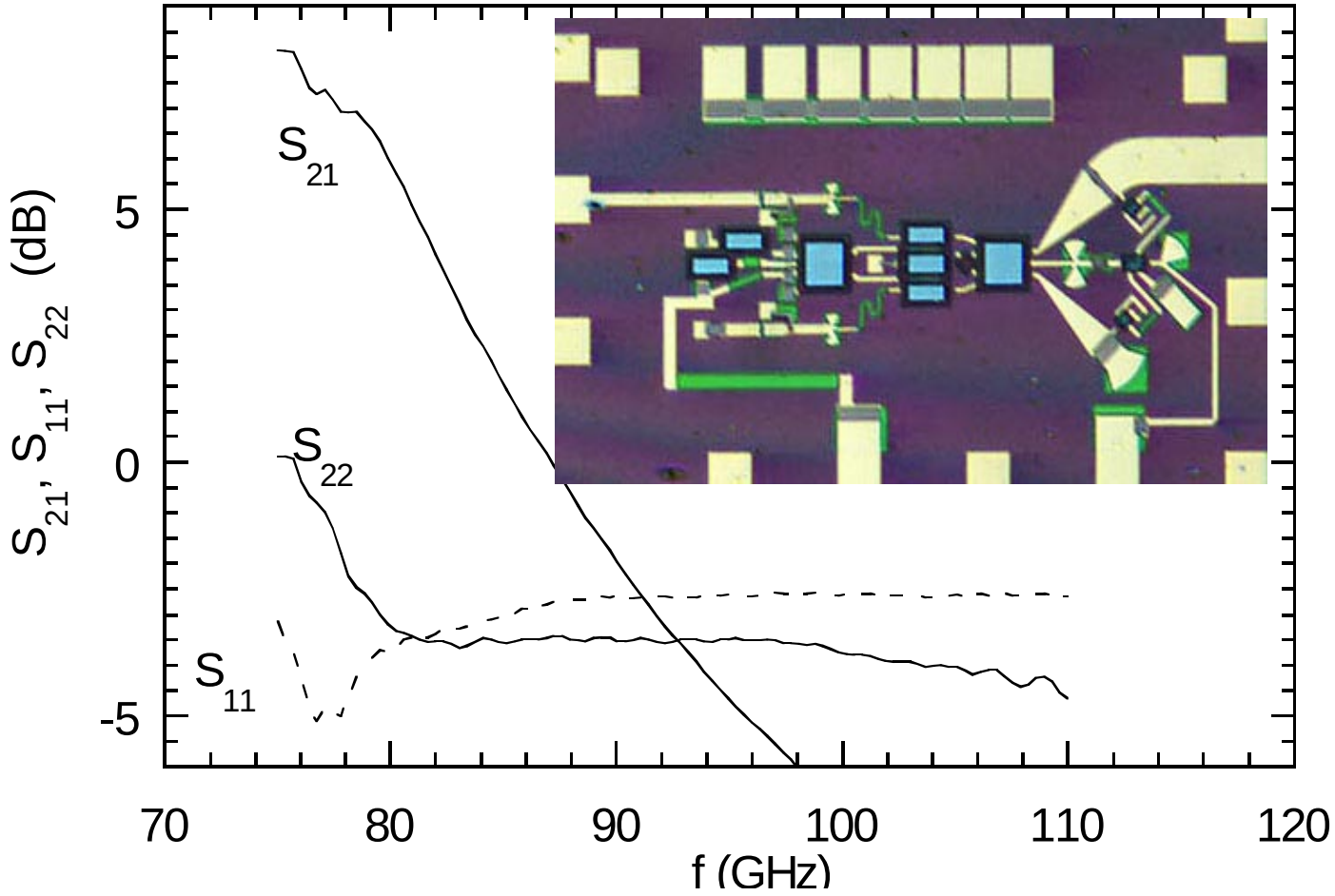
Darlington Feedback Amplifier





9.5dB gain DC to >50GHz

Differential Cascode Large Signal Amp



Measured S parameters, with respect to 50Ω characteristic Z_0, of differential cascode tuned amplifier.

Conclusions

- large fast ICs need thin wafers, microstrip
- our Cu substrate technology allows arbitrarily thin microstrip
- It also promises to solve heatsinking problem
- Furthermore, we can integrate scalable bipolar devices in our technology