11th International Conference on Indium Phosphide and Related Materials
16-20 May 1999 Davos, Switzerland

TuA1-1
(Invited)

Transferred-Substrate Heterojunction Bipolar Transistor Integrated Circuit Technology

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Abstract— **Using substrate transfer processes, we have fabricated heterojunction bipolar transistors with 0.4 μm emitter-base and collector-base junctions, minimizing RC parasitics and increasing f_{max} to 820 GHz, the highest yet reported for a transistor. The process provides microstrip interconnects on a low-ϵ_r polymer dielectric with a electroplated copper ground plane and substrate. Substrate thermal resistance is reduced 5:1 over InP. Important wiring parasitics, including wiring capacitance, ground via inductance, and IC-package ground-return inductance, are substantially reduced. Demonstrated ICs include lumped and distributed amplifiers with bandwidths to 85 GHz, master-slave flip-flops operable at over 48 GHz, and 50GHz AGC / limiting amplifiers. Current efforts include further improvement in bandwidth, development of power devices, and demonstration of more complex mixed-signal ICs.**

I. Introduction

APPLICATIONS –present & potential– for heterojunction bipolar transistors (HBTs) include RF/ microwave analog-digital conversion, microwave direct digital frequency synthesis, and fiber-optic transmission in the range of 40–120 Gigabits/second.

The motivation for high circuit bandwidth varies with the application. In fiber-optic transmission, fast ICs will directly enable increased time-division-multiplexed transmission rates, complementing increases in channel capacity provided by wavelength-division-multiplexing. For oversampled ($\Delta - \Sigma$) analog-digital converters, in-band quantization noise power decreases in proportion to the 5^{th} power of the oversampling ratio (2^{nd}-order modulators). Very high speed IC technologies offer the potential of $\Delta - \Sigma$ ADCs with clock frequencies in the 10's of GHz, providing high dynamic range –and large instantaneous bandwidth– over radio-frequencies and lower microwave frequencies. In direct digital frequency synthesis (DDS), increases in logic IC clock rates and DAC bandwidths will result in increased synthesizer bandwidth. Used in radar transmitters, modulation bandwidths can then be increased and frequency agility improved.

A 100 GHz clock rate IC technology would permit significant advances in the performance of such signal conversion ICs. To permit clock rates exceeding 100 GHz, significant issues in transistor design, interconnects, packaging, and thermal design must be addressed. The transistor current gain (f_T) and power gain (f_{max}) cutoff frequencies must be several hundred GHz. Wiring parasitics, including line capacitance per unit length, line delay per unit length, ground via inductance, and parasitic ground return inductance, must all be minimized. Ground via inductance ($\sim$ 12 pH, or j7.5 Ω at 100 GHz) in standard 100-μm-substrate microstrip MIMICs makes low-impedance source/emitter grounding difficult in > 100 GHz ICs. The interconnects must have low capacitance and low delay per unit length, and the wire lengths, hence transistor spacings, must be small. Given that fast HBTs operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then essential. To provide predictable performance, interconnects of more than a few ps length must have a controlled characteristic impedance. To prevent circuit-circuit interaction through ground-circuit common-lead inductance ("ground loops"), the IC technology must provide an integral low inductance –hence unbroken– ground plane for ground-return connections.

Ground-return inductance between the IC and package results in "ground bounce" and hence interaction between the IC's input and output lines. For ICs with top-surface (coplanar-waveguide) ground connections and multiple

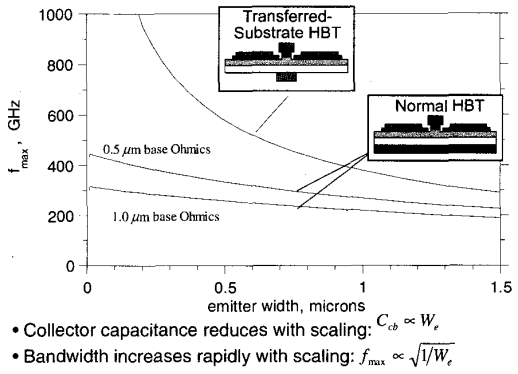

Fig. 1. Scaling of transferred-substrate and triple-mesa HBTs.

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input/output connections, ground bounce between IC and package will prevent 100 GHz operation. For an IC with N_{signal} signal lines of impedance Z_0, risetime ΔT, and voltage swing V_{signal}, and N_{ground} grounding bond wires of inductance $L_{\text{bond}} \simeq 0.6\text{pH}/\mu\text{m} \cdot 300\mu\text{m}$, the package-IC ground bounce is $V_{\text{bounce}} = V_{\text{signal}} N_{\text{signal}} L_{\text{bond}} / N_{\text{ground}} Z_0 \Delta T$. For ground bounce equal to 10% of the signal amplitudes, a 100-GHz clock rate IC must have $N_{\text{ground}}/N_{\text{signal}}$ =5–10, and 80%–90% of the IC bond-pads must be devoted to IC grounding. Reported 10 GHz clock rate ICs devote $\sim$ 50% of IC pads for grounding. For mixed-signal and communications ICs, signal coupling through ground bounce must be much smaller than 10% of the digital I/O interface levels. Consequently, common-lead inductance between the IC and package ground systems must be made vanishingly small.

II. Transferred-Substrate HBTs

Transferred-substrate HBT ICs [4] offer high transistor bandwidth, low wiring capacitance, and low wiring inductance. In this process a substrate transfer step permits two-side processing of the device epitaxial layers, allowing definition of a transistor with narrow and aligned emitter-base and collector-base junctions.

In HBTs, f_τ is primarily determined by the base transit time τ_b, the collector transit time τ_c, and the emitter charging time $C_{je}(kT/qI_e)$. Increases in f_τ are obtained by thinning the collector, by thinning and grading the base, and by increasing the emitter current density. Unfortunately, thinning the base and collector epitaxial layers increases the collector capacitance C_{cb} and the base resistance R_{bb}, decreasing $f_{max} = (f_\tau/8\pi R_{bb}C_{cbi})^{1/2}$. The base-collector junction is a distributed network and $R_{bb}C_{cbi}$ represents an effective, weighted time constant [1]. *For a fixed emitter stripe length* , decreasing the width W_e of the emitter-base junction decreases the base spreading resistance, but does not decrease the base contact resistance. Scaling W_e reduces R_{bb} towards a minimum set by the contacts. Decreasing the width of the base-collector junction W_c decreases C_{cb}.

In normal double-mesa HBTs (fig. 1), the collector-base junction and base Ohmic contact are defined in a single process step. The Ohmic contacts must be at least one contact transfer length, setting a minimum collector junction width, and a minimum collector capacitance. $R_{bb}C_{cb}$ has a minimum value, independent of lithographic limits, and f_{max} does not improve with scaling. In the transferred-substrate device, the collector width need only be larger than the emitter width. Reducing W_c and W_e progressively reduces $R_{bb}C_{cb}$, and f_{max} increases rapidly with scaling (fig. 1). With lateral scaling alone, f_{max} should exceed 1 THz as dimensions are scaled to $\sim$0.1 μm. Subsequently thinning the base and collector layers increases f_τ at the expense of f_{max}. Simultaneous high values for both f_τ and f_{max} are thus obtained.

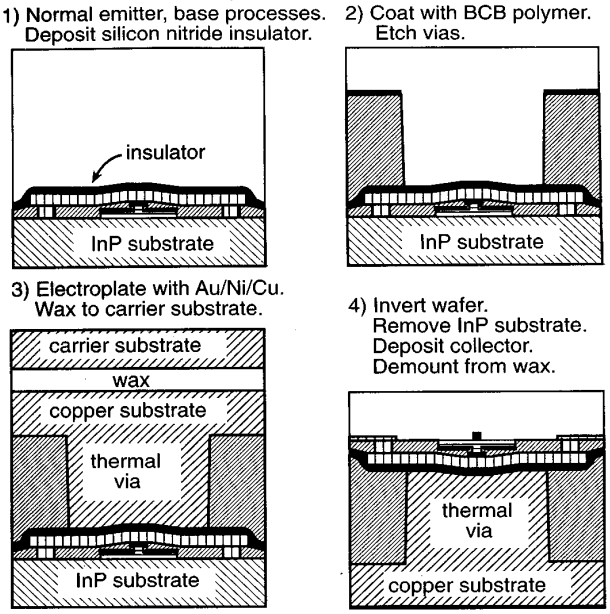

Fig. 2. Transferred-substrate HBT process flow.

In circuit design, a specific HBT emitter junction area is required, as determined by either required drive current or transconductance. With HBT emitter area fixed, C_{cb} is reduced in proportion to the ratio of collector to emitter junction areas. With emitter area fixed, reducing the emitter width 2:1 (hence increasing 2:1 the emitter stripe length) reduces the base contact resistance 2:1 and the base spreading resistance 4:1. In circuit application, the parasitics R_{bb} and C_{cb} are thus both reduced.

III. Growth and Fabrication

Fig. 3 shows a band diagram. The InGaAs base is typically 400 Å thick, has $2kT$ bandgap grading, and is Be-doped at $5{\cdot}10^{19}/\text{cm}^3$. The InGaAs collector is 2000-3000 Å thickness. A collector N^+ pulse-doped layer placed 400 Å from the base delays the onset of base push-out at high collector current densities. Devices typically use Schottky collector contacts [7], although HBTs with N+ subcollector layers (Ohmic-collector devices) have also been fabricated. While Ohmic-collector devices have non-zero collector series resistance, hence lower f_{max} [1], the 0.2 V barrier present in the Schottky-collector device increases the V_{ce} required to suppress base push-out at high current densities. Ohmic-collector devices thus show higher f_{max} under the low-V_{ce} conditions associated with current-mode-logic (CML). Schottky-collector devices are used for emitter-coupled-logic (ECL), where the operating V_{ce}

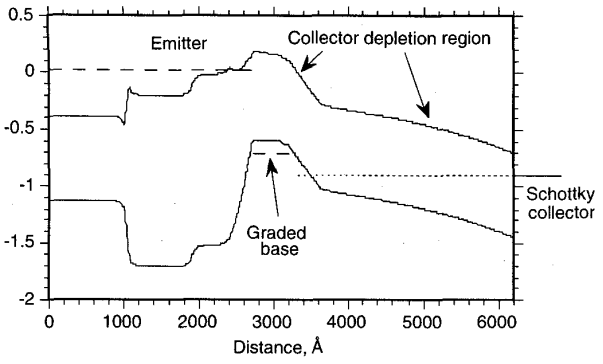

Fig. 3. Band diagram, under bias, of a typical device.

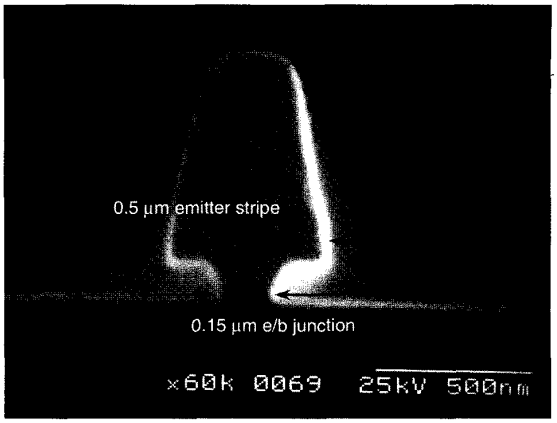

Fig. 4. Cross-section of emitter-base junction. The 0.5 μm emitter metal was defined with a projection lithography system.

is higher.

Figure 2 shows the process flow. Standard fabrication processes [3] define the emitter-base junction, the base mesa, polyimide planarization, and the emitter contacts. The substrate transfer process commences with deposition of the PECVD Si_3N_4 insulator layer and the Benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness). Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metalize the vias and to form the ground plane. In a process step similar to that used for mm-wave HEMT ICs, the wafer is temporarily wax-bonded to a Si carrier substrate. The InP substrate is removed in HCl and Schottky collectors are deposited, completing the process. The resulting composite Cu/polymer IC is then demounted from the Si wafer by dissolving the wax.

The transferred-substrate process permits high device bandwidths f_{max} through simultaneous scaling of emitter and collector junctions. For the emitter-base junction, deep submicron scaling requires tight control of lateral undercutting during the base contact recess etch. To form the emitter, reactive-ion etching in CH_4 / H_2 / Ar, monitored with a HeNe laser, first removes the N^+ GaInAs emitter contact layer. A HCl/HBr/Acetic selective wet etch then removes the AlInAs emitter, stopping on the AlInAs/GaInAs emitter-base grade. By etching at 10° C, the etch rate is slowed, and a controlled emitter undercut is formed. The undercut both narrows the emitter and serves (as normal) to define the liftoff edge in the self-aligned base contact deposition. A timed 30 s nonselective wet Citric/H_3PO_4/H_2O_2 etch then removes the base- emitter grade. Etch selectivity in both the RIE and HCl/HBr/Acetic etches aids in etch-depth control, and we are able to reproducibly etch ~100 Å into the base without use of surface contact resistance probing as a process monitor. Figure 4 shows the cross-section of a 0.15-μm emitter-base junction.

In defining submicron collector-base junctions, use of the Schottky-collector contact eliminates the need for an etch of similar precision through an N^+ collector Ohmic contact layer. The collector junction is defined by the stripe width of the deposited metal. Subsequent to collector deposition, a self-aligned wet etch of ~500 Å depth removes the collector junction sidewalls (eliminating fringing fields) and reduces the collector junction width by ~1000 Å . The step, intended to reduce C_{cb}, generally provides a greater increase f_{max} than would be expected from the observed reduction in collector junction width.

In addition to HBTs with narrow emitter and collector stripes, the process provides thermal vias for HBT heatsinking, NiCr resistors, Si_3N_4 MIM capacitors, and microstrip wiring on a ϵ_r=2.7 dielectric with vias, ground plane, and 3 levels of interconnects. At 5 μm length, the grounding vias are 20:1 shorter than in typical 100-μm-substrate microstrip MIMICs, reducing ground via inductance by over an order of magnitude. With a package-IC ground interface over the full IC back surface, the package-chip ground inductance is very low [5].

The process provides effective heatsinking (395 W/M · K for Cu *vs.* 74 for InP), permitting a 5:1 increase in transistor packing density (e.g. a 5:1 increase in dissipation per unit IC die area) for a given allowable substrate temperature rise. Presently, thermal resistance is dominated by temperature gradients internal to the transistor itself, arising from the low thermal conductivity of the InAlAs emitter and InGaAs base and collector layers. Thus, allowable power per unit HBT emitter area remains comparable to mesa HBTs. For power transferred-substrate HBTs, use of high-thermal-conductivity InP emitter and

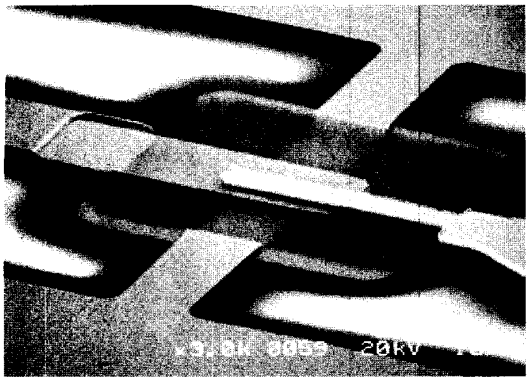

Fig. 5. Transferred-substrate HBT defined by contact lithography

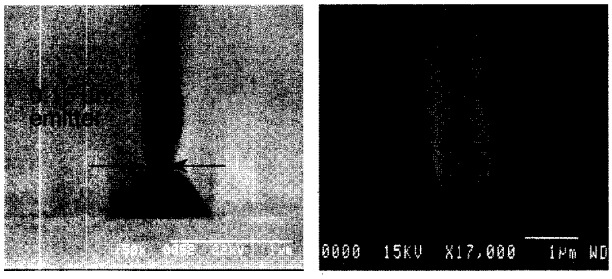

Fig. 6. E-beam HBT: test structure with 0.15 μm emitter-base junction (a), and 0.4 μm Schottky collector stripe (b)

collector epitaxial layers will greatly increase allowable power per unit HBT junction area. This is being pursued. To tolerate high power densities, the NiCr resistors must have thermal vias, which results in significant parasitic capacitance. Pull-up resistors in ECL do not require the thermal via.

Presently 70-device ICs have been fabricated at high yields and low process failure rates, and ICs fabricated on full 2 inch copper wafers. The most significant process difficulty is dimensional change of the wafer during substrate transfer. Presently wafers show $3 \cdot 10^{-4}$ fractional expansion after transfer, resulting in ± 0.5 μm misregistration (during collector lithography) at the edges of the stepper exposure field if a 3 mm reticle is employed. The stress may be caused by the BCB, the electroplated Cu, or (strongly suspected) the mounting wax. Solutions include stress reduction through replacement of offending layers, stress compensation layers, or adjusting the dimensions of the collector mask. At the expense of increased effort during collector lithography, a smaller exposure reticle size can be used for the collector lithography than for the steps preceding substrate transfer. This method was used for devices fabricated using electron-beam lithography.

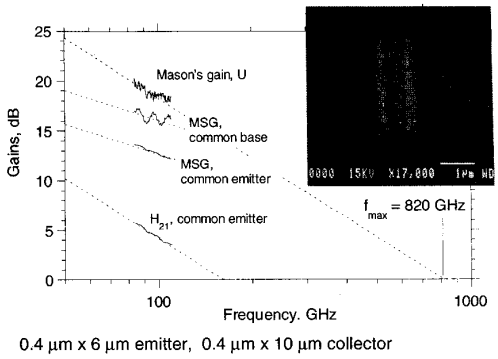

Fig. 7. W-band gains of device with a 0.4 μm $\times$ 6 μm emitter and a 0.4 μm $\times$ 10 μm collector.

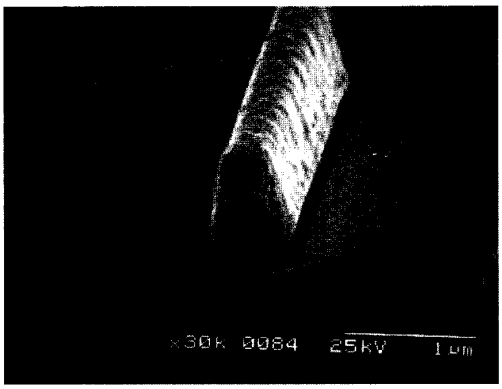

Fig. 8. SEM from emitter side of a stepper-defined HBT with a 0.2 μm $\times$ 6 μm emitter.

IV. Device Performance

Devices have been fabricated using contact lithography at 1–2 μm resolution, using a 0.5 μm stepper, and using electron-beam lithography. Fig. 5 shows a device with a 0.6μm by 8μm emitter and a 1.6μm by 12μm collector. The device exhibits 215 GHz peak f_τ, and peak f_{max} above 400 GHz. Figure 6 shows HBT emitter-base and collector-base junctions defined by electron-beam lithography. Submicron devices fabricated by E-beam lithography (fig. 7) exhibit 820 GHz. f_{max} [6]. Neither contact lithography nor electron-beam lithography is suitable for fabrication of large ICs. We have fabricated HBT ICs using a 0.5 μm projection lithography system, and have obtained $>$ 600 GHz f_{max} (fig. 8).

With the exception of reactively-tuned circuits, for which f_{max} is the sole determinant of circuit bandwidth, circuit design generally requires high values for both f_τ and f_{max}. Examining significant terms in $1/2\pi f_\tau$ (fig. 9), with base bandgap grading, $\tau_b + \tau_c$ is small at 0.4–0.5 ps,

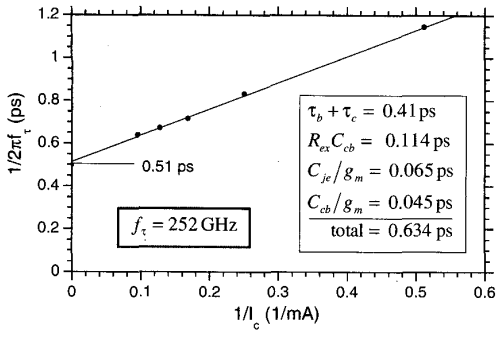

Fig. 9. HBT forward transit delay *vs.* inverse emitter current for an HBT with a 2000 Å thick collector and a 400 Å thick base with $2kT$ bandgap grading. *RC* charging terms are significant in determining f_τ

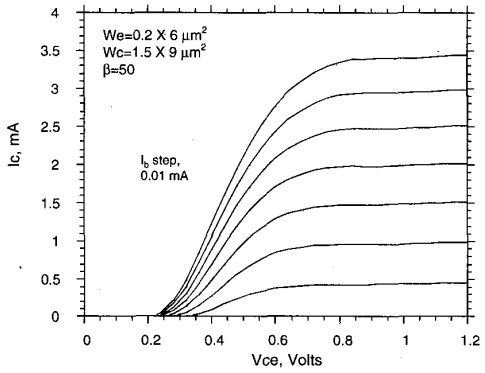

Fig. 10. Common-emitter characteristics for device defined by optical projection lithography. As a result of the 400 Å base with $2kT$ grading, β =50 is obtained even with a 0.2 μm emitter width.

while the Schottky collector eliminates R_cC_{cb}. At peak f_τ bias, $(C_{je} + C_{cb})/g_m \simeq 0.1$ps. Presently $R_{ex}C_{cb} \simeq 0.1$ ps, and has significant impact upon f_τ. With thinner collector layers, $R_{ex}C_{cb}$ increases. To obtain > 300 GHz f_τ, base bandgap grading must be increased, the collector thinned, and InAs emitter Ohmic contact layers employed.

Device scaling also reduces D.C. current gain and breakdown voltage. Base current in narrow-emitter InAlAs/InGaAs HBTs is predominantly due to conduction on the exposed InGaAs base surface between the emitter mesa and the base Ohmic contact. β decreases with emitter width, but increases as the base is thinned, as base bandgap grading is increased, and (at the expense of f_{max}) as the emitter- base spacing is increased. $\beta > 50$ has been obtained with 0.2 μm emitters (fig. 10). Using 0.7 μm emitters and 300 Å base thickness with $2kT$ grading , $\beta \simeq 200$ is obtained. By proportionally scaling the base thickness, adequate current gain is obtained even for deep submicron emitters.

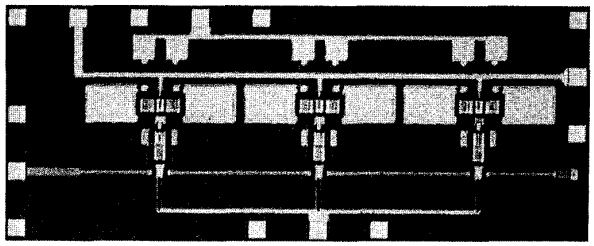

Fig. 11. Distributed amplifier in the transferred-substrate process. The amplifier exhibits 7 dB gain and 85 GHz bandwidth

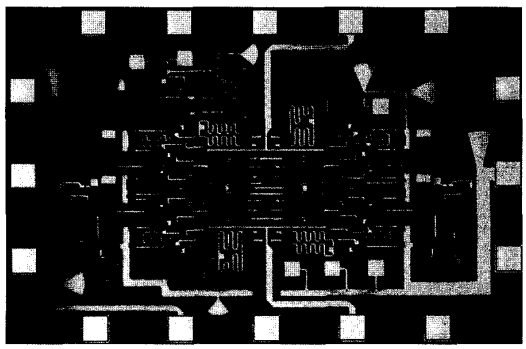

Fig. 12. High speed master-slave flip-flop. The IC contains 70 HBTs.

The 3000 Å InGaAs collectors have very low breakdown, 1.5 V BV_{ceo}, 2 V BV_{cbo} *at* 1–2 $\cdot 10^5$ A/cm^2 *current density.* The HBT output conductance is primarily collector-base (*vs.* collector-emitter) conductance, likely due to collector impact ionization. Clearly, InP collectors should be used for highly scaled devices. To this end, we have recently acquired a Phosphorous source for MBE growth of InP. The high f_τ observed with InGaAs-collector HBTs is due to velocity overshoot ($\sim 4 \cdot 10^7$ cm/s for 0.3 μm) in collector layers thinner than ~0.5 μm. InP-collector devices will obtain bandwidths comparable to the InGaAs-collector devices only if comparable velocity overshoot is obtained. The high inter-valley energy separation of InP is cause for optimism.

V. Integrated Circuits

Initial digital ICs consisted of ECL and CML master-slave D flip-flops, configured as 2:1 static frequency dividers [9]. Using devices with 0.6 μm × 8μm emitters and 1.6 μm × 12 μm collectors, the ICs operated at maximum

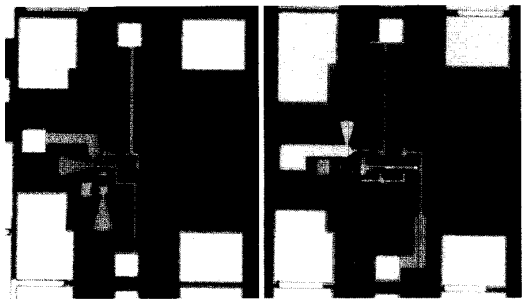

Fig. 13. Resistive feedback amplifiers with (a) 15.6 dB gain and DC-60 GHz bandwidth and (b) 6.7 dB gain and DC-85 GHz bandwidth.

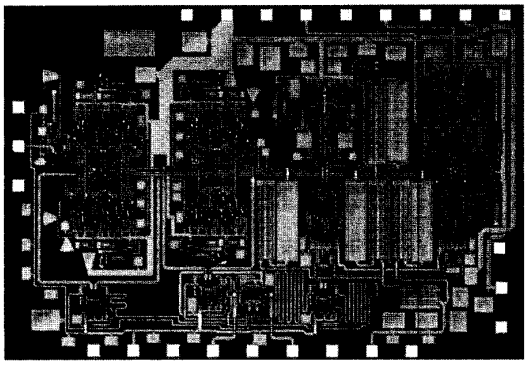

Fig. 14. Photograph of (as yet untested) Δ–Σ ADC fabricated in the transferred-substrate process. The IC contains approximately 350 HBTs.

clock frequencies 47 GHz (CML) and 48 GHz (ECL) and dissipated 380 mW (ECL) or 75 mW (CML) from a -5 V supply. More recent designs using submicron devices [10] (fig. 12) operate at considerably higher frequencies.

Demonstrated analog ICs include 85 GHz distributed amplifiers (fig. 11), 50 GHz broadband differential amplifiers for optical fiber receivers, 80 GHz reactively-tuned amplifiers, and broadband Darlington and f_τ - doubler resistive feedback amplifiers [11] (fig.13). Current efforts include development of much larger ICs, including adder-accumulators and Sine ROMs for direct digital frequency synthesis and Δ–Σ ADCs (fig. 14).

VI. Conclusions

100 GHz digital ICs require a high-bandwidth transistor, low-parasitic interconnects, and effective heatsinking. Using substrate transfer processes, HBTs can be fabricated with highly scaled lithographic and epitaxial dimensions, giving both high f_τ and high f_{max}. With further scaling and improved circuit design, 300 GHz analog and 100 GHz digital ICs will be feasible.

Acknowledgments

We acknowledge the efforts of key past UCSB students (B. Agarwal, U. Bhattacharya, R. Pullela), and the guidance of W. Stanchina and J. Jensen (HRL) and H. Kroemer (UCSB). Work at UCSB supported by the ONR under grants N00014-98-1-0068, N00014-99-10041, and N00014-98-1-0830 (J. Zolper, M. Yoder, D. VanVechten), by the AFOSR under grant F4962096-1-0019 (H. Schlossberg), and by the ARO under the Quasi-Optical MURI (J. Harvey). JPL work was performed at the Center for Space Microelectronics Technology, JPL, Caltech, and sponsored by the NASA office of Space Science

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