Submicron Transferred-Substrate Heterojunction Bipolar Transistors with greater than 1 THz f_{max}

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We report transferred-substrate heterojunction bipolar transistors (HBTs) with 19.6 dB unilateral gain and 5.4 dB short-circuit current gain at 110 GHz (fig. 1). Extrapolating at -20 dB/decade, the power gain cut-off frequency f_{max} is 1080 GHz and the current gain cut-off frequency f_τ is 204 GHz. The record high f_{max} results from the scaling of HBT junction widths, from the elimination of collector series resistance through the use of a Schottky collector contact, and from partial screening of the collector-base capacitance by the collector space charge [1].

The MBE layer structure and the fabrication process are similar to [1]. The devices were characterized by on-wafer network analysis from 0 to 50 GHz and 75 to 110 GHz. On wafer calibration standards were used to de-embed the transistor S-parameters [1]. The standard Line-reflect-line technique was used, with microstrip through line, extended lines for 20 to 50 GHz and 75 to 110 GHz calibration, and offset shorts & opens for the reflect standard and for verification. The calibration verification shows open and short circuits accurate to $\sim$ 0.2 dB magnitude and $\sim$ 3 degrees phase. Devices with 0.4 μm emitter and 0.7 μm collector widths obtained 204 GHz f_τ and record 1080 GHz peak f_{max} at V_{ce} = 1.2 V (fig. 1). In addition to the 10:1 extrapolation in frequency to 1.08 THz f_{max} , the very high power gain at 110 GHz also results in significant measurement variability, with repeated calibrations at the same bias point give f_{max} varying from 1.0 to 1.3 THz. 140 to 220 GHz network analyzers are being purchased by both UCSB and JPL, and will soon be available for measurements over an extended frequency range.

Fig. 2 and Fig. 3 show the variation of f_τ and f_{max} with bias. The total collector-base capacitance C_{cb} is extracted by plotting the imaginary part of the admittance parameter Y_{12} versus frequency. Inclusive of the differential space-charge effect [2], [3], observed earlier in MESFETs [4], $C_{cbi} = \epsilon A_E/T_c - I_c \partial\tau_c/\partial V_{ce}$, where T_c is collector thickness and $\partial\tau_c/\partial V_{ce}$ is the variation in collector transit time with bias. The measured f_τ vs. V_{ce} (fig. 3) indicates $\partial\tau_c/\partial V_{ce} \sim 0.18$ ps/Volt, predicting $\sim$ 0.9 fF reduction in C_{cbi} from I_c = 1 mA to I_c = 6 mA. Consistent with this, the total C_{cb} determined from Y_{12} (fig. 4) shows a 0.64 fF decrease between 1 mA and 6 mA I_c. Figure 5 shows a small-signal hybrid-π model for the device at I_c = 6 mA and V_{ce} = 1.2 V. At this bias point, C_{cbi} = 0.18 fF is determined by fitting to the measured unilateral gain. The measured S-parameters (fig. 6), h_{21} and U show good correlation to that of the hybrid-π model.

f_{max} increases in proportion to the inverse square root of both the junction widths and the base resistance. With improved alignment, 0.1 μm emitter and collector dimensions should be feasible. Using a CBr_4 doping source, $> 10^{20}/\text{cm}^3$ carbon base doping is feasible, improving by 3:1 both the base sheet and base contact resistance. These enhancements should result in a transistor with 2-3 THz f_{max} and reactively-tuned transistor amplifiers operating at 500-1000 GHz

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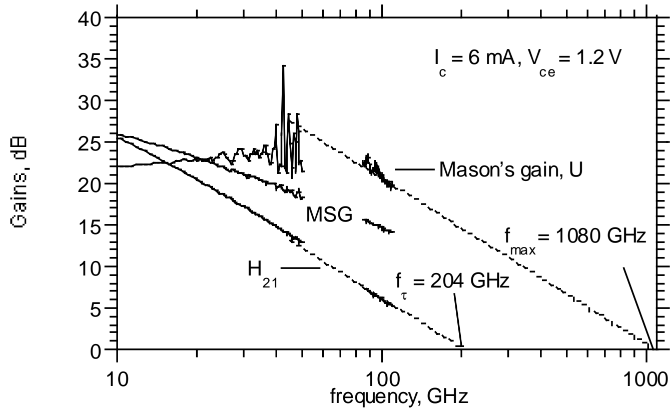

Fig. 1: Gains of 0.4 x 6 μm^2 emitter and 0.7 x 10 μm^2 collector HBT. Theoretical -20 dB/dec. (H_{21}, U) gain slopes are indicated.

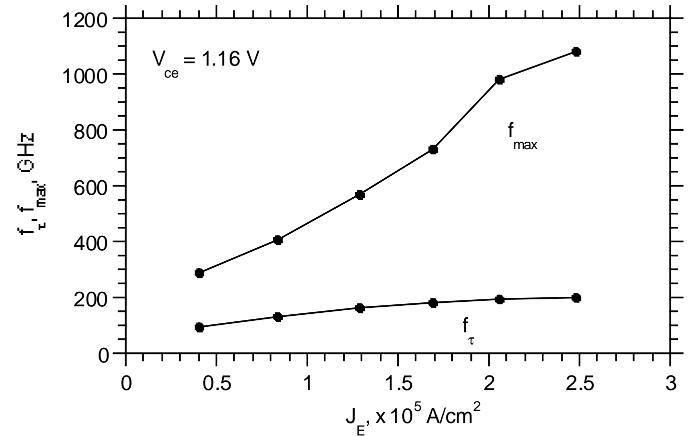

Fig. 2: Variation of f_t and f_{max} with emitter current density

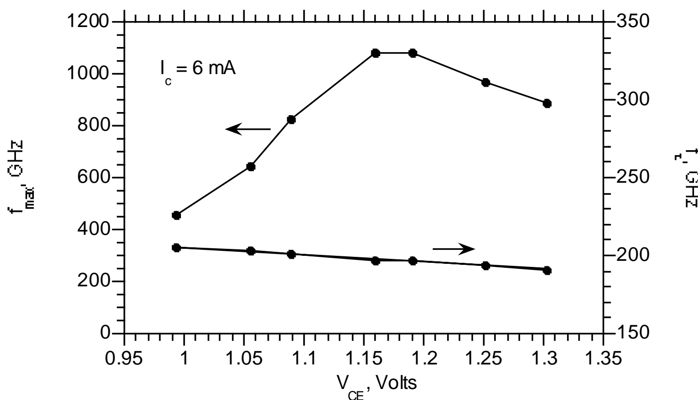

Fig. 3: Variation of f_t and f_{max} with collector-emitter voltage.

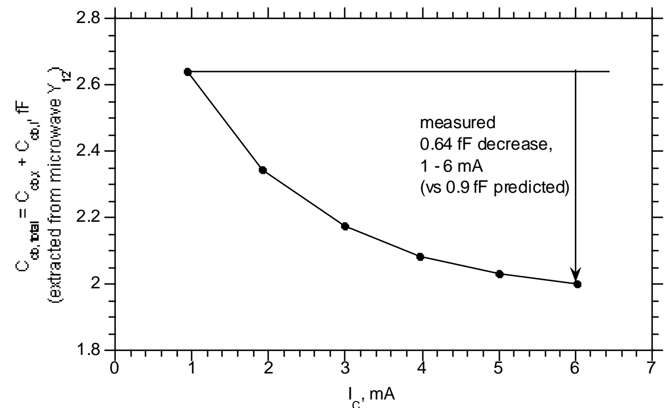

Fig. 4: Collector-base capacitance extracted from Y-parameters vs emitter current.

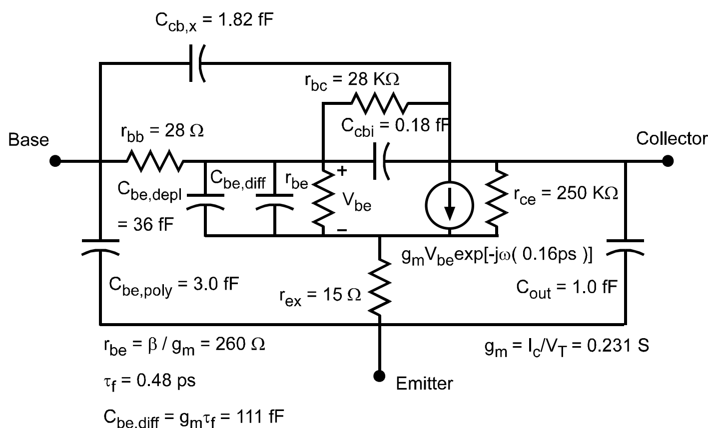

Fig. 5: Device equivalent circuit model at V_{ce} = 1.2 V and I_c = 6 mA.

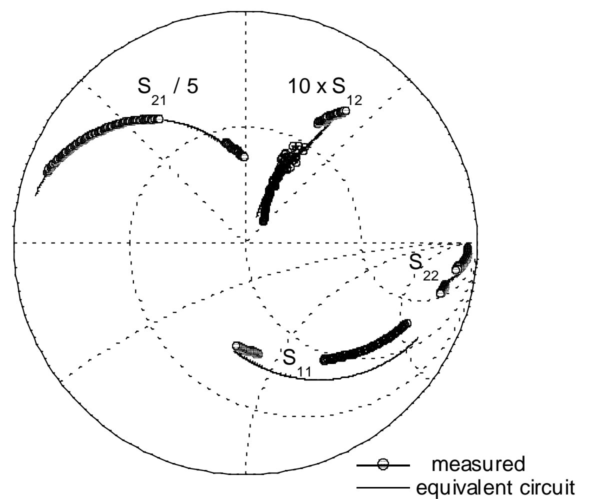

Fig. 6: Measured device S-parameters at V_{ce} = 1.2 V and I_c = 6 mA. The solid line represents S-parameters of the equivalent circuit model.