Ultra high frequency HBT integrated circuits

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Abstract— **Using substrate transfer processes, we have fabricated heterojunction bipolar transistors with submicron emitter- base and collector-base junctions, minimizing *RC* parasitics and increasing f_{max} to 500 GHz. The process also provides a microstrip wiring environment on a low- ϵ_r dielectric substrate. Demonstrated small-scale ICs in the process include lumped and distributedamplifiers with bandwidths to 85 GHz, 48 GHz static frequency dividers, and 50GHz AGC / limiting amplifiers.**

Keywords— **heterojunction bipolar transistor, HBT, transferred-substrate**

I. Introduction

APPLICATIONS –present & potential– for heterojunction bipolar transistors (HBTs) include RF/ microwave analog-digital conversion, microwave direct digital frequency synthesis, and fiber-optic transmission in the range of 40–120 Gigabits/second.

The motivation for high circuit bandwidth varies with the application. In fiber-optic transmission, fast ICs will directly enable increased time-division-multiplexed transmission rates, complementing increases in channel capacity provided by wavelength-division-multiplexing. For oversampled ($\Delta - \Sigma$) analog-digital converters, in-band quantization noise power decreases in proportion to the 5^{th} power of the oversampling ratio (2^{nd}-order modulators). Very high speed IC technologies offer the potential of $\Delta - \Sigma$ ADCs with clock frequencies in the 10's of GHz, providing high dynamic range –and large instantaneous bandwidth– over radio-frequencies and lower microwave frequencies. In direct digital frequency synthesis (DDS), increases in logic IC clock rates and DAC bandwidths will result in increased synthesizer bandwidth. Used in radar transmitters, modulation bandwidths can then be increased and frequency agility improved.

A 100 GHz clock rate IC technology would permit significant advances in the performance of such signal conversion ICs. To permit clock rates exceeding 100 GHz, significant issues in transistor design, interconnects, packaging, and thermal design must be addressed. The transistor current gain (f_τ) and power gain (f_{max}) cutoff frequencies must be several hundred GHz. Wiring parasitics must be minimized. The interconnects must have small inductance and capacitance per unit length, and the wire lengths, hence transistor spacings, must be small. Given that fast HBTs operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then essential. To provide predictable performance, interconnects of more than a few ps length must have a controlled characteristic impedance. To prevent circuit-circuit interaction through ground-circuit common-lead inductance ("ground loops"), the IC technology must provide an integral ground plane for ground-return connection. Similarly, to prevent circuit-circuit interaction between the IC's input and output lines, common-lead inductance between the IC and package ground systems must be made vanishingly small.

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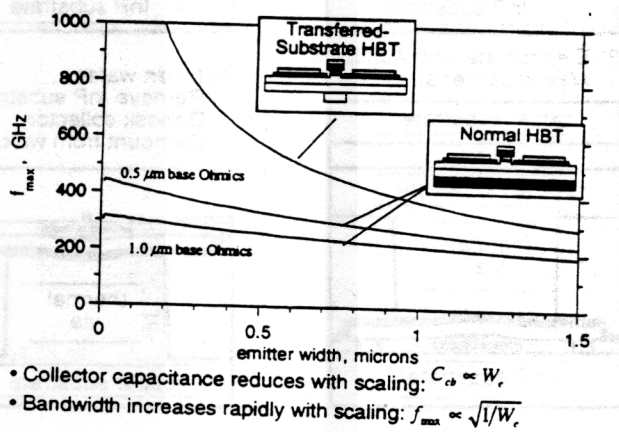

Fig. 1. Scaling of transferred-substrate and triple-mesa HBTs.

II. Transferred-Substrate HBTs

Transferred-substrate HBT ICs [3] offer high transistor bandwidth, low wiring capacitance, and low wiring inductance. In this process a substrate transfer step permits two-side processing of the device epitaxial layers, allowing definition of a transistor with narrow and aligned emitter-base and collector-base junctions.

In HBTs, f_τ is primarily determined by the base transit time τ_b, the collector transit time τ_c, and the emitter charging time $C_{je}(kT/qI_e)$. Increases in f_τ are obtained by thinning the collector, by thinning and grading the base, and by increasing the emitter current density. Unfortunately, thinning the base and collector epitaxial layers increases the collector capacitance C_{cb} and the base resistance R_{bb}, decreasing $f_{max} = (f_\tau/8\pi R_{bb}C_{cbi})^{1/2}$. The base-collector junction is a distributed network and $R_{bb}C_{cbi}$ represents an effective, weighted time constant. *For a fixed emitter stripe length* , decreasing the width W_e of the emitter-base junction decreases the base spreading resistance, but does not decrease the base contact resistance. Scaling W_e reduces R_{bb} towards a minimum set by the contacts. Decreasing the width of the base-collector junction W_c decreases C_{cb}.

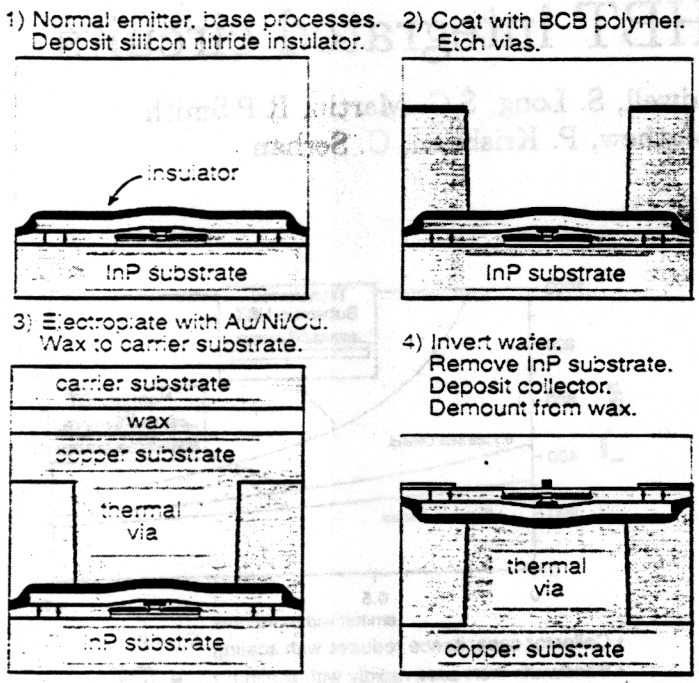

Fig. 2. Transferred-substrate HBT process flow.

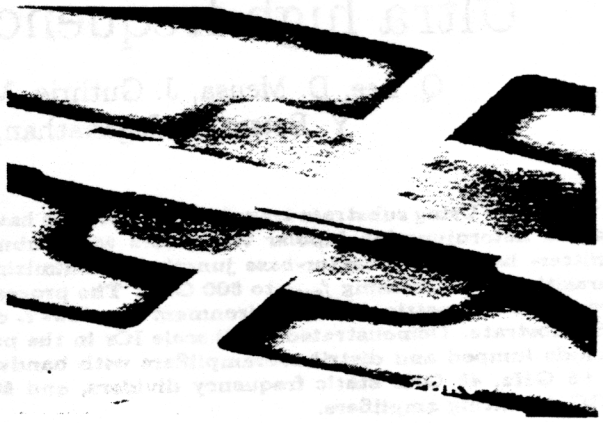

Fig. 3. Transferred-substrate HBT defined by contact lithography

In normal double-mesa HBTs (fig. 1), the collector-base junction and base Ohmic contact are defined in a single process step. The Ohmic contacts must be at least one contact transfer length, setting a minimum collector junction width, and a minimum collector capacitance. $R_{bb}C_{cb}$ has a minimum value, independent of lithographic limits, and f_{max} does not improve with scaling. In the transferred-substrate device, the collector width need only be larger than the emitter width. Reducing W_c and W_e progressively reduces $R_{bb}C_{cb}$, and f_{max} increases rapidly with scaling (fig. 1). With lateral scaling alone, f_{max} should approach 1 THz as dimensions are scaled to ~0.1 μm. Subsequently thinning the base and collector layers increases f_τ at the expense of f_{max}. Simultaneous high values for both f_τ and f_{max} are thus obtained.

III. Growth and Fabrication

We first describe the HBT layer structure. The InGaAs base is nominally 400-500 Å thick, has kT–$2kT$ bandgap grading, and is Be-doped at $5{\cdot}10^{19}/\mathrm{cm}^3$. The InGaAs collector is 2000-3000 Å thickness. A collector N^+ pulse-doped layer placed 400 Å from the base delays the onset of base pushout at high collector current densities. Devices typically use Schottky collector contacts [6], although HBTs with N+ subcollector layers (Ohmic-collector devices) have also been fabricated. While Ohmic-collector devices have non-zero collector series resistance, hence lower f_{max}, the 0.2 V barrier present in the Schottky-collector device increases the V_{ce} required to suppress base pushout at high current densities. Ohmic-collector devices thus show higher f_{max} under the low-V_{ce} conditions associated with current-mode-logic (CML). Schottky-collector devices are used for emitter-coupled-logic (ECL), where the operating V_{ce} is higher.

Figure 2 shows the process flow. Standard fabrication processes [2] define the emitter-base junction, the base mesa, polyimide planarization, and the emitter contacts. The substrate transfer process commences with deposition of the PECVD Si_3N_4 insulator layer and the Benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness). Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metalize the vias and to form the ground plane. In a process step similar to that used for mm-wave HEMT ICs, the wafer is temporarily wax-bonded to a Si carrier substrate. The InP substrate is removed in HCl and Schottky collectors are deposited, completing the process. The resulting composite Cu/polymer IC is then demounted from the Si wafer by dissolving the wax.

In addition to HBTs with narrow emitter and collector stripes, the process provides thermal vias for HBT heatsinking, NiCr resistors, Si_3N_4 MIM capacitors, and microstrip wiring on a ϵ_r=2.7 dielectric with vias, ground plane, and 3 levels of interconnects. To tolerate high power densities, the NiCr resistors must have thermal vias, which results in significant parasitic capacitance. Pull-up resistors in ECL do not require the thermal via.

The process provides highly effective heatsinking (395 W/M · K for Cu vs. 74 for InP) and, with a package-IC ground interface over the full IC back surface, very low package-chip ground inductance [4]. Presently 100-device ICs can be fabricated at high yields on full 2 inch wafers (fig. 5).

IV. Device Performance

Devices have been fabricated using contact lithography at 1–2 μm resolution, using a 0.5 μm stepper, and using electron-beam lithography. Fig. 3 shows a device with a 0.6μm by 8μm emitter and a 1.6μm by 12μm collector. The device exhibits 215 GHz peak f_τ, and peak f_{max} above 400 GHz. Figure 4 shows HBT emitter-base and collector-base junctions defined by electron-beam lithography. Submicron devices fabricated by E-beam lithography (fig. 6) exhibit 500 GHz. f_{max} [5]. Neither contact lithography nor electron-beam lithography is suitable for fabrication

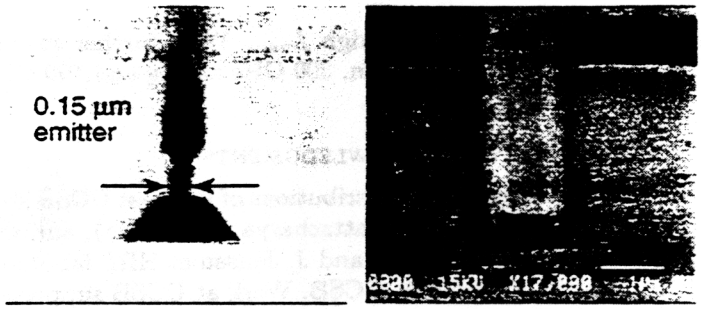

Fig. 4. E-beam HBT: test structure with 0.15 μm emitter-base junction (a), and 0.4 μm Schottky collector stripe (b)

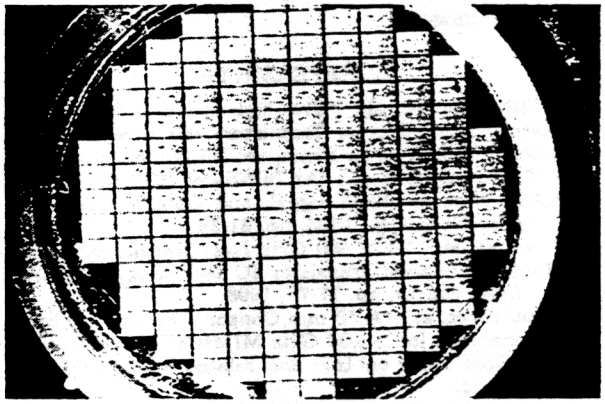

Fig. 5. Full 2 inch diameter transferred-substrate HBT wafer on copper-polymer substrate.

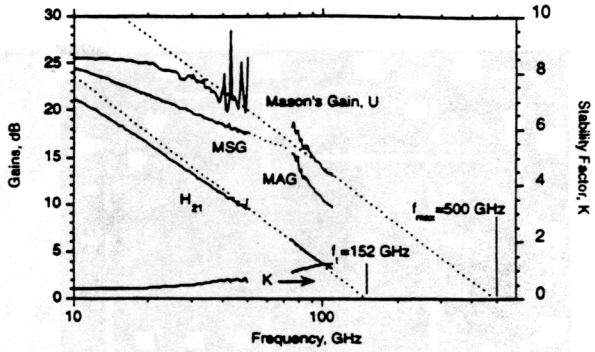

Fig. 6. W-band gains of device with a 0.4 μm × 25 μm emitter and a 1.0 μm × 29 μm collector.

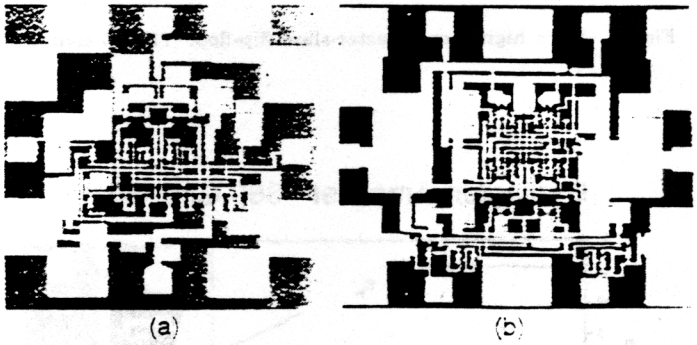

Fig. 7. CML (a) and ECL (b) master-slave D-flip-flops.

of large ICs. We also have fabricated HBT ICs using a 0.5 μm projection lithography system, and have obtained $>$ 500 GHz f_{max}.

With the exception of reactively-tuned circuits, for which f_{max} is the sole determinant of circuit bandwidth, circuit design generally requires high values for both f_τ and f_{max}. Examining significant terms in $1/2\pi f_\tau$, with base bandgap grading, $\tau_b + \tau_c$ is small at 0.4–0.5 ps, while the Schottky collector eliminates $R_c C_{cb}$. At peak f_τ bias, $(C_{je} + C_{cb})/g_m \simeq 0.1$ps. Presently $R_{ex}C_{cb} \simeq 0.1$ ps, and has significant impact upon f_τ. To obtain $>$ 300 GHz f_τ, base bandgap grading must be increased, the collector thinned, and InAs emitter Ohmic contact layers employed.

V. Integrated Circuits

As first digital IC demonstrations, we fabricated ECL and CML master-slave D flip-flops, configured as 2:1 static frequency dividers [8]. Circuits were fabricated using contact lithography, producing devices with 0.6 μm × 8μm emitters and 1.6 μm × 12 μm collectors. Circuit design is entirely standard. The CML divider uses series-gated master and slave latches. Emitter-follower buffers are added to the CML clock and data ports to form the ECL divider. The ICs (fig. 7) operated at maximum clock frequencies of 47 and 48 GHz and dissipated 380 mW (ECL) or 75 mW (CML) from a -5 V supply. More recent designs using submicron devices [9] (fig. 9)operate at the considerably higher frequencies.

Various analog ICs have been demonstrated in the process, including 85 GHz distributed amplifiers (fig. 8), 50 GHz broadband differential amplifiers for optical fiber receivers, 80 GHz reactively-tuned amplifiers, broadband Darlington feedback amplifiers (fig. 10), and very broadband f_τ - doubler feedback amplifiers. (fig. 11).

VI. Conclusions

100 GHz digital ICs require a high-bandwidth transistor, low-parasitic interconnects, and effective heatsinking. Using substrate transfer processes, HBTs can be fabricated with highly scaled lithographic and epitaxial dimensions,

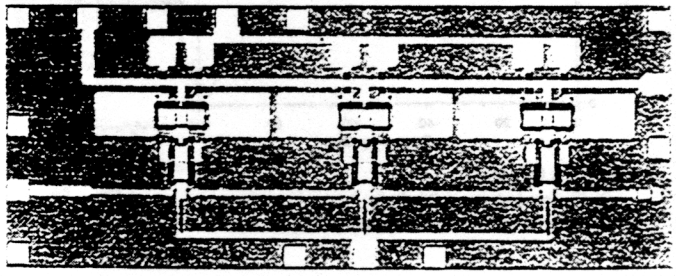

Fig. 8. Distributed amplifier in the transferred-substrate process. The amplifier exhibits 7 dB gain and 85 GHz bandwidth

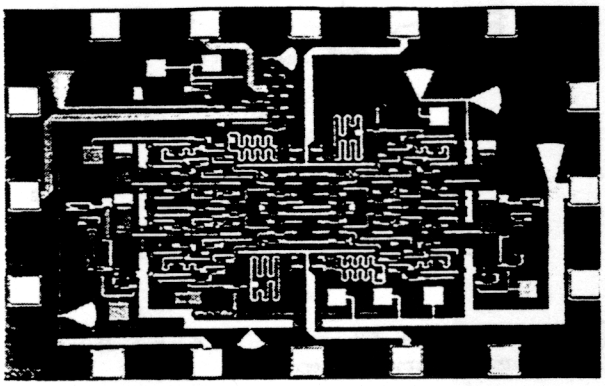

Fig. 9. Ultra high speed master-slave flip-flop. The IC contains 70 HBTs.

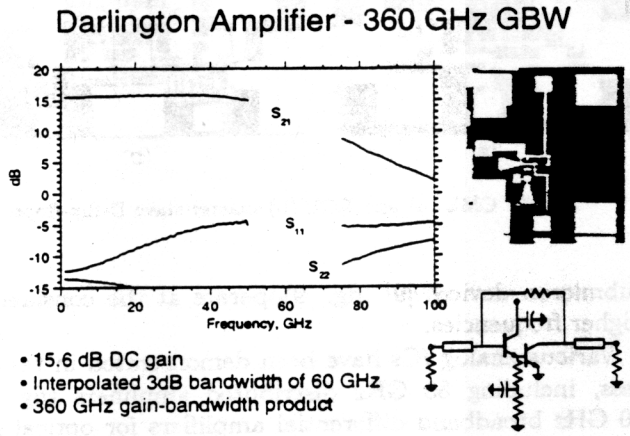

Fig. 10. Broadband Darlington feedback amplifier.

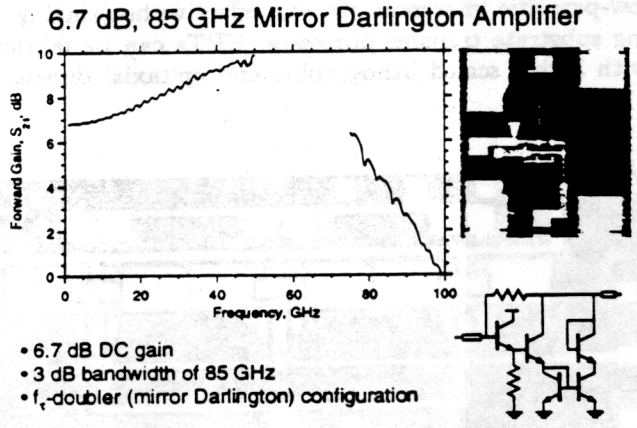

Fig. 11. Broadband feedback amplifier. The amplifier consists of a mirror f_τ doubler and emitter-follower input buffer.

giving both high f_τ and high f_{max}. With further scaling and improved circuit design, 300 GHz analog and 100 GHz digital ICs will be feasible.

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