

A > 25% PAE 0.2 - 6 GHz Lumped Power Amplifier in a 18 GHz MESFET Technology

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Abstract— We report 0.2 – 6 GHz MMIC power amplifiers with 12 dB gain, over 23 dBm output power and more than 25 % power-added-efficiency in a GaAs MESFET technology offering 18 GHz f_T and 12 V breakdown. These circuits have gain-bandwidth products of $\sim 1.3 \cdot f_T$ and are more efficient than distributed power amplifiers. These circuit topologies are being used in GaN based broad-band high power amplifiers in development.

Keywords— power amplifiers, broadband, efficient, darlington, MESFET.

I. INTRODUCTION

WIDE bandwidth power amplifiers are key components in phased-array radars and instrumentation. These amplifiers must operate over a decade bandwidth with high power-added-efficiency (PAE). Simple lumped broad-band amplifiers have gain-bandwidth products limited by the current-gain cut-off frequency, f_T . Distributed or traveling-wave amplifiers (TWAs) can provide gain-bandwidth products upto the power-gain cutoff frequency, f_{max} [1], [2]. Conventional distributed amplifiers with reverse termination have poor efficiency due to the drain-line reverse wave. Reported monolithic distributed power amplifiers (PA) typically have 10–15% PAE [3], [4]. Distributed amplifiers using tapered impedance drain-line can provide class-A limited efficiency by getting rid of the reverse termination [5], [6]. But they require high impedance lines with limited current carrying capability and are hard to realize in monolithic form for high power. Cascode-delay-matched distributed amplifiers have also been shown to be an efficient topology realizable for high powers [7]. Though these modifications improve the efficiency, distributed amplifiers in general occupy a large die area.

We present an alternative lumped broad-band power amplifier based on the f_T - doubler topology [8]. f_T - doubler small-signal amplifiers have shown gain-bandwidth products approaching twice f_T [9], [10]. As a power amplifier they can provide higher efficiency and smaller die area than conventional distributed amplifiers. We report PAs with 12 dB gain and bandwidth up to 33% of f_T , comparable to distributed power amplifiers. PAE in excess of 25% is obtained, higher than distributed amplifiers.

II. CIRCUIT DESIGN

As impedance transformation over a decade bandwidth is difficult to realize on-wafer, most wide-band amplifiers

use 50 Ω output loading. Output power is then limited to

$$P_{out} \leq \frac{(V_{br} - V_k)^2}{8Z_o} \quad (1)$$

where V_{br} is the breakdown voltage, V_k the knee voltage and $Z_o = 50 \Omega$. The device periphery (W) is chosen to provide saturation current I_{DSS} , determined by the load-line constraint,

$$I_{DSS} = \frac{(V_{br} - V_k)}{Z_o} \quad (2)$$

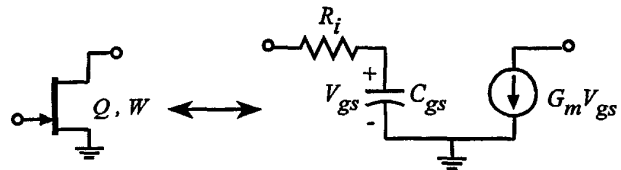


Fig. 1. Simplified A.C. FET model used for analysis

A common source amplifier, using a simplified FET model of fig. 1, has a short circuit current gain,

$$H_{21,cs} \sim \left(\frac{f_T}{jf} \right) \quad (3)$$

reaching unity at f_T . Capacitive degeneration [3] provides higher bandwidth at lower gain with constant gain-bandwidth product. To obtain sufficiently high PAE (up to 40%) gains > 10 dB are required, limiting bandwidth to $f_{3dB} < f_T/3$. With other parasitics considered, bandwidth falls significantly below $f_T/3$.

Darlington amplifiers with drains connected together (fig. 2(a)) have higher bandwidth but provide lesser efficiency. The current gain of a darlington stage is given by

$$H_{21,Darlington} \sim \frac{(1 + j2f/f_T)}{(jf/f_T)^2} \quad (4)$$

and is twice that of a single device at high frequencies, reaching unity at $2f_T$. The output power obtainable from a Darlington stage is

$$P_{out,Darlington} \leq \frac{(V_{br} - V_k - V_p)^2}{8Z_o} \equiv \frac{V_{o,p-p}}{8Z_o} \quad (5)$$

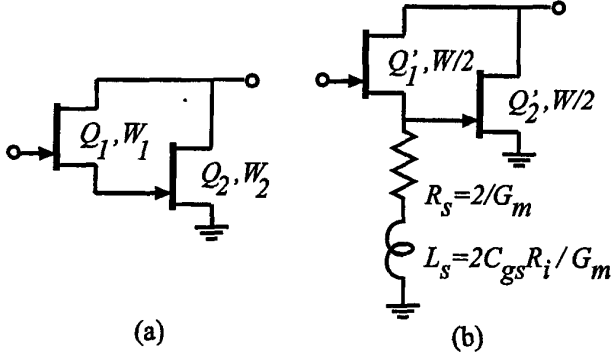


Fig. 2. A.C. schematics of (a) basic Darlington and (b) f_T -doubler configurations

a little less than the common source case (Eq. 1) because the peak - peak output voltage ($V_{o,p-p}$) is now reduced by the pinch-off voltage, V_p . Of greater importance in PAs is that the ratio of the ac currents of the two devices, is independent of device sizing and is frequency dependent, given by

$$\frac{I_{ds1}}{I_{ds2}} \sim \frac{(jf/f_T)}{(1 + jf/f_T)} \quad (6)$$

At low frequencies transistor Q_2 provides the entire ac output current. Thus we must have $I_{DSS2} = V_{o,p-p}/Z_o$ or $W_2 = W$, the same periphery as the device in the common source PA. At high frequencies (of the order of f_T) the ac output current is provided equally by Q_1 and Q_2 . Thus we must have $I_{DSS1} = V_{o,p-p}/2Z_o$ or $W_1 = W/2$. Thus in the Darlington PA the total device periphery and the net bias current are a factor of 1.5 higher than in the common source PA designed for the same ac output current. DC power consumption is a factor of 1.5 higher and PAE is impaired. Improved bandwidth is obtained at the cost of lower PAE . Potential instability in Darlington's due to their negative input resistance (Eq. 7) is well known.

$$Z_{in,Darlington} = R_{i1} + R_{i2} - \frac{G_{m1}}{\omega^2 C_{gs1} C_{gs2}} + \frac{1}{j\omega} \left(\frac{1 + G_{m1} R_{i2}}{C_{gs1}} + \frac{1}{C_{gs2}} \right) \quad (7)$$

The f_T -doubler PA (fig. 2(b)) is a modified Darlington where suitable source loading of Q'_1 splits the input voltage equally between Q'_1 and Q'_2 so that $I'_{ds1} = I'_{ds2}$ at all frequencies. Thus for the two devices to reach saturation simultaneously, we need $I_{DSS1} = I_{DSS2} = V_{o,p-p}/2Z_o$, or the two devices should have half the original periphery ($W/2$). DC power consumption is similar to the common source case and the output power is slightly reduced as in

the case of Darlington PA (Eq. 5). Also the current gain,

$$H_{21,f_T-doubler} \sim \left(\frac{2f_T}{jf} \right) \quad (8)$$

has a single pole and is unity at $2f_T$. Thus bandwidth is improved without significant loss in efficiency. Stability is also improved as the input impedance of the f_T -doubler (Eq. 9) no longer has a negative resistance.

$$Z_{in,f_T-doubler} = R_{i1} + R_{i2} + \frac{1}{j\omega} \left(\frac{1}{C_{gs1}} + \frac{1}{C_{gs2}} \right) \quad (9)$$

Further improvement in bandwidth is possible using cascode stages.

III. EXPERIMENTAL RESULTS

ICs were fabricated using the TriQuint Semiconductor, Inc., TQTRx process. Circuit simulations were done using TOM2 large signal MESFET models. Resistive feedback is used to match input and output to 50Ω without significant loss of efficiency. Broad-band π -sections using spiral inductors improve matching. High Q inductors were obtained by using two layers of metalization for the spirals.

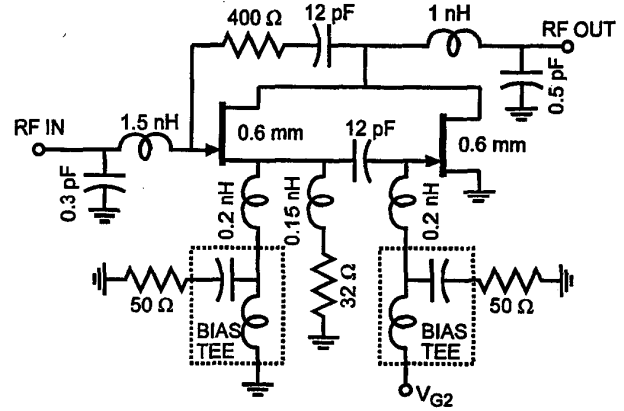


Fig. 3. Complete schematic of f_T -doubler resistive feedback PA

Fig. 3 shows the circuit diagram of the f_T -doubler PA. External bias tees were used to independently bias the two devices. The source of the first device was grounded for D.C. through a bias tee. This also helps in monitoring the currents in the two devices. The source loading was split into three parallel sections, with the bias tees A.C. ports providing part of the termination. Fig. 4 shows the measured power performance (output power, transducer power gain and PAE) at 5 GHz. The PA has a peak output power of 23 dBm with 27% PAE .

Fig. 5 shows the circuit diagram of the cascode f_T -doubler PA. A secondary RC feedback network is used to improve the cascodes' stability at high frequencies. Fig. 6 shows the measured power performance at 6 GHz. The PA has a peak output power of 23 dBm with 26% PAE .

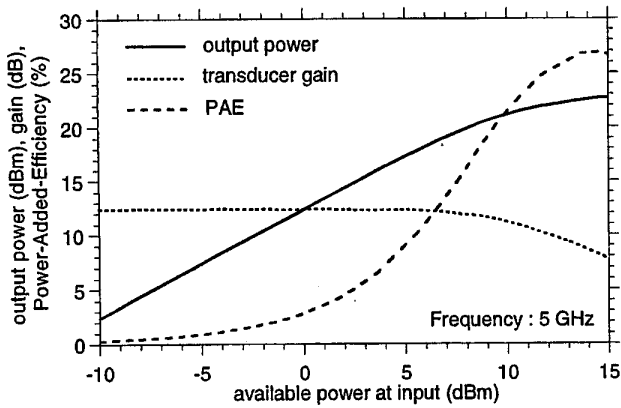


Fig. 4. Power performance of the f_T -doubler PA at 5 GHz.

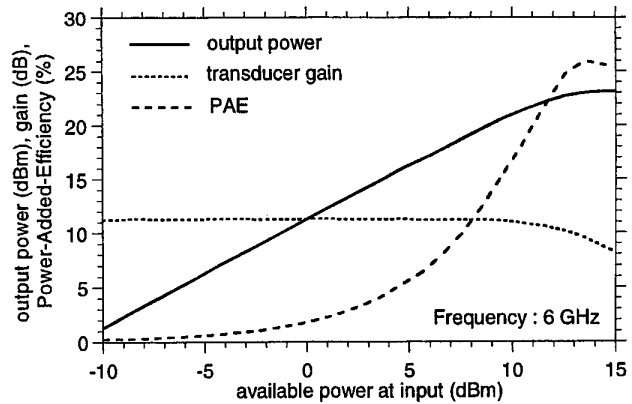


Fig. 6. Power performance of the cascode f_T -doubler PA at 6 GHz.

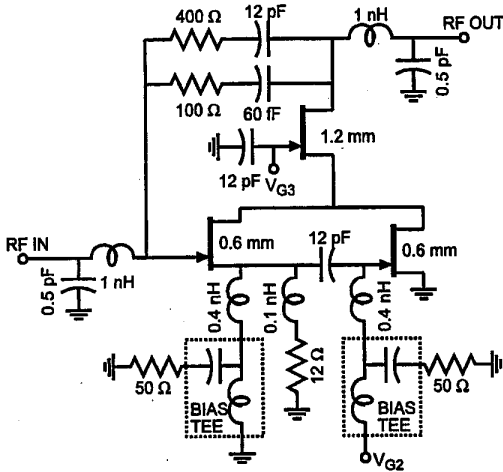


Fig. 5. Complete schematic of cascode f_T -doubler resistive feedback PA

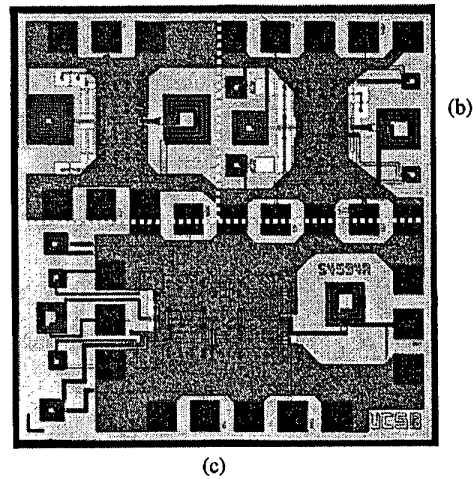


Fig. 7. Chip photograph of (a) common source, (b) f_T -doubler and (c) cascode f_T -doubler power amplifiers

Common source PAs were also fabricated for comparison. The die area (fig. 7) for the common source, f_T -doubler and cascode f_T -doubler amplifiers are $0.64 \text{ mm} \times 0.66 \text{ mm}$, $0.7 \text{ mm} \times 0.7 \text{ mm}$ and $1.36 \text{ mm} \times 0.75 \text{ mm}$ respectively. The f_T -doubler occupies similar die area as the common source PAs. The cascode f_T -doubler if fabricated using dual gate FETs would also occupy similar die area.

Fig. 8, 9, 10 compares the measured power performance of the three circuits from 0.1 - 8GHz. The common source PA provides $> 24 \text{ dBm}$ output power over 2 GHz bandwidth with $> 30\%$ PAE. The f_T -doubler PA and the cascode f_T -doubler PA provide $> 23 \text{ dBm}$ output power over 0.2 - 5 GHz and 0.2 - 6 GHz bandwidth respectively with $> 25\%$ PAE. The roll-off in the output power and PAE is attributed to the FET output capacitance of 0.27 pF/mm resulting in an output pole at $\sim 10 \text{ GHz}$. Circuits with improved output matching should provide improved PAE at the upper band-edge.

IV. CONCLUSIONS

The f_T -doubler topology is an alternative to the distributed amplifiers in realizing wide-band power amplifiers with better efficiency in a smaller die area. An experimental circuit in a GaAs MESFET technology offering 18 GHz f_T and 12 V breakdown, has achieved 0.2 - 6 GHz bandwidth, $\sim 12 \text{ dB}$ gain, $> 23 \text{ dBm}$ output power and 25% power-added-efficiency. The bandwidth is 33% of f_T and the gain-bandwidth product is $1.3 \cdot f_T$. The efficiency at higher frequencies can be improved further by using improved broadband output matching networks. These circuit topologies will be used to implement efficient broadband high power microwave amplifiers in GaN technology.

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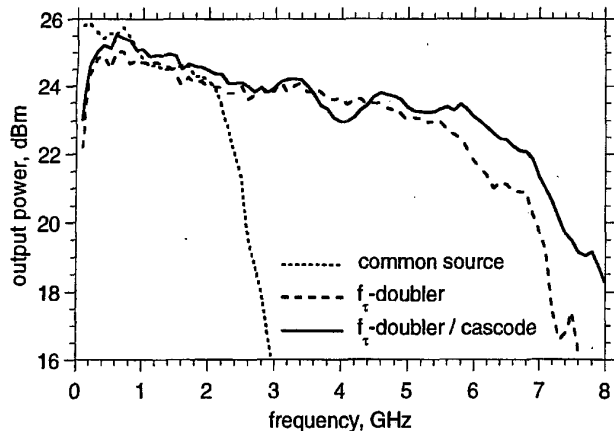


Fig. 8. Measured output power of the amplifiers as a function of frequency.

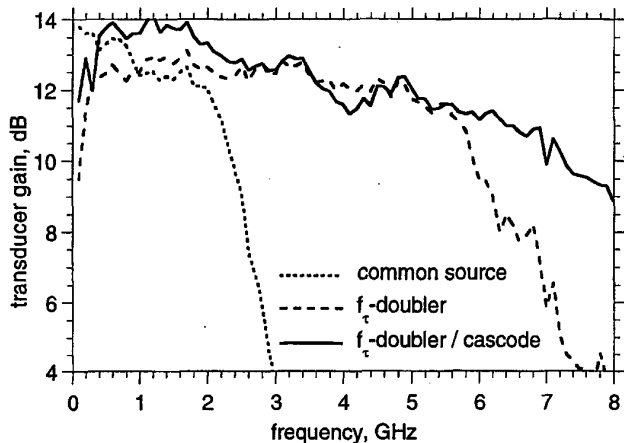


Fig. 9. Measured transducer gain of the amplifiers as a function of frequency.

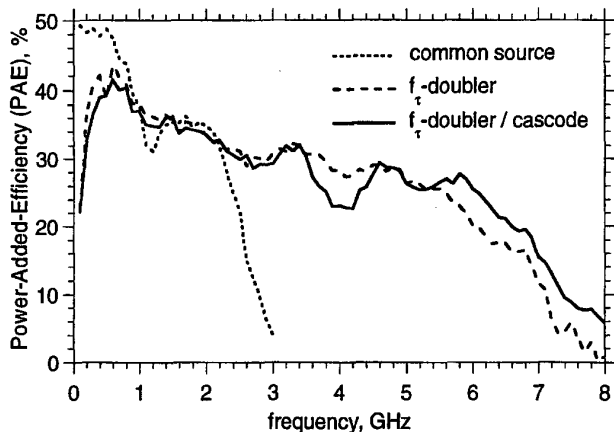


Fig. 10. Measured power-added-efficiency of the amplifiers as a function of frequency.

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