AN 18 GHz CONTINUOUS TIME $\Sigma-\Delta$ MODULATOR IMPLEMENTED IN InP TRANSFERRED SUBSTRATE HBT TECHNOLOGY

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Abstract— **We report an 18 GHz clock-rate, 2nd order continuous-time $\Sigma-\Delta$ modulator implemented using InP transferred substrate HBTs. Under two-tone test conditions, the modulator achieved 43 dB and 33 dB *SNR* at signal frequencies of 500 MHz and 990 MHz, respectively. The latter is equivalent in performance to a 1.98 GS/s Nyquist-rate ADC with 6.2 bits resolution. The IC occupied 1.95 mm^2 die area and dissipated $\sim$ 1.5W.**

I. Introduction

HIGH speed analog-to-digital converters (ADCs) find widespread applications in wideband communications and radar receivers. Efforts are being made to move the ADC forward in the signal chain, closer to the antenna. Such efforts depend critically on the ability to digitize wideband signals with very high resolution. This modified architecture should result in a more robust receiver implementation consisting of the ADC followed by DSP hardware and software.

A popular oversampling ADC architecture is based on $\Sigma-\Delta$ modulation. These achieve high *SNR* without requiring high precision in component values or device matching. Moreover, the requirements on the analog anti-aliasing filter are significantly relaxed. $\Sigma-\Delta$ modulators achieve high resolution by utilizing high sampling rates; a 2nd order ADC achieves a 15 dB improvement in *SNR* for every octave increase in sampling rate.

The *SNR* of a $\Sigma-\Delta$ modulator depends on the order of the loop filter and the oversampling ratio (*OSR*) [1]. While a high-order loop-filter results in a high *SNR*, it is difficult to design a stable modulator with order greater than two. High *SNR* can be obtained by using a 2nd order filter and as high an *OSR* as permitted by the technology of implementation. This is our approach.

InAlAs/InGaAs transferred-substrate HBTs have achieved record device bandwidths [2], [3], permitting very high speed digital circuits [4]. The continuous time architecture allows sample rates higher than the integrator unity-gain frequency. Thus, the benefits of high-bandwidth device-technology can be exploited to achieve highest modulator performance. $\Sigma-\Delta$ modulators have been reported with clock rates as high as 3.2 GHz [5] and 5 GHz [6]. Here we report a 18 GHz clock-rate, second order continuous time $\Sigma-\Delta$ ADC.

II. Device Technology and Circuit Design

The circuit was fabricated in an InGaAs/InAlAs HBT technology. While ebeam-defined devices in this technology have obtained f_{max} of 800 GHz [3], stepper-defined devices have obtained $f_\tau \sim 300$ GHz [2] and $f_{max} \geq 400$ GHz [7]. The technology provides a continuous ground plane, thus allowing a microstrip wiring environment with low wiring parasitics. All the interconnects have a controlled impedance and predictable characteristics. It also eliminates noise coupling due to ground-bounce through ground-loops. This particular IC used devices with a 4×10^{19} cm^{-3} Be-doped 300 Å base with 2 kT grade in band-gap. The collector was a Schottky contact to a 2000 Å thick lightly Si-doped layer.

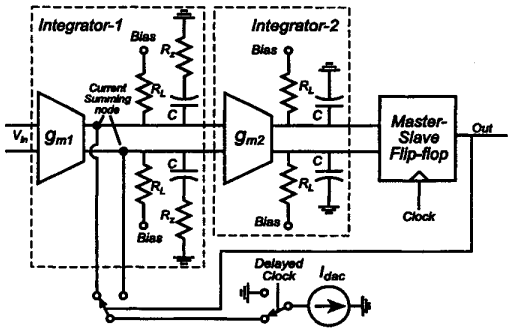

Fig. 1. A block diagram of second-order continuous time $\Sigma-\Delta$ modulator

Fig. 1 shows a simplified block diagram of the IC. The modulator consists of two transconductance (g_m) cells, each followed by a passive integrator. The quantizer is a master-slave flip-flop, while the feedback DAC is a current steering differential amplifier. The error signal is generated by current summing at the output nodes of the first transconductance cell. The entire implementation is differential for low even-order harmonic distortion, high power supply rejec-

tion ratio and reduced clock switching noise.

The preliminary design was carried out using MATLAB. The parameters for each functional element were obtained for optimum loop performance. These parameters were translated into circuit component values using a circuit simulator.

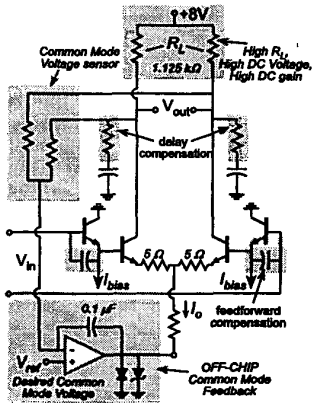

Fig. 2. A schematic of the second integrator in the loop

Fig. 2 shows the circuit schematic for the second integrator in the loop. Since noise shaping near DC is limited by the finite DC gain of the integrators [1], high gains are desired. Integrator excess phase delay limits the high frequency noise-shaping and hence limits the maximum *OSR*. Low excess phase delay and hence extremely wide integrator bandwidth are desired in addition to high DC gain for high *OSR* $\Sigma - \Delta$ ADCs.

In the absence of pnp transistors in an HBT technology, achieving a high dc gain is challenging. Usually, designers overcome this limitation by employing bootstrapped [5] or negative-resistance loads. These techniques introduce higher order poles, resulting in excess phase delay and thus limiting the *OSR*. They also increase the transistor count in the high frequency signal path, which is undesirable in very wideband circuits. Here, high DC gain is obtained simply by using a large pull-up resistive load. This necessitates a large positive power supply voltage and an (off-wafer) common-mode-feedback (CMFB) loop that controls the integrator DC bias. This is important given the small breakdown voltage of the InGaAs collector HBTs.

The integrator is a g_m stage whose output is loaded by a grounded capacitor (Figs. 1 and 2). Active integrators (using a cascaded pair of g_m stages whose second stage has a Miller-connected integrating capacitor), used commonly in $\Sigma - \Delta$ modulator designs, ob-

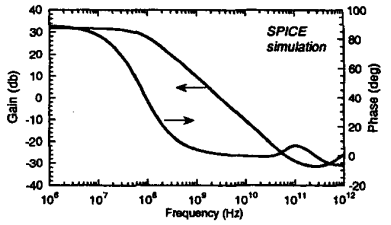

Fig. 3. Plot of frequency response of the second integrator

tain a very high DC gain ($g_m^2 R_L^2$ vs. $g_m R_L$) but have a lower feasible bandwidth due to the loop-bandwidth and loop-stability considerations associated with the Miller feedback loop. In contrast, the integrator reported here uses a simple g_m stage loaded by a capacitor, achieving a high bandwidth.

Excess delay due to higher order integrator poles associated with transistor parasitics is partly offset by a zero in the transfer function introduced by placing a resistor in series with the capacitor. Emitter followers (Figs. 2) buffer the integrator inputs, increasing the input impedance and the DC gain. Because the output impedance of the emitter follower is higher than that of the drive point ($1/j\omega C_{int}$) at high frequencies, the emitter followers are removed from the signal path at high frequencies by feed-forward compensation. The common-mode voltage at the output for CMFB, is sensed with high value on-chip resistors. SPICE simulations (Fig.3) of the integrator shows a ($1/j\omega C_{int}$) behavior from 40 MHz to $\sim$ 100 GHz.

The goal of this design is to use the maximum possible clock frequency. The main limits to the clock frequency are from the excess delay accumulated in the signal path and the metastability and dynamic hysteresis errors in the quantizer. The excess delay in the signal path includes the delay due to integrator higher order poles, the delay in the interconnects and the delay in the quantizer decision and the feedback DAC.

A fully differential DAC eliminates feedback errors associated with unequal DAC rise and fall times [5]. However, the DAC is still vulnerable to quantizer metastability errors. Such errors result in the output edge of the quantizer being modulated by the input amplitude. For small quantizer inputs, the quantizer output can take several circuit time-constants to reach the correct logic level. For strong inputs, this delay is reduced. For a quantizer output corresponding to logic 1, the DAC charge delivered to the integrating capacitor varies with the strength of quantizer input (shown qualitatively in Fig. 4).

One method to reduce such errors is to add an-

other latch stage for further regeneration [5]. A second method, used here, is a delayed return-to-zero (RTZ) DAC. The RTZ DAC is gated with a clock pulse delayed such that the DAC is active only in the final 50% of the clock period (Fig. 4). This approach requires less additional transistors (~ 6) than an extra latch (~ 40).

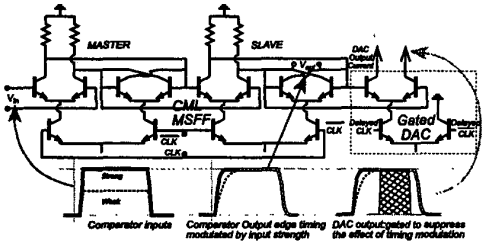

Fig. 4. A qualitative description of metastability in the flip-flop, with RTZ DAC as the proposed solution. While CML flip-flop is shown for simplicity, the circuit uses an ECL flip-flop.

The use of either an RTZ DAC or an extra latching stage results in an extra half-clock cycle delay in the feedback path, adding to other excess loop delays, and thus limiting the clock rate. Using MATLAB, we observed a 10 dB reduction in *SNR* with the addition of a half-sample delay (25 ps delay for a 20 GHz clock) in the loop. As with other excess loop delays, this is compensated to first order in frequency by introduction of a zero in the transfer function, through addition of a resistor in series with the integration capacitor.

The first g_m stage is outside the $\Sigma-\Delta$ loop, hence its nonlinearity directly degrades the ADC linearity. Jensen [5] reported a linearized g_m stage using Caprio's cell. Our earlier designs used Caprio's cell; the $\Sigma-\Delta$ modulator reported here eliminated this in favor of a differential pair with its smaller transistor count (yield limits in a university process). An ECL master-slave flip-flop (demonstrated to operate as a divide-by-two at 66 GHz [4]) was used as the quantizer. The final design parameters were: $g_{m1} = 15$ mS, $g_{m2} = 65$ mS, average DAC feed back current $I_{dac} = 2$ mA, nominal pull-up resistors $R_L = 1.125$ kΩ, clock frequency $f_c = 20$ GHz and integrating capacitors $C = 3$ pF. In fabrication, the nichrome resistors were about 20% lower than design values.

III. Measurement and Results

The HBTs on the fabricated IC wafer had a typical dc current-gain, $\beta \geq 100$, current gain cut-off frequency, $f_\tau \approx 190$ GHz, and power gain cut-off frequency, $f_{max} \approx 200$ GHz at an emitter current density of $\sim 10^5$ A/cm^2. The common-emitter breakdown voltage, BV_{CEO}, was ~ 1.4 V.

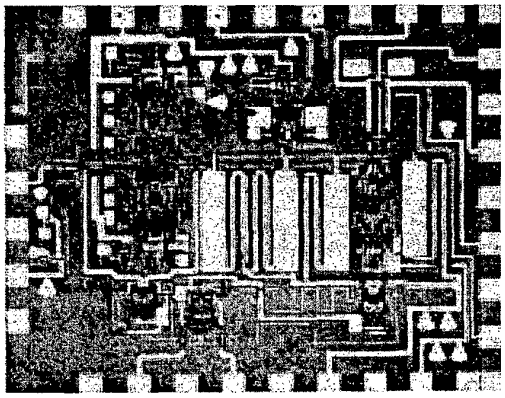

Fig. 5. Die photograph of the completed $\Sigma-\Delta$ modulator

The IC was tested by on-wafer probing using 40GHz probe cards. The photograph of the die is shown in Fig.5. The standard technique for testing $\Sigma-\Delta$ modulators uses a fast logic analyzer to acquire the digital data stream. The captured data is analyzed by FFT for its spectral content. Due to the lack of a logic analyzer with sufficient bandwidth for capturing 18 GHz data, we were forced to use an analog spectrum analyzer to view the spectrum of the digital output. The measurement setup is shown in the Fig.6. The spectrum analyzer noise-figure was improved by adding an input low-noise high-gain preamplifier and switched attenuators. The $\Sigma-\Delta$ modulator was tested with a 18 GHz clock and two-tone measurements were performed at signal frequencies of 150 MHz, 500 MHz and 900 MHz.

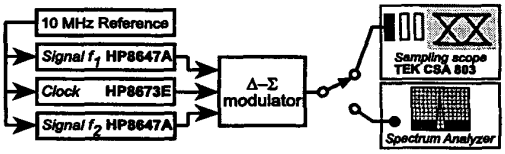

Fig. 6. The setup used for testing the $\Sigma-\Delta$ modulator

The results for variation of the output power in the fundamental and the third-order distortion component are shown in Fig. 7. The noise-floor shows little variation from 150 MHz to 1 GHz. This suggests that the modulator does not shape the quantization-noise below 1 GHz. While this is in contrast with our MATLAB simulations, it is consistent with full-loop transistor level simulations on SPICE we have recently performed. We believe this is due to metastability and dynamic hysteresis errors in the quantizer. Fig. 8 shows the spectrum of the output for a two-tone input at 150 MHz.

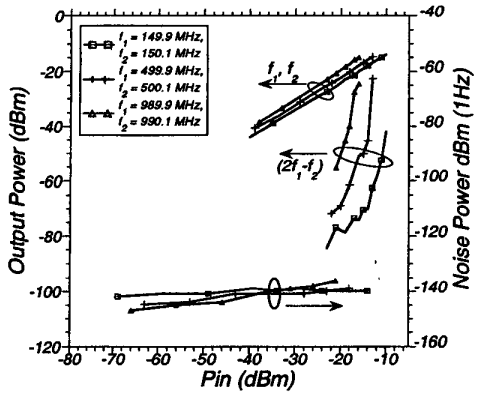

Fig. 7. Noise floor and third-order distortion power as a function of input power for different signal frequencies

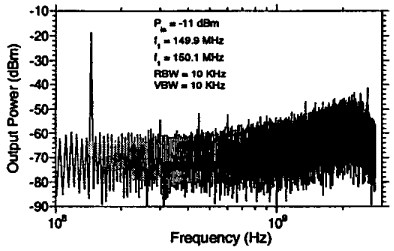

Fig. 8. Spectrum of the $\Sigma-\Delta$ modulator output for a two-tone input at 150 MHz

The *SNR* quoted here is calculated from the power in one tone relative to the noise-floor. In single tone testing, for a Nyquist-rate ADC, the number of bits of resolution (N) and the *SNR* are related by [8]

$$SNR(dB) = 6.02N + 1.76 \quad (1)$$

$$N = [SNR(dB) - 1.76]/6.02 \quad (2)$$

For single-tone testing, a Nyquist ADC with maximum input $\pm v_{max}$ can have a maximum single-tone input amplitude of $v_{in} = v_{max}cos(\omega_1 t)$, while for two-tone testing, the maximum input is $v_{in} = (v_{max}/2)cos(\omega_1 t) + (v_{max}/2)cos(\omega_2 t)$. Thus, the maximum signal power at ω_1 in two-tone testing is 6dB below that in single-tone testing. Under two-tone testing, a Nyquist-rate ADC has

$$\begin{aligned} SNR(dB) &= 6.02N + 1.76 - 6 \\ &= 6.02N - 4.24 \quad (3) \\ N &= [SNR(dB) + 4.24]/6.02 \quad (4) \end{aligned}$$

Thus, the 33 dB SNR (990 MHz signal) for the $\Sigma - \Delta$ ADC is equivalent in performance to a 1.98 GS/s Nyquist-rate ADC with 6.2 effective number of bits (ENOB) resolution (Eq. 4). The measured *SNR* with ENOB resolution is presented in Table I.

TABLE I

SNR AND THE ENOB OF AN EQUIVALENT NYQUIST-RATE ADC AT DIFFERENT SIGNAL FREQUENCIES

frequency	Measured *SNR*	ENOB resolution
150 MHz	48 dB	8.7
500 MHz	42 dB	7.7
990 MHz	33 dB	6.2

IV. CONCLUSIONS

We have demonstrated a second order continuous time $\Sigma - \Delta$ modulator fabricated in a 200 GHz f_τ, f_{max} InAlAs/InGaAs HBT process. The chip is clocked at 18 GHz with signal bandwidths ranging from 150 MHz to 990 MHz. All measurements were two-tone measurements. The modulator achieved an *SNR* of 48 dB (8.7 bits), 42 dB (7.7 bits) and 33 dB (6.2 bits) at input signals of 150 MHz, 500 MHz and 990 MHz, respectively. The poor noise-shaping below 1 GHz is being investigated.

ACKNOWLEDGMENTS

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