Broadband GaAs MESFET and GaN HEMT Resistive Feedback Power Amplifiers

Karthikeyan Krishnamurthy, Ramakrishna Vetury, Stacia Keller, Umesh Mishra, Mark J. W. Rodwell, and Stephen I. Long

***Abstract*—We report 0.2 to 6-GHz MMIC power amplifiers with 12-dB gain, over 23-dBm output power, and more than 25% power-added efficiency (PAE) in a GaAs MESFET technology offering 18-GHz f_τ and 12-V breakdown. These circuits have gain-bandwidth products of $\sim 1.3 \cdot f_\tau$ and are more efficient than distributed power amplifiers. A first demonstration of similar circuits in GaN/AlGaN HEMT technology yielded 11-dB gain, 0.2 to 7.5-GHz bandwidth amplifiers with over 31.5-dBm output power and up to 15% PAE. With improved devices and models we expect significantly higher power from the GaN HEMT circuits.**

***Index Terms*—Broadband amplifiers, FET circuits, power amplifiers.**

I. INTRODUCTION

WIDE-BANDWIDTH power amplifiers are key components in phased-array radars and instrumentation. These amplifiers must operate over a decade bandwidth with high output power and power-added efficiency (PAE). Simple lumped broadband amplifiers have gain-bandwidth products limited by the current-gain cut-off frequency f_τ. Distributed or traveling-wave amplifiers (TWAs) can provide gain-bandwidth products up to the power-gain cutoff frequency, $f_{\max}$ [1], [2]. Conventional distributed amplifiers with reverse termination have poor efficiency due to the drain-line reverse wave. Reported monolithic distributed power amplifiers typically have 10% to 15% PAE [3], [4]. Distributed amplifiers using tapered impedance drain-lines can in theory provide efficiencies up to the class-A limit of 50%, by eliminating the reverse termination [5], [6]. Tapered drain-line TWAs require high impedance transmission lines with limited current carrying capability, and thus are hard to realize for high output powers in monolithic form. Cascode-delay-matched distributed amplifiers have also been shown to be an efficient topology realizable for high output powers [7]. Though these modifications improve the efficiency, distributed amplifiers in general occupy a large die area.

We had presented [8] an alternative lumped broadband power amplifier based on the f_τ-doubler topology [9]. The f_τ-doubler small-signal amplifiers have shown gain-bandwidth products approaching twice the transistor f_τ [10], [11]. As a power amplifier f_τ-doubler circuits can provide higher efficiency and smaller die area than conventional distributed amplifiers. In this paper we report GaAs MESFET power amplifiers with 12-dB gain and bandwidths as high as 33% of f_τ, comparable to distributed power amplifiers. PAE in excess of 25% is obtained, higher than reported for distributed amplifiers. AlGaN/GaN HEMTs have high $f_\tau V_{\rm br}$ products [12], and are good candidates for high-power broadband amplifiers. First results on f_τ-doubler power amplifiers using single and dual-gate GaN HEMTs are also presented [13].

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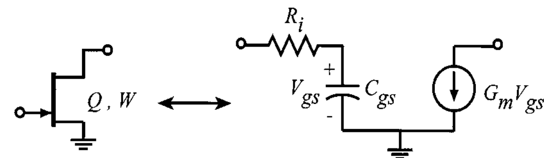

Fig. 1. Simplified ac FET model used for analysis.

II. CIRCUIT DESIGN

As impedance transformation over a decade bandwidth is difficult to realize on-wafer, most wideband amplifiers use 50-Ω output loading. Transistor output power is then limited to

$$P_{\rm out} \le \frac{(V_{\rm br} - V_k)^2}{8Z_o} \tag{1}$$

where $V_{\rm br}$ is the breakdown voltage, V_k the knee voltage and $Z_o = 50\ \Omega$. The device periphery W is chosen to provide saturation current $I_{\rm DSS}$, determined by the load-line constraint

$$I_{\rm DSS} = \frac{(V_{\rm br} - V_k)}{Z_o}. \tag{2}$$

A common-source amplifier, using a simplified FET model of Fig. 1, has a short circuit current gain

$$H_{21,\rm cs} = \left(\frac{f_\tau}{jf}\right) \tag{3}$$

reaching unity at f_τ (Fig. 2). Capacitive degeneration [3] provides higher bandwidth at lower gain with constant gain-bandwidth product. To obtain sufficiently high PAE (up to 40%), gains >10 dB are required, limiting bandwidth to $f_{3\ dB} < f_\tau/3$. With other parasitics considered, bandwidth falls significantly below $f_\tau/3$.

Darlington amplifiers have higher bandwidth than common-source amplifiers but provide lesser efficiency.

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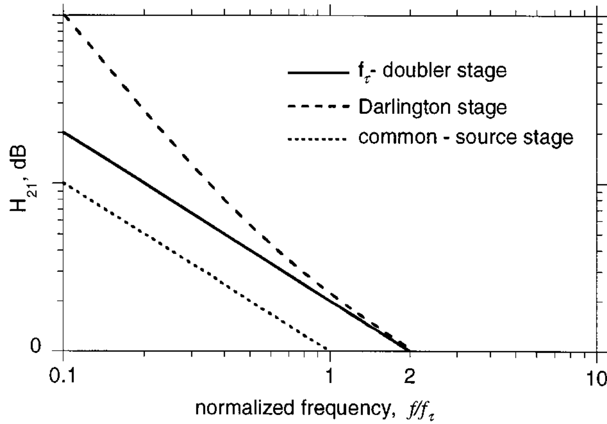

Fig. 2. Short circuit current gain H_{21} for common-source, Darlington, and f_τ-doubler configurations.

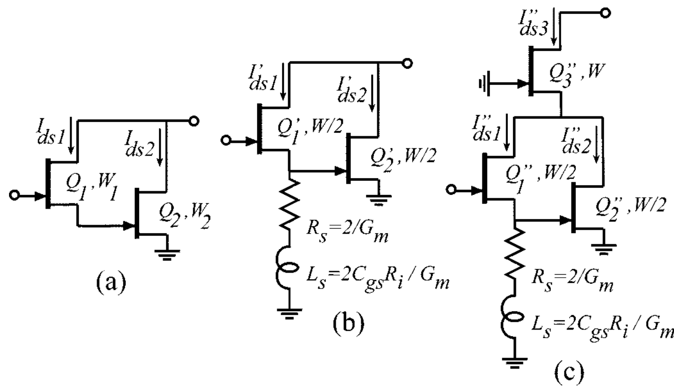

Fig. 3. AC schematics. (a) Basic Darlington. (b) f_τ-doubler configuration. (c) Cascode f_τ-doubler configuration.

If the drain of the common-drain device is connected to the amplifier output [Fig. 3(a)], then the current gain

$$H_{21,\text{Darlington}} = \frac{(1+j2f/f_\tau)}{(jf/f_\tau)^2} \tag{4}$$

is twice that of a common-source stage at high frequencies (Fig. 2), reaching unity at $2f_\tau$. The peak output power obtainable from a Darlington stage is

$$P_{\text{out,Darlington}} \le \frac{(V_{\text{br}} - V_k - V_p)^2}{8Z_o} \equiv \frac{V_o{}^2,\text{p}-\text{p}}{8Z_o} \tag{5}$$

which is slightly less than the common-source case [see (1)] because the peak–peak output voltage $V_{o,\text{p}-\text{p}}$ is now reduced by the pinch-off voltage V_p. Of greater importance for efficiency is the ratio of the ac currents of the two devices. This ratio is independent of device sizing and is frequency-dependent, given by

$$\frac{I_{\text{ds1}}}{I_{\text{ds2}}} = \frac{(jf/f_\tau)}{(1+jf/f_\tau)}. \tag{6}$$

At low frequencies, transistor Q_2 provides the entire ac output current. Thus, a Darlington amplifier designed for the same power level as the common-source power amplifier must have $I_{\text{DSS2}} = V_{o,\text{p}-\text{p}}/Z_o$ or $W_2 = W$, the same periphery as the device in the common-source case. At high frequencies (of the order of f_τ) the ac output current is provided equally by Q_1 and Q_2. Thus, we must have $I_{\text{DSS1}} = V_{o,\text{p}-\text{p}}/2Z_o$ or $W_1 = W/2$. Therefore, in the Darlington power amplifier, the total device periphery and the net bias current are a factor of 1.5 higher than in a common-source power amplifier designed for the same ac output current. DC power consumption is a factor of 1.5 higher and the PAE is impaired. Improved bandwidth is obtained at the cost of lower PAE. Potential instability due to negative input resistance

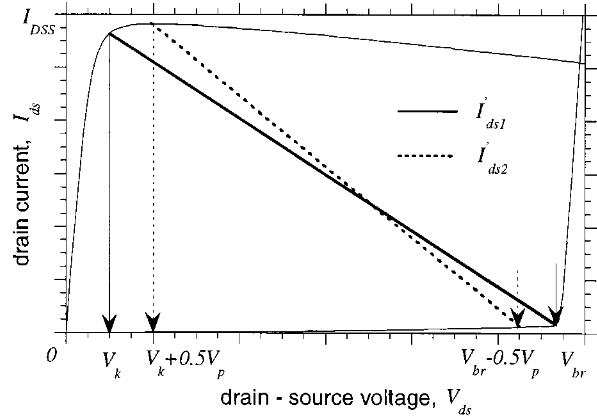

Fig. 4. Load-lines seen by the two devices in a f_τ-doubler power amplifier, superimposed on the device $I_{\text{ds}} - V_{\text{ds}}$ plot.

$$Z_{\text{in,Darlington}} = R_{i1} + R_{i2} - \frac{G_{m1}}{\omega^2 C_{\text{gs1}} C_{\text{gs2}}} + \frac{1}{j\omega}\left(\frac{1+G_{m1}R_{i2}}{C_{\text{gs1}}} + \frac{1}{C_{\text{gs2}}}\right) \tag{7}$$

is a further limitation of Darlingtons.

The f_τ-doubler power amplifier [Fig. 3(b)] is a modified Darlington stage where suitable source loading of Q_1' splits the input voltage equally between Q_1' and Q_2', so that $I_{\text{ds1}}' = I_{\text{ds2}}'$ at all frequencies. The source loading consists of a resistor $R_s = 2/G_m$ in series with an inductor $L_s = 2C_{\text{gs}}R_i/G_m$. Published f_τ-doubler amplifiers [10], [11] have not incorporated this inductor. L_s is required to obtain equal input voltage division between Q_1' and Q_2' for frequencies $f \sim 1/2\pi R_i C_{\text{gs}}$; the L_s/R_s time constant being equal to the $R_i C_{\text{gs}}$ time constant.

With this source loading, Q_1' and Q_2' carry equal ac drain current for all frequencies. Thus, for the two devices to reach saturation simultaneously, we require that $I_{\text{DSS1}}' = I_{\text{DSS2}}' = V_{o,\text{p}-\text{p}}/2Z_o$. Hence the two devices should have half the periphery of a common-source stage of equal output power (i.e., $W/2$). The two devices Q_1' and Q_2' have marginally different load-lines given by $(2Z_o + 2/G_m)$ and $2Z_o$, respectively. This is due to the extra source loading seen by Q_1', which limits the peak–peak V_{ds} of Q_1' and Q_2' to $(V_{\text{br}} - V_k)$ and $(V_{\text{br}} - V_k - V_p)$, respectively (Fig. 4). This does not significantly affect the output power, provided that $Z_o \gg 1/G_m$ or $(V_{\text{br}} - V_k) \gg V_p$. As in the case of the Darlington amplifier, the peak output power

$$P_{\text{out},f_\tau-\text{doubler}} \le \frac{(V_{\text{br}} - V_k - V_p)(V_{\text{br}} - V_k - V_p/2)}{8Z_o} \tag{8}$$

is slightly smaller than the common-source power amplifier. DC power consumption is similar to the common-source case provided that dc power dissipation in the source resistance is elim-

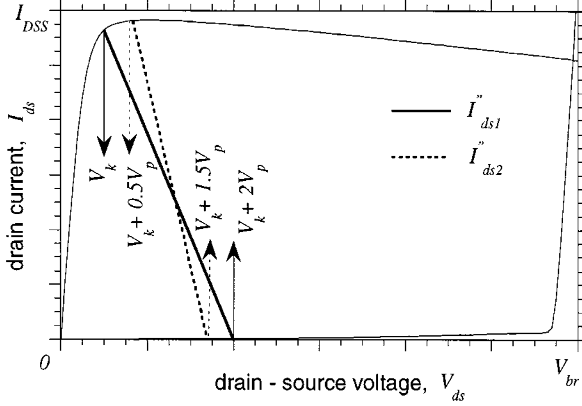

Fig. 5. Load-lines seen by the two devices, Q_1'' and Q_2'' in a cascode f_τ-doubler power amplifier, superimposed on the device $I_{\rm ds} - V_{\rm ds}$ plot.

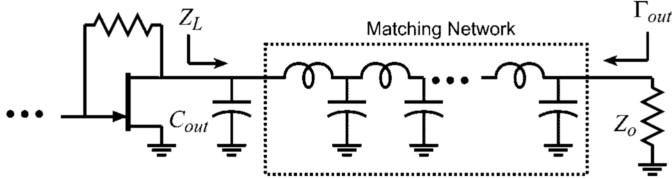

Fig. 6. π-section output matching networks for broadband power amplifiers.

inated by grounding the source of Q_1' for dc using a RF choke. The current gain of the f_τ-doubler stage

$$H_{21,f_\tau-\text{doubler}} = \left(\frac{2f_\tau}{jf}\right) \tag{9}$$

has a single pole and is unity at $2f_\tau$ (Fig. 2). Thus bandwidth is improved without significant loss in efficiency. Stability is also improved as the input impedance of the f_τ-doubler

$$Z_{\text{in},f_\tau-\text{doubler}} = R_{i1} + R_{i2} + \frac{1}{j\omega}\left(\frac{1}{C_{\rm gs1}} + \frac{1}{C_{\rm gs2}}\right) \tag{10}$$

no longer has a negative resistance.

Because the f_τ-doubler topology alleviates the bandwidth limitation due to $C_{\rm gs}$, the parasitic $C_{\rm gd}$ and $C_{\rm ds}$ may then become significant. Addition of a common-gate stage to form a cascode f_τ-doubler [Fig. 3(c)] reduces the effect of $C_{\rm gd}$ substantially. In this case, since the f_τ-doubler is driving a low input impedance common-gate stage, the two devices Q_1'' and Q_2'' drive widely different loads of $4/G_m$ and $2/G_m$, respectively (Fig. 5). However the power dissipated in Q_1'' and Q_2'' is a small fraction of the net output power as in the case of a cascode (common-source - common-gate) amplifier.

For all the configurations considered above, the capacitances $C_{\rm gd}$ and $C_{\rm ds}$ load the amplifier output. Broadband π-sections (Fig. 6) could be used to partially absorb the net output capacitance ($C_{\rm out}$) and improve matching. In small signal amplifiers, these networks are designed to minimize the magnitude of the output reflection coefficient ($\Gamma_{\rm out}$), over the bandwidth.

In power amplifiers there is an additional constraint on the matching network, to improve output power and PAE at the upper band edge. In the absence of the matching network, the load-line deviates from Z_o with increasing frequency (Fig. 7) due to $C_{\rm out}$. With the matching network (Fig. 6), the peak output

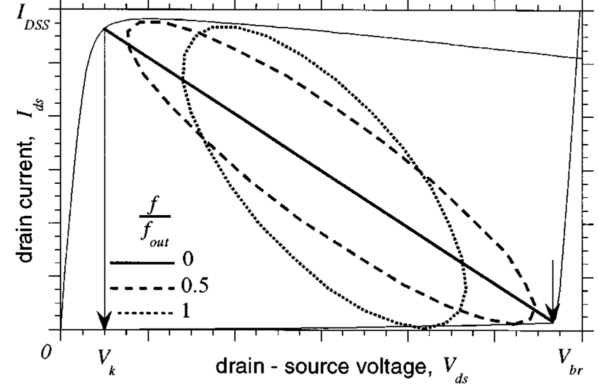

Fig. 7. Variation of load-line with frequency due to the presence of $C_{\rm out}$ ($f_{\rm out} = I_{\rm DSS}/2\pi C_{\rm out} V_{\rm br}$).

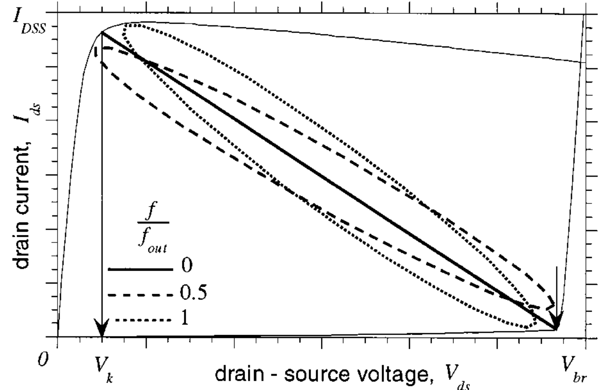

Fig. 8. Variation of load-line with frequency in the presence of a four-section matching network at the output.

power as a function of frequency is dependent on $\text{Re}(Z_L)$ or $\text{Re}(Y_L)$ as decided by the magnitude of Z_L [14]. For the case of $|Z_L| < Z_o$, the load-line is limited by the maximum allowed current swing ($I_{\rm DSS}$). The peak output power $P_{\rm out}(f)$ is now less than the optimum case [$P_{\rm out}$ in (1)] and given by

$$\frac{P_{\rm out}(f)}{P_{\rm out}} = \frac{\text{Re}(Z_L)}{Z_o}. \tag{11}$$

For the case of $|Z_L| > Z_o$, the load-line is limited by the maximum allowed voltage swing ($V_{\rm br}$) and the peak output power is now

$$\frac{P_{\rm out}(f)}{P_{\rm out}} = \text{Re}(Y_L) Z_o. \tag{12}$$

So to obtain the maximum output power, the matching networks have to be designed to minimize $\text{Im}(Z_L)$ and $\text{Im}(Y_L)$ over the bandwidth. Fig. 8 shows the load-line variation in the presence of a four-section matching network. These networks will improve PAE over a bandwidth of at most $\Delta f_{\rm out} = I_{\rm DSS}/2\pi C_{\rm out} V_{\rm br}$, the output pole frequency.

III. Experimental Results

A. GaAs MESFET Power Amplifiers

The ICs were fabricated using the TriQuint Semiconductor, Inc., TQTRx process. The circuits were simulated using TOM2 large signal MESFET models. Fig. 9 shows the circuit diagram

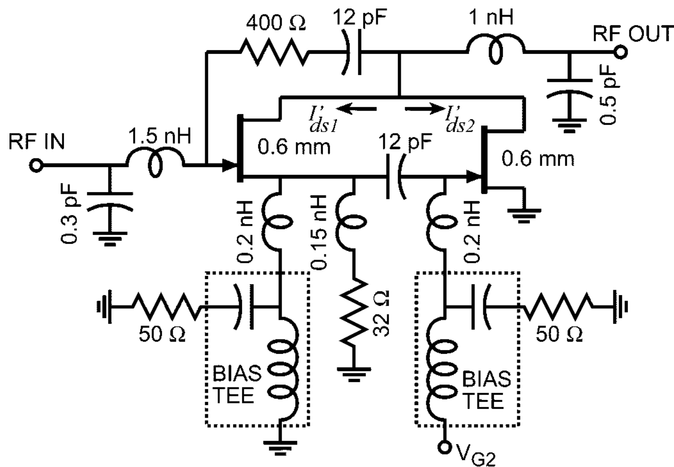

Fig. 9. Complete schematic of the GaAs MESFET f_T-doubler resistive feedback power amplifier.

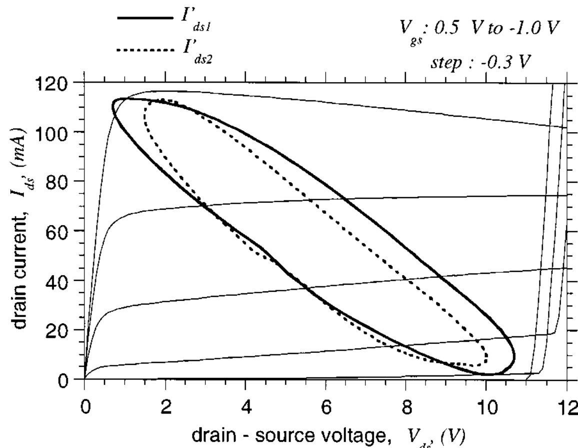

Fig. 10. Simulated load-lines of the devices in the GaAs MESFET f_T-doubler resistive feedback power amplifier (frequency = 3 GHz), superimposed on the simulated device $I_{ds} - V_{ds}$ plot.

of the f_T-doubler power amplifier. Resistive feedback matches input and output impedances to 50 Ω without significant loss of efficiency. Broadband π-sections at the input and output were designed to improve matching. High Q spiral inductors were obtained by using two layers of metallization. External bias tees were used to independently bias the two devices. The source of the first device was grounded for dc through a bias tee. This also facilitates monitoring the device bias currents. The source loading was split into three parallel sections, with the bias tee's 50-Ω ac ports providing part of the RF termination. This helps in monitoring the RF current split between the two devices. For maximum efficiency operation, bias is adjusted to fill the load-line of each device. The simulated load-line for the two devices (Fig. 10) at 3 GHz shows a nearly equal current division. The capacitive current seen in the load-line is due to the device parasitic capacitance at the drain. Measured power performance (output power, transducer power gain, and PAE) at 5 GHz (Fig. 11) shows a peak output power of 23 dBm with 27% PAE.

Fig. 12 shows the circuit diagram of the cascode f_T-doubler power amplifier. A secondary RC feedback network, effective at high frequency, provides unconditional stability. Fig. 13

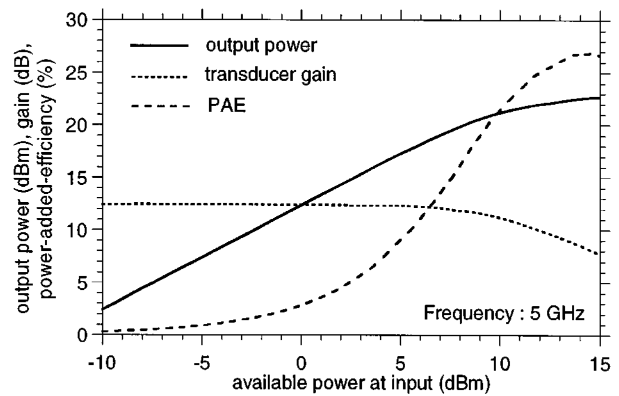

Fig. 11. Power performance of the GaAs MESFET f_T-doubler power amplifier at 5 GHz.

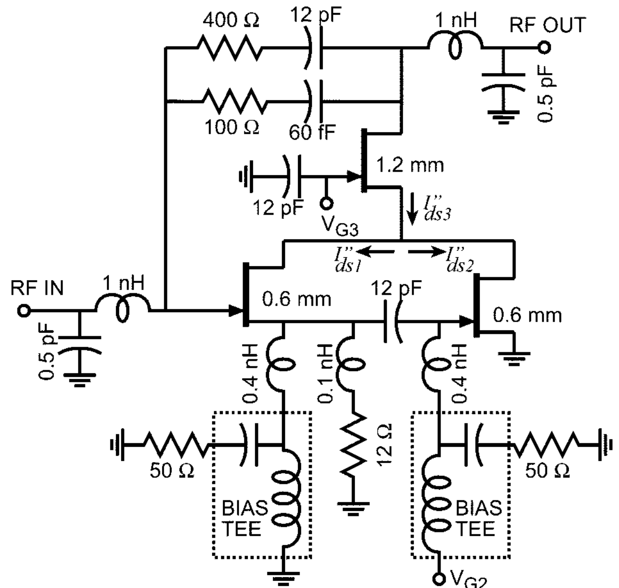

Fig. 12. Complete schematic of the GaAs MESFET cascode f_T-doubler resistive feedback power amplifier.

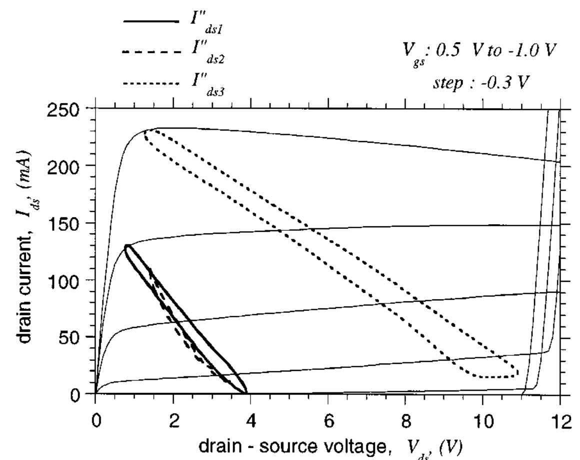

Fig. 13. Simulated load-lines of the devices in the GaAs MESFET cascode f_T-doubler resistive feedback power amplifier (frequency = 3 GHz), superimposed on the simulated device $I_{ds} - V_{ds}$ plot.

shows the simulated load-line for the three devices at 3 GHz. Measured power performance at 6 GHz (Fig. 14) shows a peak output power of 23 dBm with 26% PAE.

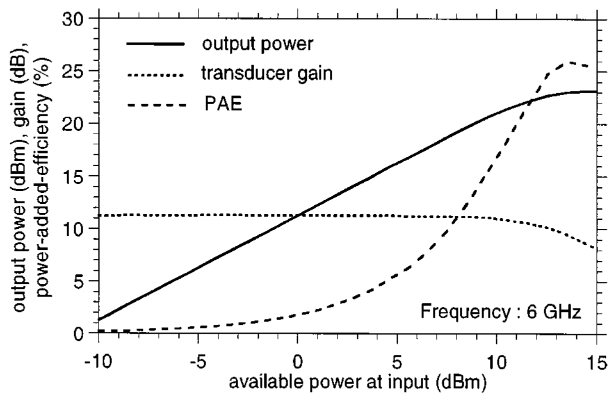

Fig. 14. Power performance of the GaAs MESFET cascode f_τ-doubler power amplifier at 6 GHz.

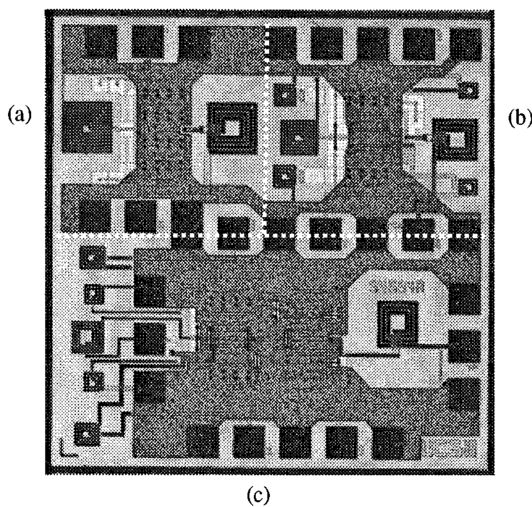

Fig. 15. Chip photograph of the GaAs MESFET. (a) Common-source. (b) f_τ-doubler. (c) Cascode f_τ-doubler power amplifier.

Common-source power amplifiers were also fabricated for comparison. The die areas (Fig. 15) for the common-source, f_τ-doubler, and cascode f_τ-doubler amplifiers are 0.64 mm $\times$ 0.66 mm, 0.7 mm $\times$ 0.7 mm, and 1.36 mm $\times$ 0.75 mm, respectively. The f_τ-doubler occupies similar die area as the common-source power amplifiers. f_τ-doubler power amplifiers using dual-gate FETs should provide similar performance as cascode f_τ-doubler power amplifiers without the excess die area.

Figs. 16–18 compare the power performance of the three circuits measured over 0.1 to 8 GHz. The common-source power amplifier provides >24-dBm output power over 2-GHz bandwidth with >30% PAE. The f_τ-doubler power amplifier and the cascode f_τ-doubler power amplifier provide >23-dBm output power over 0.2 to 5-GHz and 0.2 to 6-GHz bandwidth, respectively, with >25% PAE. The roll-off in the output power and PAE is attributed to the FET output capacitance of 0.27 pF/mm resulting in an output pole at ~10 GHz. Circuits with multi-section LC networks at the output, as discussed in the previous section, should provide improved PAE at the upper band-edge.

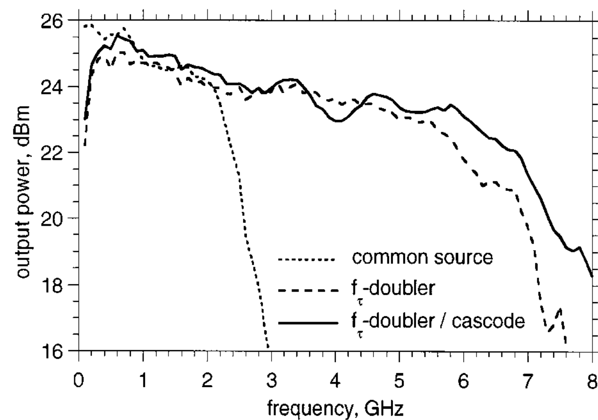

Fig. 16. Measured output power of the GaAs MESFET amplifiers as a function of frequency.

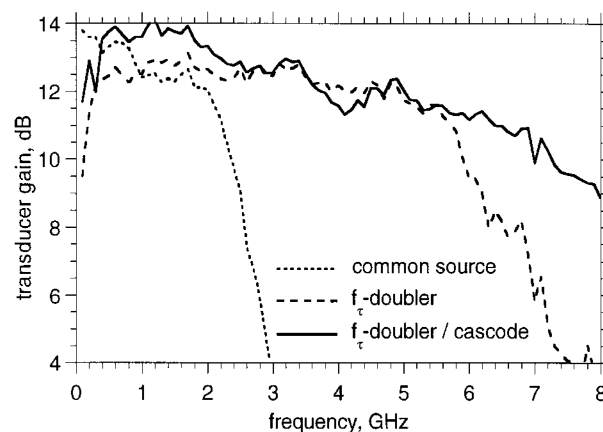

Fig. 17. Measured transducer gain of the GaAs MESFET amplifiers as a function of frequency.

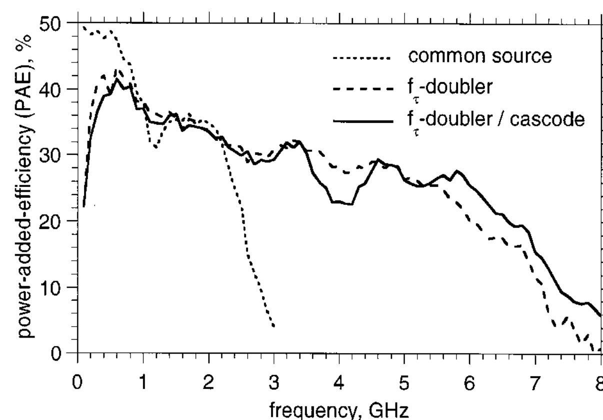

Fig. 18. Measured PAE of the GaAs MESFET amplifiers as a function of frequency.

B. GaN HEMT Power Amplifiers

GaN HEMTs with 0.7-μm gate-length were fabricated on epitaxial material grown by MOCVD on C-plane sapphire. The layer structure and process details are discussed in [15]. A total device periphery of $W = 2.4$ mm was used to drive up to 1-A current into a 50-Ω load, with the device breakdown exceeding 50 V. Simulations predicted 10-dB gain and 0.2 to 10-GHz bandwidth. The devices were flip-chip bonded

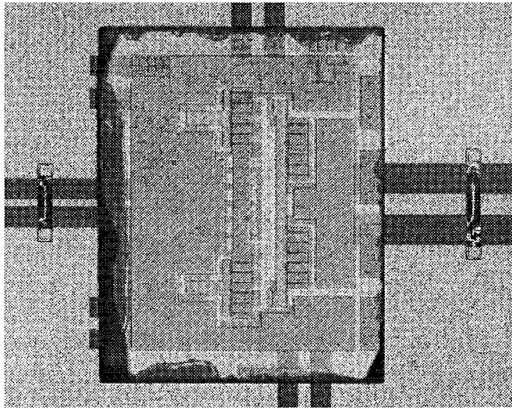

Fig. 19. Photograph of the GaN HEMT f_T-doubler resistive feedback power amplifier (GaN HEMT on transparent sapphire substrate, flip-chip bonded on AlN substrate).

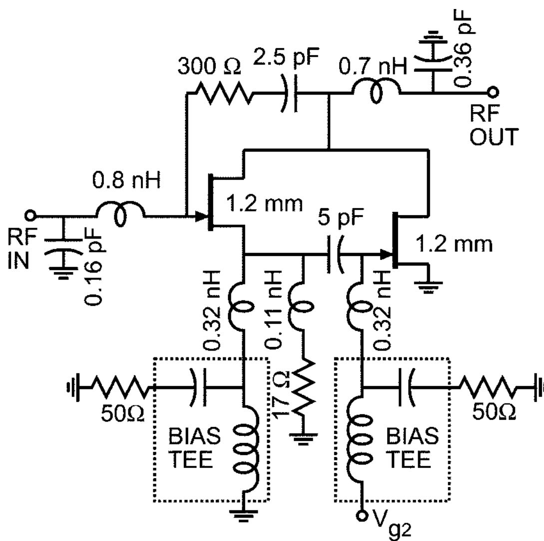

Fig. 20. Complete schematic of the GaN HEMT f_T-doubler resistive feedback power amplifier.

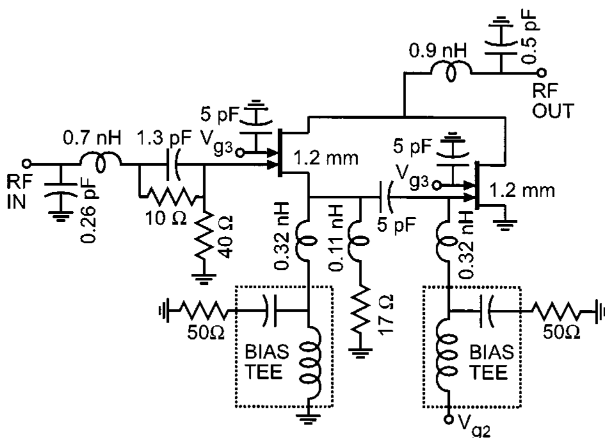

Fig. 21. Complete schematic of the GaN HEMT dual-gate cascode f_T-doubler resistive feedback power amplifier.

to AlN substrates (Fig. 19) which has the passive components (NiCr resistors, Si_3N_4 capacitors) and coplanar waveguide interconnects, and provides a low-resistance thermal path for

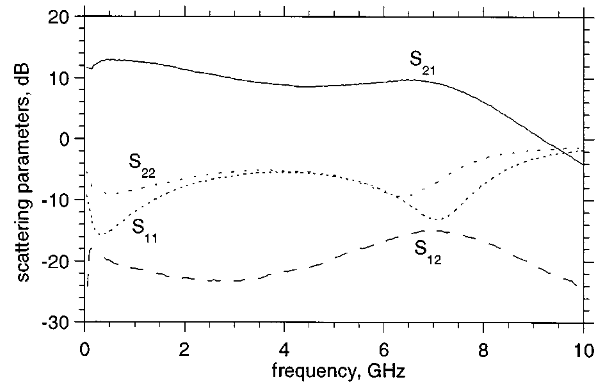

Fig. 22. Small-signal performance of the GaN HEMT f_T-doubler resistive feedback power amplifier.

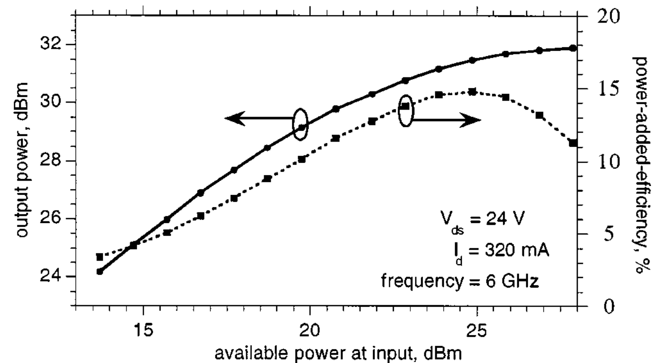

Fig. 23. Power performance of the GaN HEMT dual-gate cascode f_T-doubler power amplifier at 6 GHz ($V_{ds} = 24$ V, $I_d = 320$ mA).

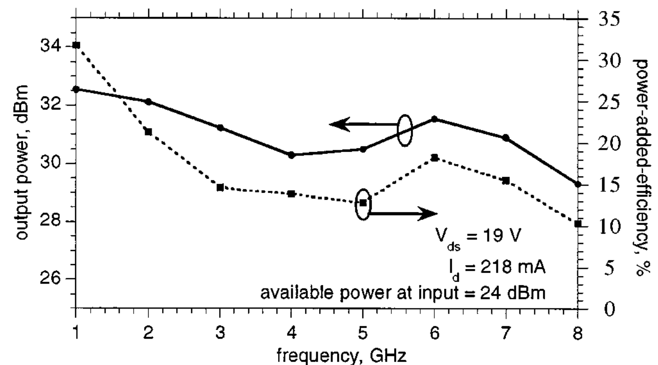

Fig. 24. Power performance of the GaN HEMT f_T-doubler resistive feedback power amplifier from 1 to 8 GHz ($V_{ds} = 19$ V, $I_d = 218$ mA, available power at input $= 24$ dBm).

efficient heat-sinking. The GaN die also provides a second plane of wiring for crossovers.

The single gate f_T-doubler power amplifier (Fig. 20) uses resistive feedback to match the input and output to 50 Ω. The dual-gate cascode f_T-doubler power amplifier (Fig. 21) uses capacitive division [3] to decrease gain and improve bandwidth. This design uses a resistive divider as a lossy input matching network. The divider also provides a low-impedance path for the gate bias preventing bias shifts at high RF drive. Biasing and π-section matching networks were done similar to the GaAs MESFET designs. The GaN die size is 1.1 mm × 1.45 mm for either circuit.

Measured small-signal scattering parameters of the resistive feedback power amplifiers (Fig. 22) shows ∼11-dB small-signal gain with 0.2 to 7.5-GHz bandwidth. The dual-gate cascode power amplifier provides ∼10-dB small-signal gain with 0.2 to 8-GHz bandwidth and up to 1.5-W output power with 15% PAE at 6 GHz (Fig. 23). The resistive feedback power amplifier (Fig. 24) provides >1-W output power over 1 to 7 GHz with >10% PAE. The bandwidth is limited by the large extrinsic drain–source capacitance $C_{\rm ds}$ resulting from the flip-chip bonding. Improved transistor pad layouts should reduce the capacitance by a factor of two and improve circuit bandwidth. In both circuits the output power is observed to saturate at power levels well below what was expected from the transistor dc characteristics. Output waveform measurements at 2 GHz with an oscilloscope indicate strong dc-RF dispersion in the HEMT I-V characteristics, possibly due to the presence of traps in the material. $V_{\rm Dsat}$ increases and $I_{\rm DSS}$ decreases when the device is operated at high frequencies. Also, leakage prevented complete cut-off of the channel current at high drain voltages.

IV. Conclusion

The f_τ-doubler topology is an alternative to the distributed amplifiers in realizing wideband power amplifiers with better efficiency in a smaller die area. An experimental circuit in a GaAs MESFET technology offering 18-GHz f_τ and 12-V breakdown has achieved 0.2 to 6-GHz bandwidth, ∼12-dB gain, >23-dBm output power and 25% PAE. The bandwidth is 33% of f_τ and the gain-bandwidth product is $1.3 \cdot f_\tau$. Similar circuits using GaN HEMTs have yielded ∼11-dB gain, 0.2 to 7.5-GHz bandwidth, ∼31.5-dBm output power, and up to 15% PAE. Circuits fabricated on improved material with reduced dc-RF dispersion have recently obtained up to 5-W output power over a similar bandwidth, and will be reported subsequently. Better physical layout of the flip-chip bonded devices will reduce $C_{\rm ds}$ and increase bandwidth and efficiency. The efficiency at higher frequencies can be increased further by using improved broadband output networks.

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