Submicron Transferred-Substrate Heterojunction Bipolar Transistors

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Abstract

We report submicron transferred-substrate AlInAs/GaInAs heterojunction bipolar transistors. Devices with 0.4 μm emitter and 0.4 μm collector widths have 17.5 dB unilateral gain at 110 GHz. Extrapolating at -20 dB/decade, the power gain cut-off frequency f_{max} is 820 GHz. The high f_{max} results from the scaling of HBT junction widths, from elimination of collector series resistance through the use of a Schottky collector contact, and from partial screening of the collector-base capacitance by the collector space charge.

Introduction

Very wide bandwidth heterojunction bipolar transistors (HBTs) [1], [2] will enable microwave analog-digital converters, microwave direct digital frequency synthesis, fiber-optic transmission at >40 Gb/s, and wireless data networks at frequencies above 100 GHz. Such ICs will demand very high transistor current gain cutoff frequency f_τ and power gain cutoff frequency f_{max}. While vertical scaling of the device increases f_τ, lateral scaling is also necessary to simultaneously obtain low values of base-collector capacitance C_{cb} and base resistance R_{bb}, contributing to high values of $f_{max} \sim \sqrt{f_\tau / 8\pi R_{bb} C_{cbi}}$, ($C_{cbi}$ is the fraction of C_{cb} charged through the base resistance R_{bb}). The transferred-substrate technology [3], allows both lateral and vertical scaling of the HBT dimensions. We had earlier reported transferred-substrate HBTs with 0.8 μm collector junction width and > 400 GHz f_{max} [3]. Here we report submicron devices fabricated using electron-beam lithography with estimated 820 GHz f_{max}, the highest reported for any transistor.

Device Design and Fabrication

The MBE epitaxial layer structure used in this work is identical to [3], except that the base is 40 nm thick, is Be-doped at 5×10^{19} cm^{-3} and uses 50 meV base bandgap grading, introduced by varying the Ga:In ratio. The fabrication process is similar to that described in [3]. Emitter contact metal is defined by E-beam lithography at 0.5 μm linewidth, which produces 0.4 μm wide base/emitter junction after the dry/wet etch process. Collector metal, with a "T" cross-section, is defined by E-beam lithography at 0.5 μm contact width (figure 1a). An isotropic collector recess etch to 0.05 μm depth forms collector-base junctions with a tapered profile, reducing C_{cb} while maintaining latitude for emitter-collector misalignment. After etching collector junction width is 0.4 μm. A device schematic cross-section is shown in figure 1b.

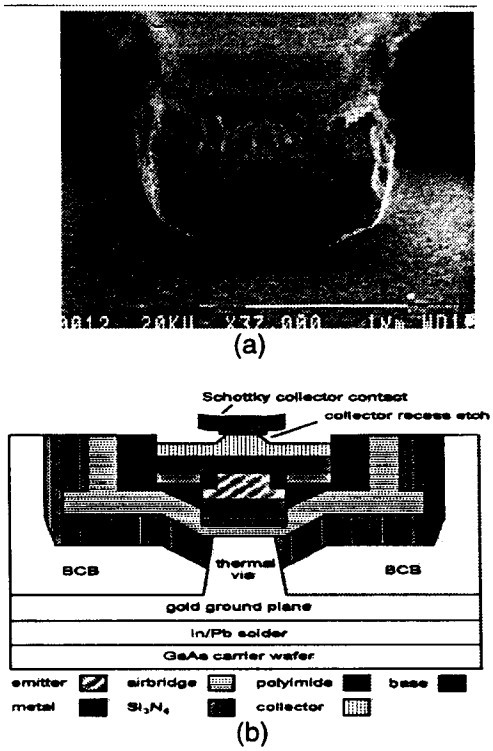

Fig. 1. (a) 0.4 μm Schottky collector stripe. (b) Schematic cross-section of transferred-substrate HBT.

Results

The devices were characterized by HP8510 on-wafer network analysis from 0 to 50 GHz and 75-110 GHz using (GGB Inc.) waveguide-coupled microwave wafer probes. To avoid measurement errors (in S_{12}, hence U) arising from microwave probe-probe coupling, the HBTs are separated from the probe pads by 230-μm-length on-wafer microstrip lines. On wafer calibration standards were used to de-embed

the transistor S-parameters. The standard Line-reflect-line (LRL) technique was used. Biasing at V_{ce} = 1.2 volts and I_c = 5.0 mA, devices with 0.4 μm emitter and 0.4 μm collector widths obtained 3.2 dB current gain and 17.5 dB unilateral power gain at 110 GHz (figure 2). Extrapolating at -20 dB/decade, the current gain cut-off frequency f_τ is 162 GHz and the power gain cut-off frequency f_{max} is a record 820 GHz. The common-emitter (figure 2) and common-base (not shown) maximum stable gains are 12.2 dB and 16.0 dB at 110 GHz.

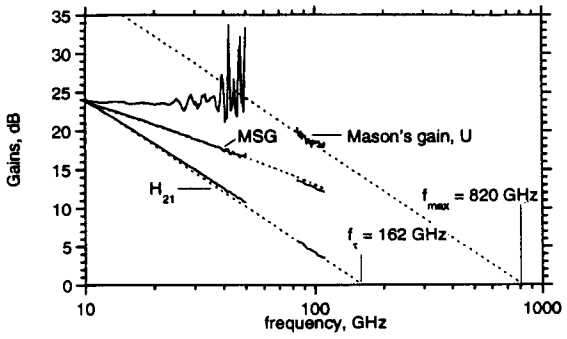

Fig. 2. Common-emitter RF characteristics of device with a 0.4 x 6 μm^2 emitter and a 0.4 x 10 μm^2 collector, biased at V_{ce} = 1.2 V and I_c = 5 mA.

Figure 3 shows a small-signal hybrid-π model for a device with a 0.4 x 6 μm^2 emitter and a 0.4 x 10 μm^2 collector biased at I_c = 5 mA and V_{ce} = 1.2 V. The forward time delay ($\tau_f = \tau_b + \tau_c$), the base emitter depletion capacitance, the base collector output resistance and the base collector capacitance were extracted form the s-parameters of the device measured as a function of the bias.

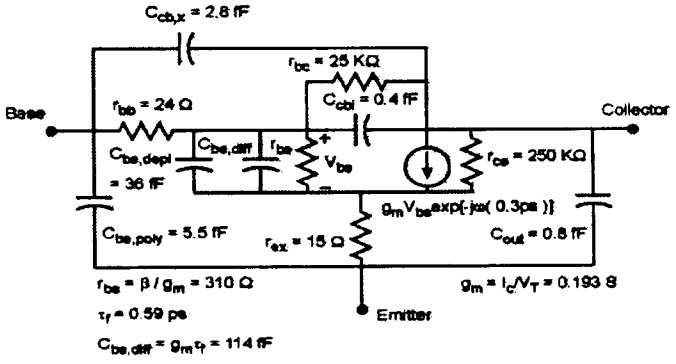

Fig. 3. Device equivalent circuit model at V_{ce} = 1.2 V and I_c = 5 mA.

The rest of the component's values shown in Figure 3, were calculated form the physical dimensions of the device and process parameters (e.g. sheet resistance). The value of C_{cbi} = 0.4 fF was determined by fitting to the measured unilateral gain. This value is smaller than the intrinsic dielectric capacitance ($\varepsilon A_E/T_c$ = 0.88 fF, T_c the collector thickness) due to the differential space-charge effect [5], [6], [7]. The C_{cbi} cancellation can be evaluated experimentally by measuring the change of f_τ with V_{ce}, using $C_{cbi} = \varepsilon A_E/T_c - I_E \times \partial\tau_c/\partial V_{bc}$ [5]. The measured f_τ vs. V_{ce} indicates $\partial\tau_c/\partial V_{bc}$ ~ 0.1 ps/Volt, predicting C_{cbi} ~ 0.38 fF at I_c = 5 mA. The extracted value of C_{cbi} (0.4 fF) is 2.2:1 smaller than the expected zero-current capacitance ($\varepsilon A_E/T_c$ = 0.88 fF).
Comparing the present results with those reported in [3], the high f_{max} value results from scaling of HBT junction widths and from partial screening of the collector-base capacitance by the collector space charge.

Conclusions

We have demonstrated submicron transferred-substrate heterojunction bipolar transistors. Devices with 0.4 x 6 μm^2 emitters and 0.4 x 10 μm^2 collectors obtained an extapolated f_τ of 162 GHz and f_{max} of 820 GHz. With further scaling, HBTs with > 1000 GHz f_{max} should be feasible, pemitting ICs operating above 300 GHz.

Acknowledgments

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