InAlAs/InGaAs HBTs with Simultaneously High Values of F_τ and $F_{\max}$ for Mixed Analog/Digital Applications

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***Abstract*—We report the design, fabrication, and measurement of InAlAs/InGaAs heterostructure bipolar transistors (HBTs) designed for high speed digital circuits. At 0.96 V V_{CE} the current gain cutoff frequency, f_τ, is 300 GHz and the maximum frequency of oscillation, $f_{\max}$, is 235 GHz. This value of f_τ is the highest reported for bipolar transistors. At a slightly higher V_{CE} bias, a high value of 295 GHz for f_τ and $f_{\max}$ were obtained simultaneously.**

***Index Terms*—HBTs.**

I. Introduction

FAST HBTs have become key components in digital communication systems, direct digital frequency synthesizers, and radar. ICs for these applications frequently combine digital and analog subcircuits. While for analog applications the values of f_τ and $f_{\max}$ are important, for digital circuits the base collector capacitance, C_{cb}, base-emitter junction capacitance, C_{je}, current density, and f_τ are the main parameters determining the circuit speed.

By lateral and vertical scaling of the device dimensions InAlAs/InGaAs transferred-substrate HBTs have shown very high current-gain and power-gain cutoff frequencies [1], [2]. In this work, the HBT was designed for high-speed digital circuits while maintaining a high $f_{\max}$ for wide-band analog circuits. This was achieved by adjustment of the collector to emitter stripe width ratio, by using a thin collector drift layer, and by introducing an additional process step to reduce parasitic layout capacitance. A record 300 GHz f_τ with a corresponding 235 GHz $f_{\max}$ was measured at a 1.5 mA/μm^2 current density and 0.96 V V_{CE}. Simultaneously, a high value of 295 GHz for f_τ and $f_{\max}$ was measured at a slightly increased V_{CE}. Device speed is only slightly reduced at a high 2 mA/μm^2 current density.

II. Device Design for Digital Applications

A detailed charge control delay analysis of emitter coupled logic (ECL) gates, similar to the one shown in [3], and applied to two-level series-gated ECL circuits [4], results in a delay expression in which the time constants $C_{cb}\Delta V_{\log ic}/I_0$, $R_{bb}C_\pi$, and τ_F are significant terms. Here, C_{cb} is the base collector capacitance, I_0 the driving current, $\Delta V_{\log ic}$ the voltage swing, R_{bb} the base resistance, C_π the large-signal base-emitter capacitance, and τ_F the forward delay. Using the dimensions defined in Fig. 1, the delay term associated with C_{cb} can be written as follows:

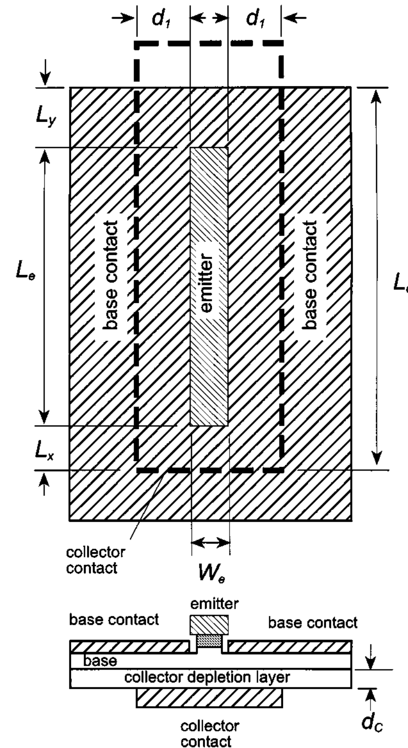

Fig. 1. Schematic top and side view of a transferred-substrate HBT. L_E and W_E are emitter length and width, respectively. d_1 is the alignment width tolerance between the collector and emitter stripes and L_x and L_y are the alignment length tolerances between the collector and emitter stripes.

$$\left[\frac{\Delta V_{\log ic}}{J_0}\right]\left[\frac{\varepsilon}{d_C}\right]\left(1+\frac{2d_1}{W_E}\right)\left(1+\frac{L_x+L_y}{L_E}\right) \qquad (1)$$

where J_0 is the emitter current density and d_C the depletion depth. To increase logic speed (d_1/W_E) and $((L_x+L_y)/L_E)$ should be minimized. An increase of W_E also increases R_{bb} and hence its associated delay terms. For a given base sheet resistance and emitter-collector alignment tolerance, d_1, an optimum value for W_E can be found for minimum ECL gate delay.

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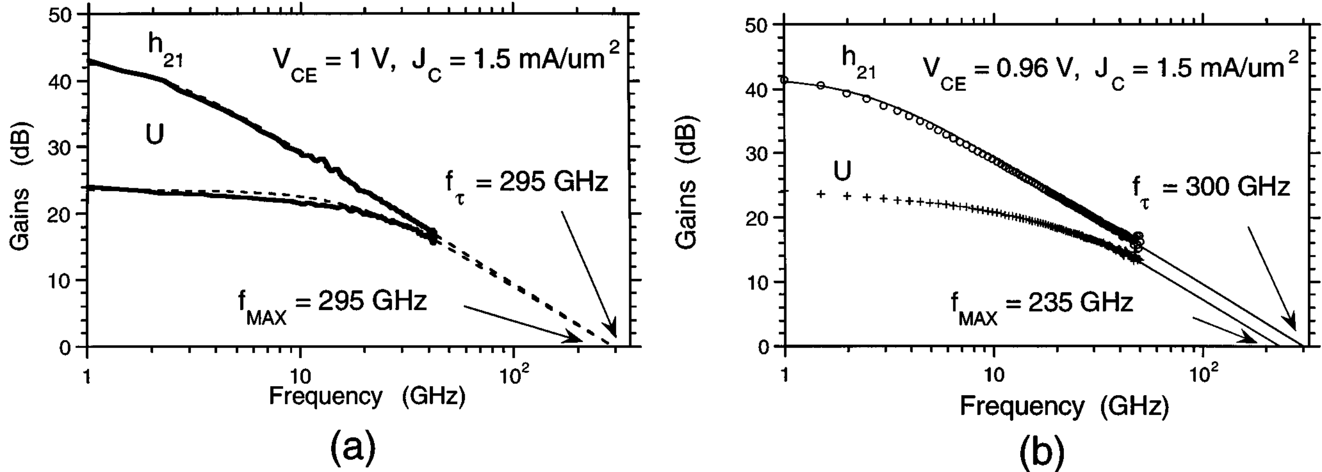

Fig. 2. Measured data and curve fit of h_{21} and Mason' Gain (U) at (a) $VCE = 1$ V and (b) $VCE = 0.96$ V. Current density was 1.5 mA/μm^2. Device mesa dimensions: Emitter 1×8 μm^2, Collector 2×8.5 μm^2.

In this design, d_1 was 0.4 μm and the base sheet resistance was 800 Ω/sq. The emitter mask stripe width was chosen to be 1.2 μm corresponding to 1.0 μm junction width. After W_E is determined, the value of L_E is determined from the required device operating current.

High current density operation is essential for high-speed logic [see (1)]. This is one of the reasons for the success of SiGe based digital circuits [5]. For a given value of V_{CE}, maximum current density as limited by the Kirk effect is proportional to $1/d_C^2$ [6]. For a device operating at the Kirk effect threshold, the time constant $(\Delta V_{\mathrm{Log}ic} \times C_{cb}/I_C)$ is therefore, proportional to d_C and is reduced by thinning the collector. The breakdown voltage of the base-collector diode determines the minimum value of d_C. This enhances the importance of wide bandgap collector structures for digital design.

Reducing the value of d_C also improves τ_F because the collector delay is reduced. As shown below the collector delay is the dominant delay term in $\tau_{EC} = 1/(2\pi f_\tau)$. The value of d_C for the device presented here was 200 nm which supported current densities of the order of 2 mA/μm^2.

III. Device Fabrication and Testing

The HBT layers were grown by molecular beam epitaxy, using Be for p-doping and Si for n-doping. The layer structure consisted of a 8×10^{17} cm^{-3} n-type InAlAs emitter, digital grading layers between emitter and base, a 30 nm p-type InGaAs base doped to 4×10^{19} cm^{-3} with a 2 kT composite grading, and a 1×10^{16} cm^{-3} n-type doped 200 nm InGaAs collector. The devices were fabricated using a substrate-transferred process, as described in [7]. The emitter and collector dimensions were 1.2 μm $\times$ 8 μm and 2 μm $\times$ 8.5 μm, respectively.

The s-parameters of the devices were measured as a function of bias. On wafer, line reflect line (LRL) calibration standards were used for measuring the s-parameters up to 50 GHz. The use of the LRL method eliminates the necessity to de-embed the input pad capacitance, a step that greatly affects the extracted value of f_τ.

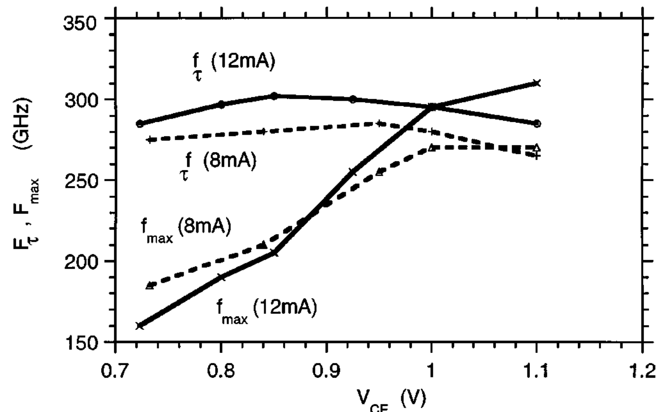

Fig. 3. Dependence of f_τ and $f_{\max}$ on collector voltage V_{CE} for the device in Fig. 2(a). The collector current densities were $J_C = 1$ mA/μm^2 and 1.5 mA/μm^2.

IV. Results and Discussion

The values of f_τ and $f_{\max}$ were extracted using a single pole approximation fit to h_{21} and Mason's gain (U), respectively. The measured data and extrapolations for h_{21} and U on two different devices are shown in Fig. 2(a) and (b) for $V_{CE} = 1$ V and $V_{CE} = 0.96$ V, respectively. The current density for both measurements was $J_C = 1.5$ mA/μm^2. The figures present data from devices that demonstrate simultaneous 295 GHz f_τ and $f_{\max}$ and a record 300 GHz f_τ. Fig. 3 shows the dependence of f_τ and $f_{\max}$ on V_{CE} measured at current densities of 1 mA/μm^2 and 1.5 mA/μm^2 for the device shown in Fig. 2(a). The slight decrease of f_τ for high V_{CE} values is due to decreased electron velocity in the collector under high fields. At low V_{CE} values $f_{\max}$ is relatively low due to the Kirk effect, which results in a high C_{cb} value.

These transistors have very low BV_{CEO}. The BV_{CBO} is somewhat higher at ~2.0 V at 2 mA/μm^2; because of this, we were able to build and test ECL 2 : 1 static frequency dividers with these transistors. These dividers operated at a maximum 53 GHz clock rate. Further thinning of the InGaAs collector region to achieve higher f_τ would result in BV_{CEO}

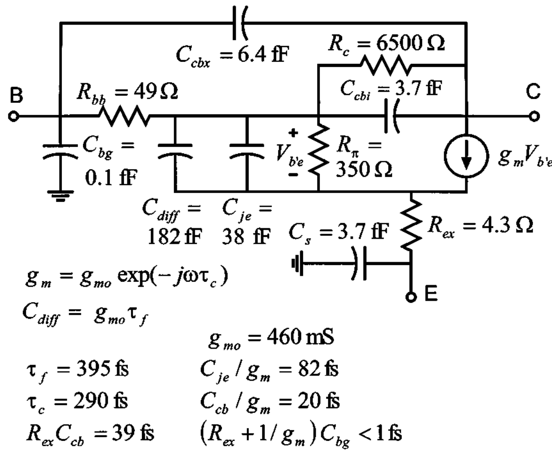

Fig. 4. Small signal equivalent circuit and delay terms at a bias point of $V_{CE} = 1$ V, $J_C = 1.5$ mA/μm^2.

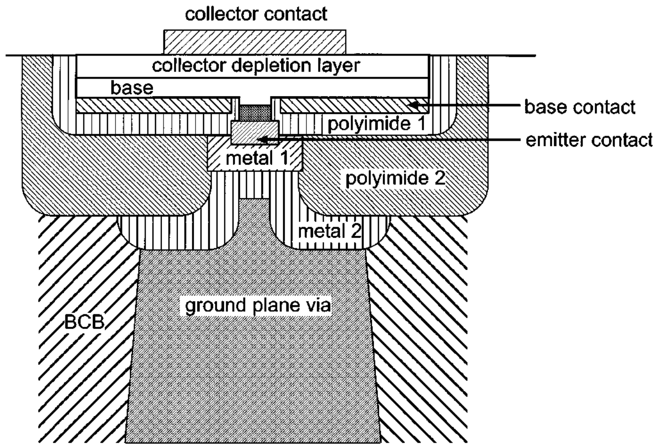

Fig. 5. Cross-sectional schematic of the transferred-substrate HBT including the additional polyimide two layer in order to reduce base-to-ground capacitance, C_{bg}.

and BV_{CBO} that are too low for circuit applications, and InP collectors would be needed.

From the variation of the s-parameters with bias and from the known device geometry, a small-signal equivalent circuit was extracted (Fig. 4). The different time constants contributing to $\tau_{CE} = 1/(2\pi f_\tau)$ are also shown in Fig. 4. The forward transit delay, τ_F, contributed ~74% of the total delay ($\tau_c \sim 285$ fs, τ_b ~90 fs) while the base-emitter junction capacitance, C_{je}, and the base collector capacitance, C_{cb}, contributed ~14% and ~12% of the total delay, respectively. When comparing these results to previously published data in [2], the higher value of f_τ shown here is due to a thinner base, a reduction of the $R_{ex}C_{cb}$ time constant, and the elimination of a parasitic base-to-ground capacitance, C_{bg}. The latter was achieved by inserting an additional polyimide dielectric spacer layer into the process. The additional polyimide layer shown in Fig. 5 increases the spacing between the base contacts and the wide metal ground plane delivered through the BCB via. Process constraints prevent the etching of narrow vias through the 5-μm thick BCB dielectric. In order to further increase the value of f_τ and simultaneously maintain high $f_{\max}$, it is necessary to reduce the thickness of the collector together with a lateral scaling of the device dimensions. A wide bandgap InP collector layer might be necessary in order to prevent the thin collector from breaking down at less then 1.5 V bias.

In conclusion, InAlAs/InGaAs HBTs with simultaneous high values of f_τ and $f_{\max}$ were fabricated and tested. The resulting f_τ of 300 GHz is the highest ever reported for bipolar transistors.

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