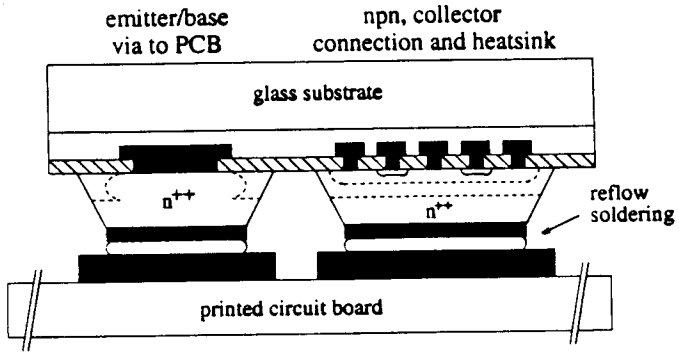
ADVANCE PROGRAM

2000 IEEE BIPOLAR/BiCMOS CIRCUITS AND TECHNOLOGY MEETING

MARRIOTT CITY CENTER HOTEL
MINNEAPOLIS, MINNESOTA

SEPTEMBER 25 & 26, 2000

SHORT COURSE — SEPTEMBER 24, 2000



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2000 BCTM

SCHEDULE AT A GLANCE

Sunday — September 24			
8:45 AM — 5:15 PM	SHORT COURSE Basic Building Blocks for RF BiCMOS Process Technology		
7:30 PM	Registration/Reception		
Monday — September 25 Registration open from 7:30 AM in Ballroom Atrium			
8:00 AM	Opening Remarks and Announcements		
8:15 AM — 9:00AM	Keynote Speaker Prof. Mark Rodwell Bipolar Transistor ICs: 50GHz and Beyond Ballrooms 1 and 2		
9:00 AM	Coffee and Cookies in Ballroom Atrium		
9:20 AM — 11:00 AM	Emerging Smart Power Technologies Ballroom 3	Wireless Circuits Ballroom 4	
11:00 AM	Visit Vendor Exhibitions		
11:30 AM	Lunch + Luncheon Speaker: Dr. Else Kooi Ballrooms 1 and 2		
1:20 PM — 3:00 PM	Advanced BJT Modeling Ballroom 3	Analog and Digital Circuit Design Ballroom 4	
3:00 PM	Coffee in Ballroom Atrium		
3:20 PM — 5:25 PM	Novel Power Devices Ballroom 3	Communication Technologies Ballroom 4	PA Device Physics Ballroom 1
Author Interviews Immediately After Sessions			
Dinner Break			
7:45 PM	Complementary Refreshments in Atrium		
8:00 PM	Panel Session Will the Future RFIC Companies be Fabless? Ballroom 3		
Tuesday — September 26			
8:00 AM — 10:15 AM	Special Session: New Technology Directions Ballrooms 1 and 2		
10:15 AM	Coffee Break in Ballroom Atrium		
10:30 AM — 12:10 PM	RF Building Blocks Ballroom 3	BJT Modeling and Parameter Extraction Ballroom 4	
12:10 PM	Lunch / Exhibition Reception in Atrium		
1:50 PM — 3:55 PM	RF Components Ballroom 3	Topics in HBT Technologies Ballroom 4	
Author Interviews Immediately After Sessions			

WELCOME AND OPENING REMARKS

8:00 - 8:15 AM — GRAND PORTAGE BALLROOMS 1-2

KEYNOTE SPEECH

8:15 - 9:00 AM — GRAND PORTAGE BALLROOMS 1-2

Bipolar Transistor ICs: 50GHz and Beyond

Prof. Mark Rodwell, (Univ. of California, Santa Barbara) Y. Betser, S. Jaganathan, S. Krishnan, T. Mathew, Y. Wei, M. Urteaga, D. Scott, S. Long (Univ. of California, Santa Barbara), R. Smith, S. Martin (NASA/JPL)

Research in wideband heterojunction bipolar transistors is driven by applications in high frequency communications and radar. Significant military applications include RF/microwave delta-sigma ADCs, DACs, and digital frequency synthesis. ICs for 10-40Gb/s fiber transmission are of immediate commercial significance. Si/SiGe and InP HBTs are now competing for these markets. 100GHz clock rates will soon be realized in small-scale digital ICs, and 160Gb/s fiber transmission ICs will soon be feasible in the laboratory. While InP offers strong heterojunctions, very high base doping, and very high collector electron velocities, Si/SiGe devices have been much more aggressively scaled and operate at much higher current densities. To compete effectively with Si for analog circuits, InP HBTs must be scaled to deep submicron dimensions; critically, for digital circuits InP HBT current densities must also be increased to well above 200kA/cm^2. Submicron InP HBTs fabricated at UCSB have obtained 300GHz current-gain cutoff frequencies and (extrapolated) 1100GHz power-gain cutoff frequencies. Circuit results include DC-80GHz lumped amplifiers and 66GHz master-slave latches. Large-scale digital ICs operating above 50GHz combine the wiring density of digital ICs with the bandwidth of monolithic millimeter-wave ICs; substantial improvements are required of the wiring environment. We will describe our efforts in thin polymer-microstrip interconnects and low-voltage-swing logic.

9:00 - 9:20 PM — Break (Coffee and Cookies)

1. Emerging Smart Power Technologies

Monday AM — Ballroom 3
Session chair: Rik Jos
Co-chair: Frank Thiel

(1.1) 9:20 - 10:10 AM — Bipolar Devices in Advanced Power BiCMOS Technology (Invited Paper)

T. Efland, R. Teggatz, J. Devore, S. Pendharkar, A. Hastings (Texas Instruments)

Technology is driven by the evolving CMOS roadmap, and it is increasingly difficult to integrate good bipolar transistors in modern CMOS processes. Two examples are given, with details of the difficulties involved for a typical advanced power BiCMOS technology with respect to design concerns. In addition, bipolar issues relating to guardring, parasitic, and ESD concerns are discussed. Lastly a table of key circuits dependent on bipolar transistors is outlined.

(1.2) 10:10 - 10:35 AM — Analysis and Compact Modeling of a Vertical Grounded-Base NPN Bipolar Transistor used as an ESD Protection in a Smart Power Technology (Student Paper)

G. Bertrand (LAAS, France), C. Delage (ON Semiconductor, France), M. Bafleur, N. Nolhier, J. Dorkel (LAAS, France), Q. Nguyen (ON Semiconductor, France), N. Mauran (LAAS, France), P. Perdu (CNES, France)

A thorough analysis of the physical mechanisms involved in a vertical grounded-base NPN bipolar transistor (VGBNPN) under an ESD stress is first carried out by using 2D-device simulation, square pulse measurement (TLP) and photoemission experiments. As a result, we propose a physics-based compact model that reproduces the unexpected low value of the VGBNPN snapback holding voltage under TLP stress.

(1.3) 10:35 - 11:00 AM — Integration of High-voltage Bipolars into a 0.35μm CMOS Based Smart Power Platform

V. Parthasarathy, R. Zhu, V. Khemka, M. Ger, T. Bettinger, S. Chang, P. Hui, A. Bose (Motorola)

The integration of optimized high-voltage bipolar components in a 0.35μm CMOS based smart power platform is achieved through the use of advanced implantation techniques that did not exist in older diffusion based technologies.

2. Wireless Circuits

Monday AM — Ballroom 4
Session chair: Scott Williams
Co-chair: Leo de Vreede

(2.1) 9:20 - 9:45 AM — Fully Integrated W-CDMA IF Receiver and Transmitter including IF Synthesizer and on-chip VCO for UMTS Mobiles

W. Thomann, J. Fenk (Infineon Technologies, Germany), R. Hagelauer, R. Weigel (Univ. of Linz, Austria)

A fully integrated Si-bipolar IF receiver and transmitter with on-chip synthesizer for use in third-generation W-CDMA mobiles is introduced. Both devices in a small outline leadless package incorporate an on-chip IF synthesizer with on-chip VCO tuning and tank as well as 5th order baseband filters and comply with ARIB W-CDMA and UMTS standards.

(2.2) 9:45 - 10:10 AM — A SiGe-Bipolar Down-Conversion Mixer for a UMTS Zero-IF Receiver (Student Paper)

H. Pretl, W. Schelmbauer (Univ. of Linz, Austria), B. Adler (Infineon Technologies, Germany), L. Maurer, (Univ. of Linz, Austria), J. Fenk, (Infineon Technologies, Germany), R. Weigel (Univ. of Linz, Austria)

A down-conversion I/Q-mixer is reported that has been implemented in a 75GHz f_t bipolar SiGe technology, including I/Q-generation and biasing. Achieving high IIP2 and low local oscillator leakage it is intended to be used in a zero-IF receiver front-end for UMTS.

(2.3) 10:10 - 11:00 AM — Integrated Transceivers for Digital Cordless Applications (Invited Paper)

S. Heinen (Infineon)

Over the last decade the RF-IC integration level has shown significant