# High $F_\tau$ and $F_{max}$ InAlAs/InGaAs Transferred-Substrate HBTs

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We report the design, fabrication and measurement of a high speed InAlAs/InGaAs Heterostructure Bipolar Transistor (HBT). At a $V_{CE}$ of 0.96 V the current gain cutoff frequency, $f_\tau$, and the maximum frequency of oscillation, $f_{max}$, were 300 GHz and 235 GHz, respectively. This value of $f_\tau$ is the highest ever reported for bipolar transistors. At a slightly higher $V_{CE}$ bias, simultaneously high values of $f_\tau$= 293 GHz and $f_{max}$ =275 GHz were obtained.

Fast HBTs have become key components in future and present designs for 100GHz digital communication systems, direct digital frequency synthesizers and radar. To achieve these goals, it is essential for the device to have simultaneous high values of $f_\tau$ and $f_{max}$, capability for high current density operation and a low extrinsic base collector capacitance.

The HBT layers were grown by Molecular beam Epitaxy, using Be for p-doping and Si for n-doping. The layer structure consisted of a $8x10^{17}$ $cm^{-3}$ n-type InAlAs emitter, digital grading layers between emitter and base, a 30 nm p-type InGaAs base doped to $4x10^{19}$ $cm^{-3}$ with a 2KT composite grading, and a $1x10^{16}$ $cm^{-3}$ n-type doped 200 nm InGaAs collector. The relatively thin collector is essential for high current density operation due to the Kirk effect. The devices were fabricated using a substrate- transferred process, as described in [1].

In Fig. 1 are shown common emitter (CE) and common base (CB) characteristics of a device under test. The device's emitter and collector mesa dimensions were 1 x 8 $\mu m^2$ and 2 x 8.5 $\mu m^2$, respectively. The CE current gain was >100 at high current densities which is the reason for the relatively low CE breakdown voltage. For digital circuits however, the CB breakdown voltage is important. The devices sustained a $V_{CB}$ of 1V up to current densities of 1 mA/$\mu m^2$ (see Fig. 1b) and a $V_{CB}$ of 0.5V up to current densities of 2 mA/$\mu m^2$ (not shown here). This is sufficient for use of these devices for digital applications.

The S-parameters of the devices were measured as a function of bias. On wafer, Line Reflect Line (LRL) calibration standards were used for measuring the s-parameters up to 50 GHz. The use of the LRL method eliminates the necessity to de-embed the input pad capacitance, a step which highly affects the extracted value of $f_\tau$. The value of $f_\tau$ was extracted by using a single pole approximation fit to $h_{21}$. A –20 dB/dec extrapolation was used to extract $f_{max}$ from Mason's gain (U). The measured data and curve fits for $h_{21}$ and U are shown in Fig 2a and Fig. 2b for $V_{CE}$=0.96 V and $V_{CE}$=1V, respectively. The current density was $J_C$=1.5 mA/$\mu m^2$. The dependence of $f_\tau$ and $f_{max}$ on $V_{CE}$ is shown in Fig. 3. As expected, the change in $f_{max}$ is significant while $f_\tau$ stays almost constant. The slight decrease of $f_\tau$ for high $V_{CE}$ values is due to an increase in the forward delay.

From the variance of the s-parameters with bias and from the device geometry, an equivalent small signal circuit diagram of the HBT was extracted and is shown in Fig. 4. The different time constants contributing to $\tau_{CE}=1/(2\pi f_\tau)$ are also shown in Figure 4. The forward transit delay, $\tau_F$, contributed as much as ~73% of the total delay, while the base emitter junction capacitance, $C_{je}$, and the base collector capacitance, $C_{cb}$, contributed ~15% and ~11% of the total delay, respectively. When comparing these results to the previously published data in [2], the higher value of $f_\tau$ shown here is due to a thinner base, a reduction of the $R_{ex}C_{cb}$ time constant and the elimination of a parasitic base to ground capacitance, $C_{bg}$. The latter was achieved by insertion of a thick Polyimide layer between the base metal and the ground plane. The value of $R_{ex}C_{cb}$ was reduced by scaling-down the area ratio between collector and emitter mesas. In order to further increase the value of $f_\tau$ and simultaneously keep a high value of $f_{max}$, it is necessary to reduce the thickness of the collector together with a lateral scaling of the device dimensions. A wide gap material for the collector layer might be necessary in order to prevent the thin collector from breaking down.

In conclusion, InAlAs/InGaAs HBTs with simultaneous high values of $f_\tau$ and $f_{max}$ were fabricated and tested. The resulting $f_\tau$ of 300 GHz was the highest ever reported for bipolar transistors.

1. Q. Lee et al. "Sub-micron transferred-substrate HBTs", *1999 IEEE Conference IPRM, Davos, Switzerland, May 1999.*
2. D. Mensa et al. "Transferred-substrateHBTs with 254 GHz ft", *Electronics letters, vol. 35 (7) pp.605-606, 1999.*

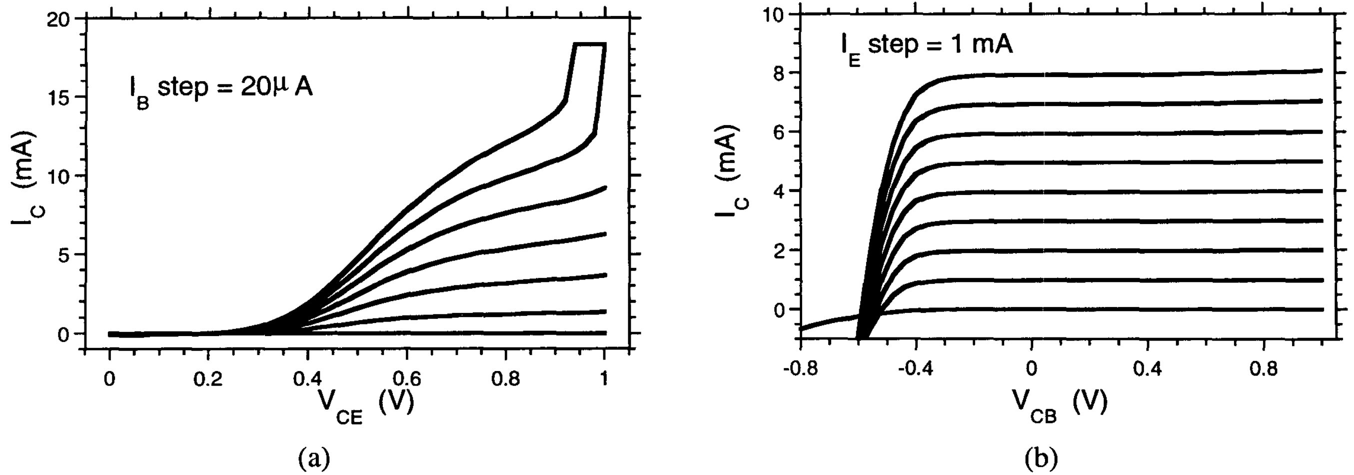


Figure 1 – (a) Common emitter and (b) common base characteristics.
Device mesa dimensions: Emitter 1 x 8 $\mu m^2$, Collector 2 x 8.5 $\mu m^2$.

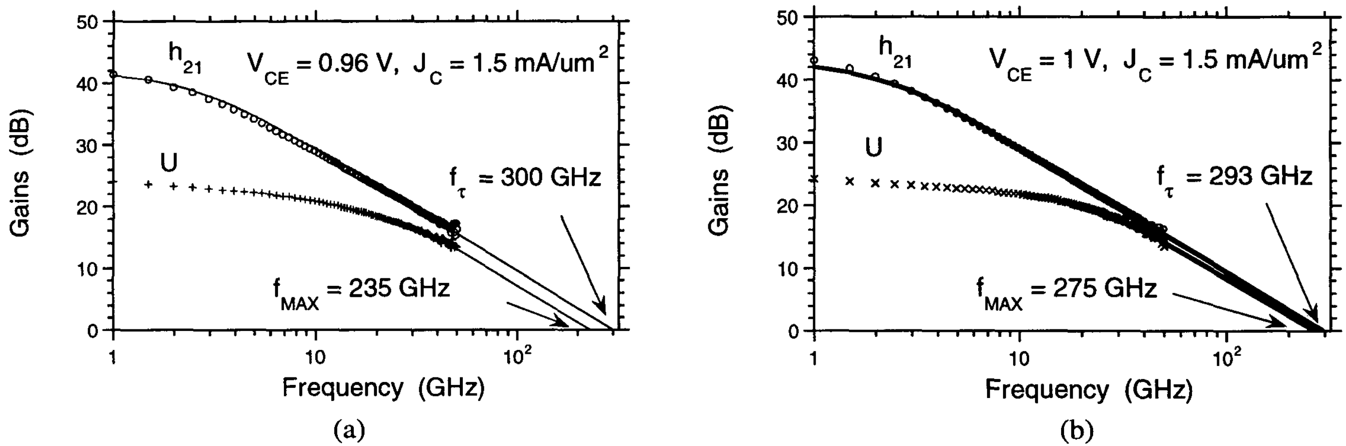


Figure 2 – Measured data and curve fit of $h_{21}$ and Mason' Gain (U) at (a) VCE = 0.96 V and (b) VCE = 1 V. Device mesa dimensions: Emitter 1 x 8 $\mu m^2$, Collector 2 x 8.5 $\mu m^2$.

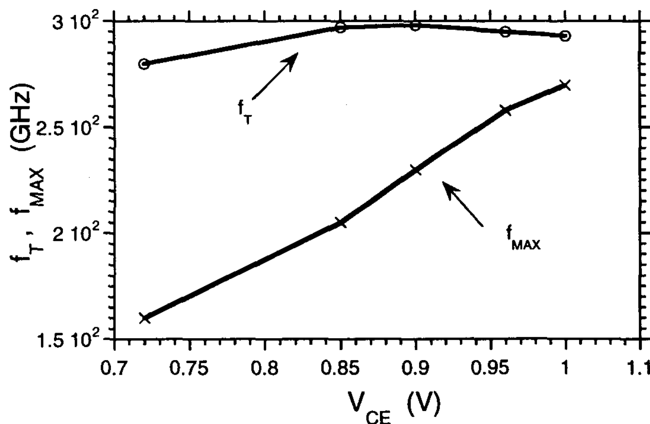


Figure 3 – Dependence of $f_\tau$ and $f_{max}$ on collector voltage $V_{CE}$. The collector current density was $J_C$ = 1.5 mA/$\mu m^2$.

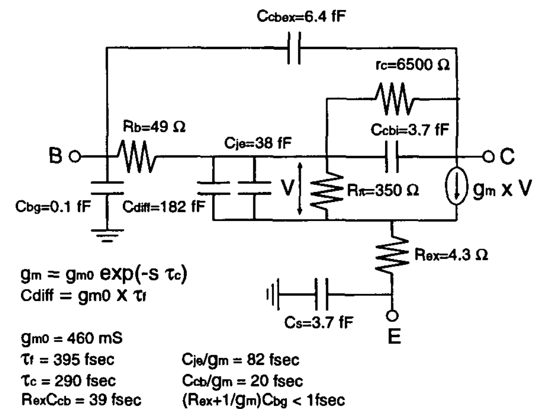


Figure 4 – Small signal equivalent circuit and delay terms at a bias point of $V_{CE}$ = 1V, $J_C$ = 1.5 mA/ $\mu m^2$.