ductance FETs (NOTFET)," in *IEEE Indium Phosphide and Related Materials Conf. Dig.*, 1990, p. 24.
[5] R. Majidi-Ahy *et al.*, "5-100 GHz InP CPW MMIC 7-section distributed amplifier," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1990, pp. 31–34.
[6] R. Majidi-Ahy *et al.*, "94 GHz InP MMIC five-section distributed amplifier," *Electron. Lett.*, vol. 26, no. 2, pp. 91–92, Jan. 1990.
[7] N. Camilleri *et al.*, "A W-band monolithic amplifier," in *IEEE Int. Microwave Symp. Dig.*, 1990, pp. 903–906.
[8] K. H. G. Duh *et al.*, "W-band InGaAs HEMT low noise amplifiers," in *IEEE Int. Microwave Symp. Dig.*, 1990, pp. 595–598.
[9] C. Yuen *et al.*, "High-gain, low-noise monolithic HEMT distributed amplifiers up to 60 GHz," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1990, pp. 23–26.
[10] R. Majidi-Ahy *et al.*, "100 GHz active electronic probe for on-wafer *S*-parameter measurements," *Electron. Lett.*, vol. 25, no. 13, pp. 828–830, 1989.
[11] R. Majidi-Ahy *et al.*, "100 GHz high-gain InP MMIC cascode amplifier," in *IEEE GaAs IC Symp. Proc.*, 1990, pp. 173–176.
[12] Y. C. Pao *et al.*, "Impact of surface layer on InAlAs/InGaAs/InP high electron mobility transistors," *IEEE Electron Device Lett.*, vol. 11, no. 7, pp. 312–314, 1990.
[13] L. E. Dickens *et al.*, "A GaAs wideband cascode MMIC amplifier," in *IEEE GaAs IC Symp. Proc.*, 1983, pp. 112–124.

33-GHz Monolithic Cascode AlInAs/GaInAs Heterojunction Bipolar Transistor Feedback Amplifier

Mark Rodwell, J. F. Jensen, W. E. Stanchina, R. A. Metzger, D. B. Rensch, M. W. Pierce, T. V. Kargodorian, and Y. K. Allen

Abstract—**Microwave cascode feedback amplifiers with 8.6-dB gain and dc to 33-GHz bandwidth were developed. The amplifiers utilize AlInAs/GaInAs heterojunction bipolar transistors having $f_{max} = 70$ GHz and $f_\tau = 90$ GHz. Active bias networks eliminate the need for on-wafer Si_3N_4 bypass capacitors.**

I. Introduction

COMPARED to hybrid microwave integrated circuits (MIC's), monolithic microwave/millimeter-wave integrated circuits (MIMIC's) potentially have lower cost, size, and weight, and with large-scale integration will permit low-cost integrated microwave systems. With many monolithic amplifier designs, these potential advantages are lost through inefficient use of the substrate area, with transmission lines consuming 90–95% of the die. The die size per circuit function is large, resulting in high cost, and limiting integration to 1–2 gain stages per die.

Compared to matched amplifiers, feedback amplifiers attain smaller bandwidths for a given f_{max}, but occupy small die areas and have well-controlled characteristics set by the feedback elements. This results in lower cost, and permits higher levels of system integration per die. Feedback amplifiers dominate in broad-band applications below 4 GHz, where transistors of adequate f_{max} are readily available.

Using (20-GHz f_{max}, 10-GHz f_τ) silicon bipolar transistors in the Darlington configuration, 8-dB gain has been attained with dc to 6 GHz [1]. With (20–30-GHz f_{max} and f_τ) GaAs/AlGaAs bipolar transistors in the Darlington configuration, 11-dB gain has been attained with dc to 10 GHz [2].

Heterojunction bipolar transistors in the AlInAs/GaInAs system [3] on InP substrates [4] have attained 70-GHz f_{max} and 90-GHz f_τ [3]. Using these devices, we have developed cascode feedback amplifiers with 8.6-dB gain and dc to 33-GHz bandwidth [5]. For comparison, a common-emitter feedback amplifier on the same wafer attained 8.6-dB gain and dc to 14-GHz bandwidth.

Manuscript received March 21, 1991; revised July 3, 1991.

M. Rodwell is with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106.
J. F. Jensen, W. E. Stanchina, R. A. Metzger, D. B. Rensch, M. W. Pierce, T. V. Kargodorian, and Y. K. Allen are with Hughes Research Laboratories, Malibu, CA 90265.

IEEE Log Number 9102698.

II. AlInAs/GaInAs HBT Technology

Heterojunction bipolar transistors (HBT's) provide substantially greater power gain cutoff frequencies than homojunction devices. In AlGaAs/GaAs devices [6], the wide-bandgap emitter permits larger base doping without significant charge injection into the emitter, giving low base resistance even with small base widths. The emitter doping can be dropped, reducing base–emitter depletion capacitance. Compared to GaAs/AlGaAs devices, the AlInAs/GaInAs HBT has a greater electron mobility and peak electron velocity in the base and collector, with consequent reduction in the base and collector transit times. The larger AlInAs/GaInAs bandgap discontinuity results in higher emitter injection efficiencies. GaInAs's smaller bandgap (than GaAs's) results in smaller base–emitter voltages, reducing power–delay products in digital circuits.

The AlInAs/GaInAs HBT device layers were grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating InP substrate. The layers were all lattice matched to the substrate and consisted of a 800-nm N^+ InGaAs subcollector, a 270-nm N^- GaInAs collector region doped at $4\times10^{16}/cm^3$, a 80-nm P^+ GaInAs base

0018-9200/91/1000-1378$01.00

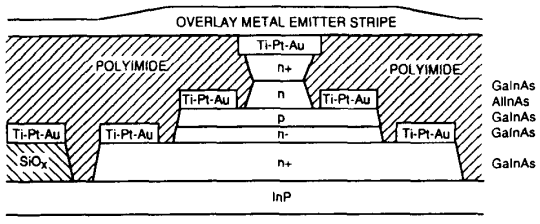
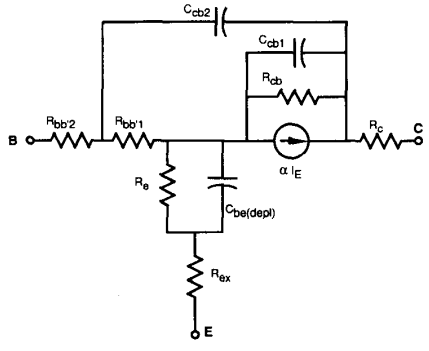


Fig. 1. Cross section of an AlInAs/GaInAs HBT.



$$\alpha(\omega) = \frac{\alpha_o e^{-j\omega\tau_c}}{1 + j\omega\tau_b}\left(\frac{\sin(\omega\tau_c)}{\omega\tau_c}\right)$$

$R_{b'b1}$=35 Ω	$C_{be(depl)}$=124 fF
$R_{b'b2}$=15 Ω	C_{cb1}=7 fF
R_{ex}= 9.5 Ω	C_{cb2}=23 fF
R_e=6.6 Ω	α_o=0.98
R_{cb}=25 kΩ	τ_b=0.96 ps
R_e=NkT/qI$_E$; N=1.35	τ_c=0.36 ps

Fig. 2. Extracted equivalent circuit of the 2-μm×5-μm emitter HBT.

doped at $10^{20}/\text{cm}^3$, a 5-nm undoped GaInAs spacer layer, a 180-nm-thick AlInAs emitter N doped at $8\times 10^{17}/\text{cm}^3$, and two highly doped $10^{19}/\text{cm}^3$ layers of AlInAs and GaInAs to reduce emitter contact resistance.

The triple-mesa device structure is shown in Fig. 1. The device employs Ti/Pt/Au contacts. The base metal was self-aligned to the emitter stripe by using the undercut of the emitter contact achieved through wet chemical etching of the emitter to access the base layer. The etch to the base layer was nonselective. Evaporated SiO_x and polyimide were used to planarize the structure to the top of the emitter contact.

Fitting measured 45-MHz to 26.5-GHz device S parameters at $V_{CE} = 1.3$ V and $I_C = 7.5$ mA, the device small-signal model of Fig. 2 is derived. At this bias point, f_τ and $f_{\max}$ are 80 and 65 GHz, and peak values are 90 and 70 GHz, respectively [5].

III. Circuit Design

The common-emitter, Darlington, and cascode feedback amplifier configurations were investigated. In silicon technology [1], with $f_{\max}$ substantially larger than f_τ, the Darlington stage attains larger bandwidth than the common emitter. In current AlInAs/GaInAs technology, $R_{b'b}$ and C_{bc} are more significant parasitics, and the cascode stage becomes advantageous.

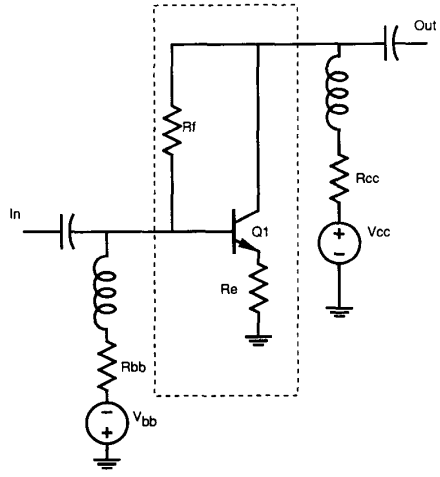


Fig. 3. Common-emitter feedback amplifier.

A. Common-Emitter Feedback Amplifier

In the common-emitter configuration (Fig. 3), in order to obtain a desired (negative) voltage gain A and input and output impedances matched to Z_O (usually 50 Ω), the required total emitter circuit resistance is $1/g_{m,\text{extrinsic}} = (R_e + R_{ex} + NkT/qI_c) = Z_o/(1-A)$, and the required feedback resistor is $R_f = Z_o(1-A)$, where R_{ex} is the transistor parasitic emitter resistance. Using the Miller approximation, the bandwidth can be roughly estimated. The input pole is dominant, and has a time constant of approximately $\{R_{bb'} + Z_o/2\}\{(1-A)C_{cb} + 1/2\pi f_\tau(R_e + R_{ex} + NkT/qI_c)\}$; bandwidth decreases with gain. The base spreading resistance $R_{bb'}$ increases the node impedance at the intrinsic base, decreasing the bandwidth. Increasing the emitter stripe length decreases $R_{bb'}$ but increases C_{cb}, with constant collector–base time constant $\tau_{\text{collector}} = C_{cb}R_{bb'}$. An optimum emitter stripe length is found which maximizes the bandwidth. With the transistor area selected, the collector current is selected to maximize f_τ, and the external emitter resistance R_e is chosen to obtain the correct extrinsic transconductance $g_{m,\text{extrinsic}}$. Circuit optimization using Touchstone® yielded circuit parameters reasonably consistent with this elementary analysis. In the resulting design, $Q1$ is a 2×10-μm emitter device biased at $I_c = 17$ mA, $R_e = 5$ Ω, and $R_f = 208$ Ω, the amplifier output is biased at 2 V, and 9.3-dB gain and 14.4-GHz bandwidth are predicted.

B. Darlington Feedback Amplifier

The Darlington configuration [1], [2] (Fig. 4) increases the stage bandwidth by providing a low-impedance drive to the (capacitive) input of the common-emitter device ($Q2$). If the collector–base junction of $Q1$ remains connected between amplifier input and output (as in Fig. 4),

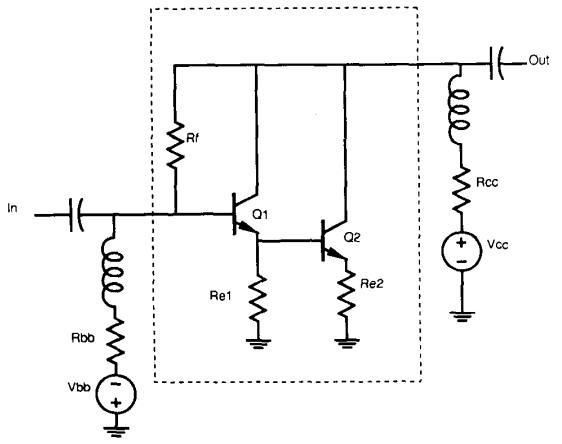


Fig. 4. Darlington feedback amplifier.

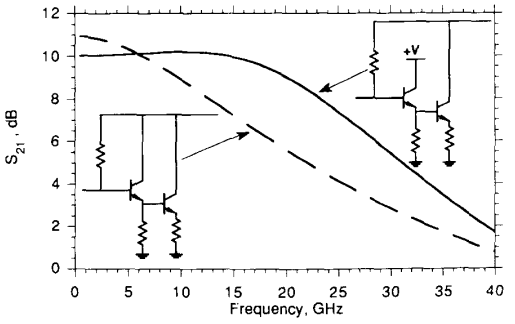


Fig. 5. Simulated gain (S_{21}) of Darlington stages with and without an independent $Q1$ collector supply. $Q1$ and $Q2$ are 2-μm×10-μm devices with $I_c = 16$ mA, $R_f = 208\ \Omega$, and $R_{e1} = 62\ \Omega$. With the $Q1$ collector tied to the amplifier output, Miller effect degrades the bandwidth from 26 to 14 GHz, and the low-frequency gain is increased slightly due to the $Q1$ collector signal current.

Miller multiplication of the $Q1$ collector–base capacitance will still contribute to the amplifier input capacitance.

Again, bandwidth is optimized by varying the emitter stripe lengths of $Q1$ and $Q2$, while operating the devices at the peak f_τ collector current; decreasing the $Q1$ emitter stripe length to decrease C_{cb} will increase $R_{bb'}$. With large $Q1$ emitter length, Miller-multiplied C_{cb} will degrade amplifier bandwidth, while with small emitter length, large $R_{b'b}$ will increase the node impedance at the intrinsic base, again degrading bandwidth. If $R_{bb'}C_{cb}$ is comparable to the transistor forward transit time $\tau_b + \tau_c$, then the Miller-multiplied collector–base time constant severely degrades amplifier bandwidth. Touchstone simulations (Fig. 5) confirmed that the Darlington provides bandwidth (12 GHz) only comparable to the common emitter, unless the collector of $Q1$ is connected not to the amplifier output, but is biased by an independent bypassed supply. In this case, 26-GHz bandwidth is attained, but the monolithic circuit must then incorporate a low-impedance bias node for the collector of $Q1$. Because the on-wafer bypass capacitors necessary to ac ground the $Q1$ collector were not available in the fabrication process, the independent-collector-supply Darlington configuration could not be implemented.

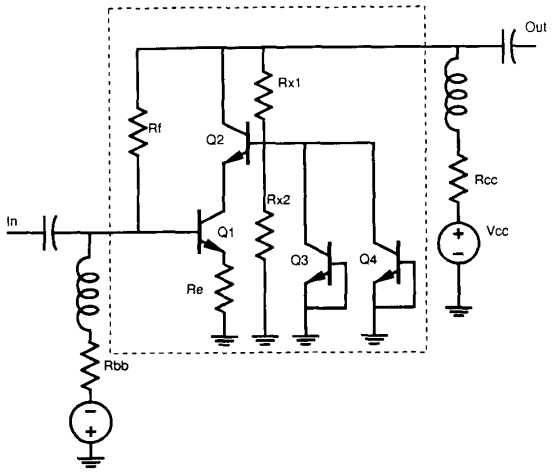


Fig. 6. Cascode feedback amplifier.

In silicon bipolar microwave amplifiers [1], f_{max} is generally substantially larger than f_τ, hence $R_{bb'}C_{cb}$ is substantially smaller than $\tau_b + \tau_c$. In this case, the Darlington configuration provides a large bandwidth improvement, even with collector of the emitter-follower stage connected to the amplifier output. In our process $f_{max} \approx f_\tau$, hence $R_{bb'}C_{cb}$ places more severe constraints on circuit performance.

C. The Cascode Configuration

The cascode configuration (Fig. 6) reduces Miller multiplication of C_{cb}, and hence provides a substantial bandwidth improvement if $R_{bb'}C_{cb}$ is a dominant parasitic. The transistors are operated at the current density corresponding to the peak f_τ, and R_e is then used to set the stage transconductance. As with the common-emitter stage, larger devices have larger collector–base capacitance, while smaller devices have larger base series resistance; stage bandwidth varies as device size is varied, and an optimum device size is found.

The simple cascode (Fig. 6) will provide increased bandwidth (30 GHz simulated) only if the base of $Q2$ is ac grounded with low impedance over the amplifier bandwidth. Circuit simulations (Fig. 7) indicate that a minimum base bypass capacitance of approximately 1 pF is required to attain the full potential bandwidth of the cascode stage. At the time of design, MIM capacitors were not available in the process. Instead, collector–base junctions of an array of large transistors were used for cascode base bypassing, providing approximately 0.35 pF.

To attain wide bandwidth without use of large-value on-wafer bypass capacitors, an emitter-follower bias-source buffer stage $Q3$ is added to the cascode feedback amplifier (Fig. 8). The emitter-follower bias stage in turn

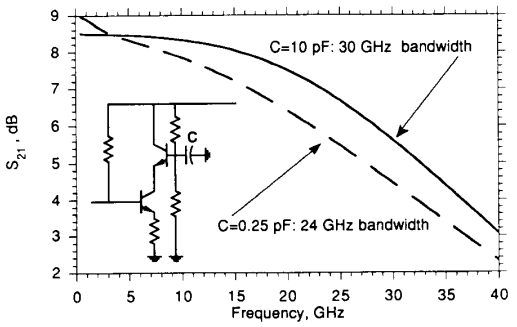


Fig. 7. Circuit simulations: effect of cascode base bypass capacitance on the amplifier gain bandwidth.

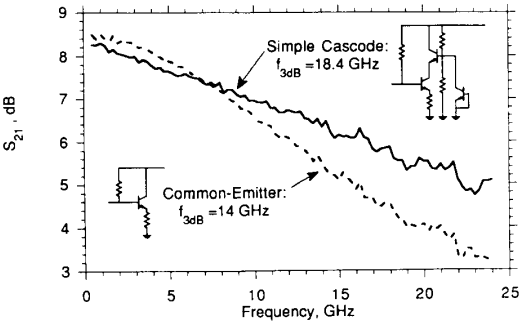


Fig. 10. Measured forward gain S_{21} of the common-emitter and simple cascode feedback amplifiers.

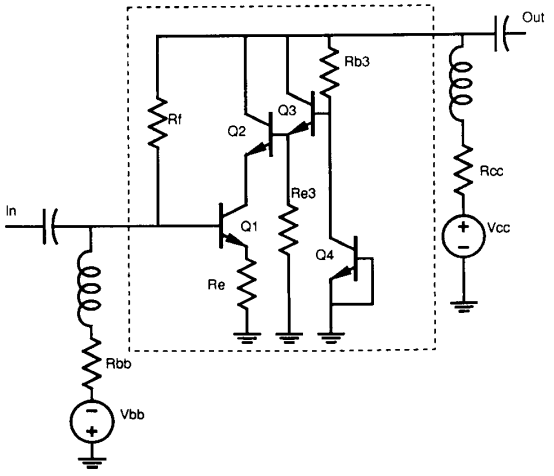


Fig. 8. Active-bias cascode feedback amplifier.

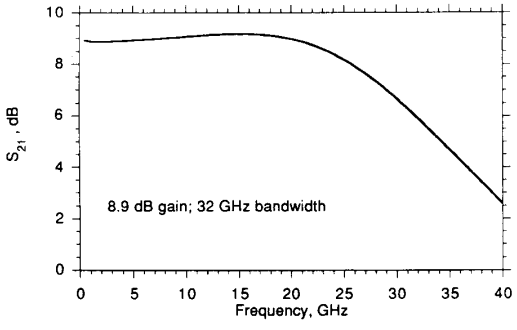


Fig. 9. Simulated forward gain (S_{21}) of the active-bias cascode feedback amplifier.

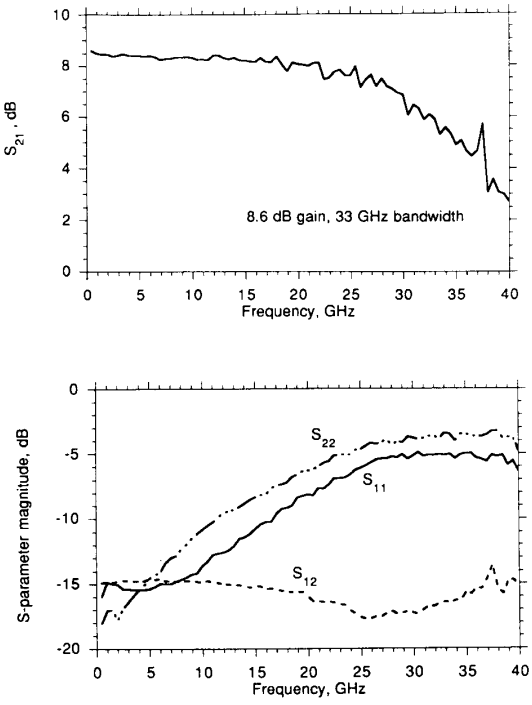


Fig. 11. Measured forward gain S_{21}, reverse isolation S_{12}, input return loss S_{11}, and output return loss S_{22} of the active-bias cascode feedback amplifier.

has its input ac grounded by the ≈ 0.35-pF collector–base junction capacitance of $Q4$. Design values include: 2×10-μm emitter areas for $Q1$ and $Q2$, a 2×5-μm $Q3$ emitter area, $R_f = 208\ \Omega$, $R_e = 5\ \Omega$, $R_{e3} = 800\ \Omega$, and $R_{b3} = 800\ \Omega$. The amplifier output is biased at 4 V, and $Q1$ and $Q2$ operate at 16-mA emitter current. Simulations (Fig. 9) then predict 8.9-dB gain to 32 GHz.

IV. Results

The common-emitter, simple cascode, and active-bias cascode amplifiers were characterized by dc to 40-GHz on-wafer network analysis with microwave wafer probes. The common-emitter feedback amp exhibited 8.6-dB gain (S_{21}), with a 3-dB bandwidth of 14.1 GHz (Fig. 10). As shown in Fig. 10, the simple cascode exhibited only a marginally larger 18.4-GHz bandwidth.

The measured S parameters of the active-biased cascode are shown in Fig. 11. S_{21} exhibits a low-frequency gain of 8.6 dB, and a bandwidth at the -3-dB point of 33 GHz. Reverse isolation is greater than -14 dB at all frequencies, while the input and output return losses

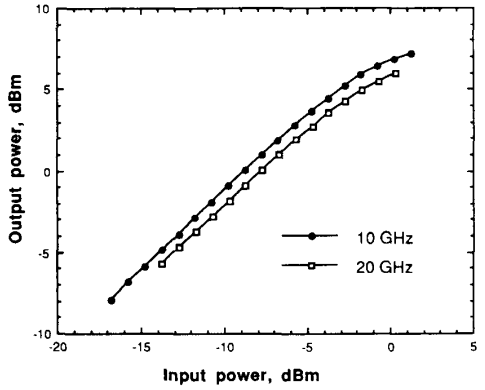


Fig. 12. Measured gain compression characteristics of the active-bias cascode amplifier.

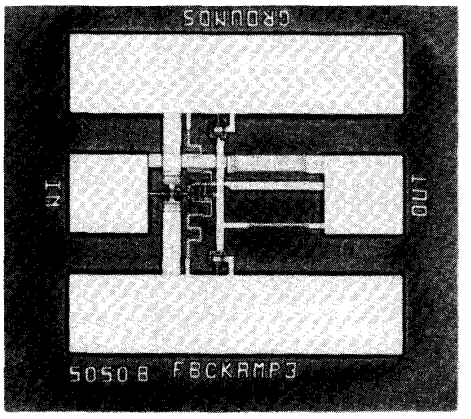


Fig. 13. Photomicrograph of the active-bias cascode feedback amplifier. For scale, the input and output bond pads are 100 μm $\times$ 100 μm.

degrade progressively with frequency, reaching -5 and -3.7 dB at 33 GHz, respectively. The degradation of S_{11} and S_{22} with frequency limits the usable amplifier bandwidth to approximately 16 GHz. The bandwidth over which S_{11} and S_{22} are better than -10 dB can be greatly extended through addition of small inductive compensation elements in series with the feedback resistor and at the amplifier input. Because the transistor parameters were evolving at the time of circuit design, matching elements were not incorporated. The maximum output power is primarily limited by saturation in $Q3$, and is approximately 5 dBm at the 1-dB gain compression point (Fig. 12).

V. Summary

Monolithic feedback amplifiers were developed using AlInAs/GaInAs HBT technology. Because of the significant collector–base feedback time constant, the cascode configuration provides a large improvement in amplifier bandwidth, but a low-impedance bias node must be provided for the common-base transistor. An active bias network was thus used; cascode and Darlington designs using MIM bypass and coupling capacitors are currently in process.

The resulting 33-GHz amplifier bandwidth is competitive with AlGaAs/GaAs MODFET traveling-wave amplifiers [7], but with a much smaller die area (excluding the bond pads necessary to interface with microwave wafer probes) of 200 μm $\times$ 225 μm (Fig. 13). The AlInAs/GaInAs monolithic feedback amplifiers are extremely small, wide-band gain blocks suitable for use as subcomponents in complex MIMIC's for monolithically integrated millimeter-wave systems.

References

[1] I. Kipnis, J. F. Kukielka, J. Wholey, and C. P. Snapp, "Silicon bipolar fixed and variable gain amplifier MMICs for microwave and lightwave applications up to 6 GHz," in *IEEE MTT-S Int. Microwave Symp. Dig.* (Long Beach, CA), June 1989, pp. 109–112.

[2] K. W. Kobayashi *et al.*, "GaAs heterojunction bipolar transistor MMIC DC-10 GHz direct-coupled feedback amplifier," in *1989 GaAs IC Symp. Tech. Dig.* (San Diego, CA), pp. 87–90.

[3] J. F. Jensen *et al.*, "AlInAs/GaInAs HBT IC technology," *IEEE J. Solid-State Circuits*, vol. 26, no. 3, pp. 415–421, Mar. 1991.

[4] R. N. Nottenberg *et al.*, "In-P-based heterostructure bipolar transistors," in *1989 GaAs IC Symp. Tech. Dig.* (San Diego, CA), pp. 135–138.

[5] M. Rodwell *et al.*, "33 GHz monolithic cascode InGaAs/InAlAs heterojunction bipolar transistor feedback amplifier," presented at the 1990 IEEE Bipolar Circuits and Technology Meeting, Minneapolis, MN, Sept. 17–18, 1990.

[6] P. M. Asbeck *et al.*, "GaAlAs/GaAs heterojunction bipolar transistors: Issues and prospects for application," *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2032–2042, Oct. 1989.

[7] C. Yuen *et al.*, "A monolithic 3 to 40 GHz HEMT distributed amplifier," presented at the 1988 GaAs IC Symp., Nashville, TN, Nov. 6–9, 1988.