Extremely High g_m > 2.2 S/mm and f_T > 550 GHz in 30-nm Enhancement-Mode InP-HEMTs with Pt/Mo/Ti/Pt/Au Buried Gate

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InP-based high electron mobility transistors (HEMTs) are attractive devices for high-speed, low-noise, low power amplifier applications. These devices have performance advantages due to their higher low-field electron mobility, their higher peak electron velocity, and their higher sheet carrier density. Indeed, high performance InP-HEMTs with a cutoff frequencies (f_T) of over 550 GHz have been demonstrated [1,2]. These performances were achieved only in depletion-mode (D-mode) HEMTs. An enhancement-mode (E-mode) HEMT is strongly required since it eliminates the need of negative voltage supply, and it simplifies circuit configuration by integrating with D-mode HEMTs. However, E-mode HEMTs with a comparable high-speed performance to D-mode HEMTs have not been reported. This is partly because of a higher sheet resistance of uncapped recessed region designed for E-mode operation, which results in a high access resistance that degrades extrinsic transconductance (g_m). Moreover, HEMTs with a sub-50-nm gate length experience a severe short-channel effect which further pushes the threshold voltage (V_{th}) to the negative direction, making it difficult to operate in E-mode. In this paper, we report on 30-nm E-mode InP-HEMTs with an extremely high g_m of over 2.2 S/mm and an ft of over 550 GHz using a Pt/Mo/Ti/Pt/Au buried gate technology.

Figure 1 illustrates a cross-section of a fabricated InP-HEMT. The HEMT epitaxial structure consists of an InAlAs buffer, pseudomorphic $In_{0.7}Ga_{0.3}As$ channel, an InAlAs spacer layer, Si planar doping, an InAlAs barrier, an InP etch-stopper, and n^{++}-InGaAs/InAlAs cap layers. A 30-nm T-gate was formed by a conventional lift-off technique using a tri-layer electron beam lithography. Pt(3 nm or 9 nm)/Mo/Ti/Pt/Au gate metal was used for E-mode HEMTs while a conventional Ti/Pt/Au gate was used for D-mode HEMTs. Pt was used to form a buried gate by annealing and Mo was used as a diffusion barrier. Figure 2 shows V_{th} of 30-nm E-mode InP-HEMTs before and after annealing at 210°C and 250°C for 1 hour. It is notable that there is a significant difference in V_{th} shift between 3 and 9-nm samples, and V_{th} of 3-nm sample saturates at 250°C. This result indicates Mo acts as an effective diffusion barrier of Pt and diffusion depth can be controlled by the thickness of Pt.

Figure 3 shows output characteristics of a 30-nm E-mode HEMT with a 9-nm Pt gate and a 30-nm D-mode HEMT with a Ti gate fabricated on the same wafer. Both devices were annealed at 250°C for 1 hour. The devices show good pinch-off characteristics and very low on resistances (R_{on}) of 0.38 ohm·mm (E-mode) and 0.36 ohm·mm (D-mode). Figure 4 shows transfer charactersitics of the E-mode HEMT. A V_{th} of +0.18 V at a drain-source voltage (V_{ds}) of 0.6 V and a peak g_m of 2.22 S/mm were obtained. This g_m value is higher than that (1.44 S/mm) of the D-mode HEMT by 54% and is the highest value ever reported for any field effect transistors (FETs). Good Schottky characteristics were maintained even after 250°C annealing for 1 hour. Figure 5 plots RF gain of the 30-nm E-mode HEMT biased at a V_{ds} of 0.6 V and a gate-source voltage (V_{gs}) of 0.4 V, exhibiting an extremely high f_T of 550 GHz and an f_{max} of 346 GHz. This f_T is the highest value ever reported for any E-mode InP-HEMTs and even comparable to the fastest D-mode HEMTs [1]. f_T and f_{max} values measured at various bias conditions are also plotted in Fig. 6. It should be noted that f_T exceeds 200 GHz only at a V_{ds} as low as 0.1 V, and 350 GHz at 0.2 V, which is suitable for very low-power applications. These results demonstrate the potential of the Pt/Mo/Ti/Pt/Au buried gate technology to enable further lateral and vertical scaling of InP-HEMTs.

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[1] Y. Yamashita *et al.*, IEEE Electron Device Lett., 23, 573 (2002).
[2] K. Shinohara *et al.*, IEEE Electron Device Lett., 25, 241 (2004).

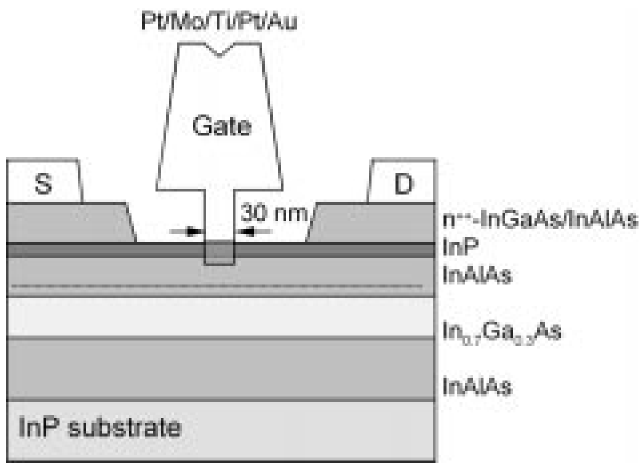

Fig. 1. Schematic illustration of InP-HEMT with a Pt/Mo/Ti/Pt/Au buried gate.

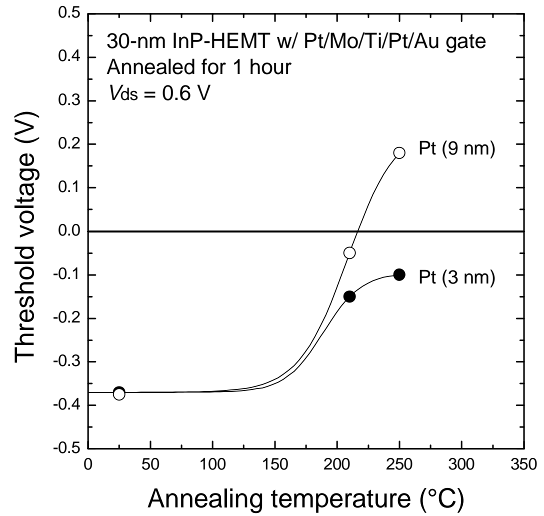

Fig. 2. Threshold voltage of 30-nm InP-HEMTs with Pt/Mo/Ti/Pt/Au gate before/after annealing.

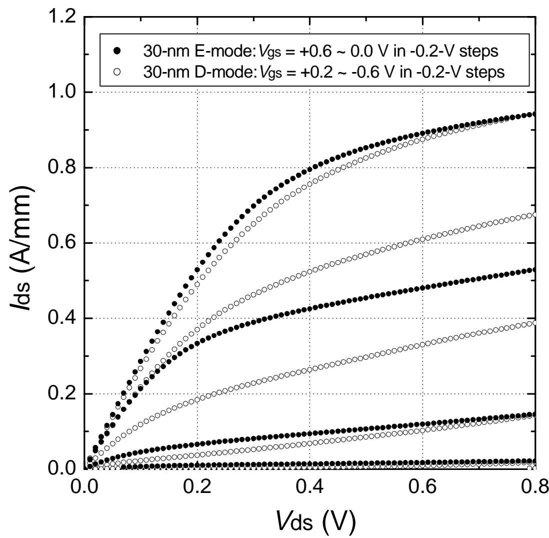

Fig. 3. Output characteristics of 30-nm E/D-mode HEMTs.

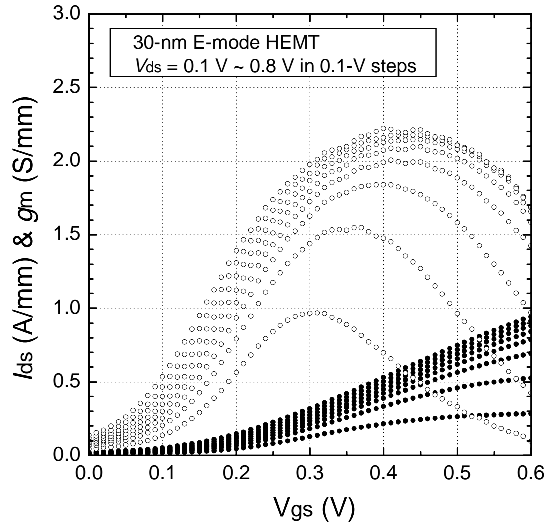

Fig. 4. Transfer characteristics of 30-nm E-mode HEMT.

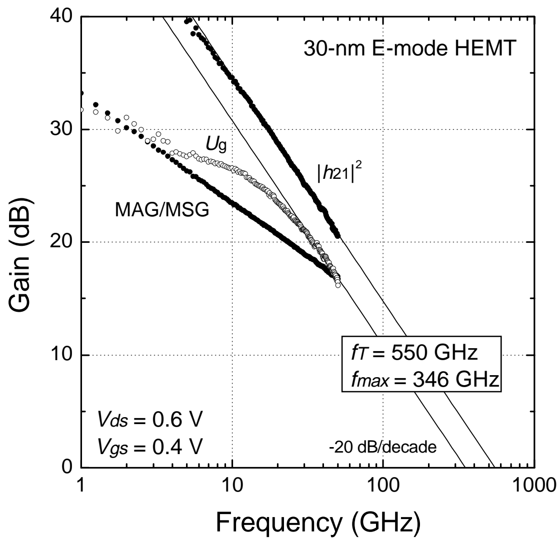

Fig. 5. RF gain for 30-nm E-mode HEMT.

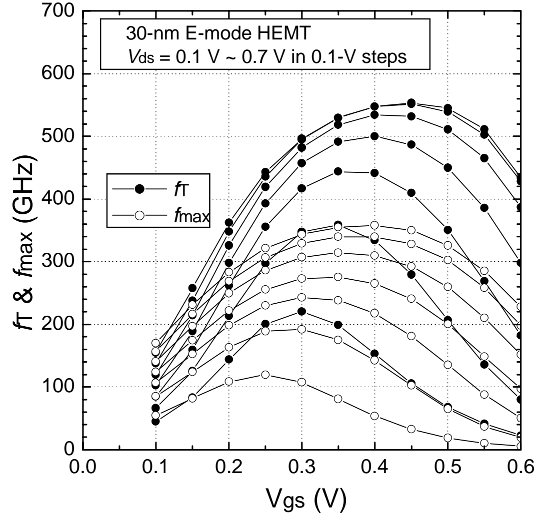

Fig. 6. ft and fmax at various bias conditions of 30-nm E-mode HEMT.