mm-Wave IC Design: The Transition from III-V to CMOS Circuit Techniques

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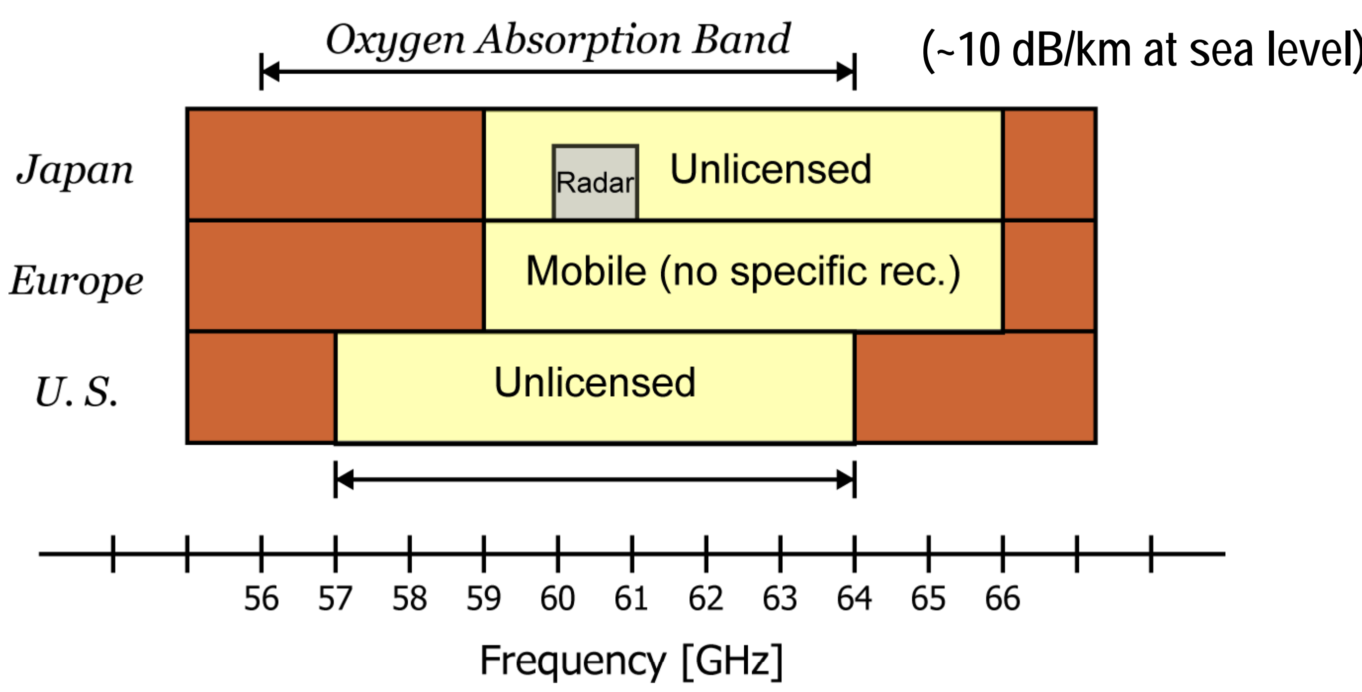
Outline

- Background
  - Emerging mm-wave applications
  - Open design issues for mm-Wave CMOS
- CMOS for mm-wave design
  - Optimizing CMOS device performance – layout & bias
  - On-chip inductors in CMOS
  - Cell-based device modeling and design methodology
  - State of the art CMOS mm-Wave design examples
- mm-Wave design techniques
  - Device characterization issues
  - Unconditionally stable, gain-matched amplifier design procedure
  - Tuned amplifier, power amplifier design examples
  - On-chip transmission line design
- Summary
- References

Yue & Rodwell, IEEE CSIC Short Course, Nov. 2006

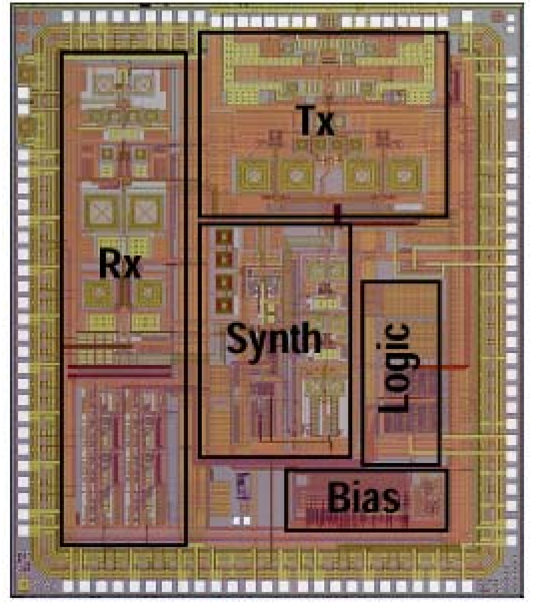
Emerging mm-Wave Wireless Applications



- Unlicensed 60-GHz band for Gbit wireless link:
  - Outdoor, point-to-point wireless link
  - Wireless High-Definition Multimedia Interface (HDMI)
- Licensed point-to-point wireless link in E-band (71-76, 81-86 GHz, and 92-95 GHz)
- Vehicular radar at 76-77 GHz
- 94-GHz band for high-resolution imaging

<u>Questions:</u>
Can we leverage scaled CMOS to produce more cost-effective products and enable new markets?

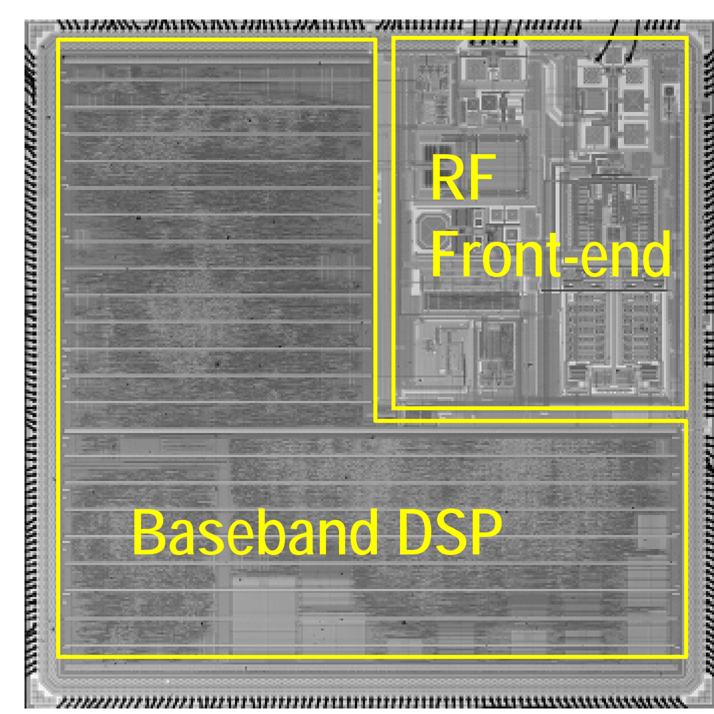
Recent Evolution for CMOS RF



(D. Su, ***et al. ISSCC 2002***.)

- 0.25-µm CMOS
- 5-GHz RF transceiver

Lower power, cost and size



(S. Mehta, ***et al. ISSCC 2005***.)

- 0.18-µm CMOS
- RF + baseband DSP

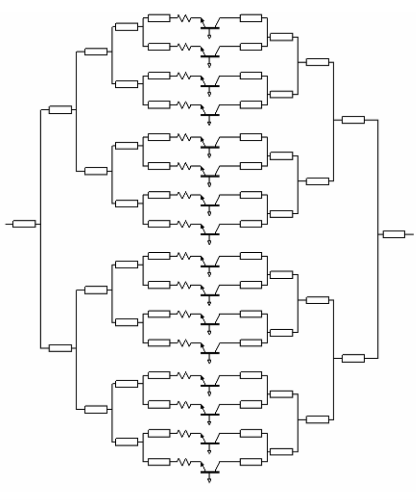
But difficult to migrate below 0.18µm even for RF SoC...

State of the Art mm-Wave IC: 330 GHz 16-Finger Power Amp

designs in progress*: Michael Jones*

device: 5 V, 650 GHz f_{max} InP DHBT

wiring: thin film microstrip with 2 um BCB



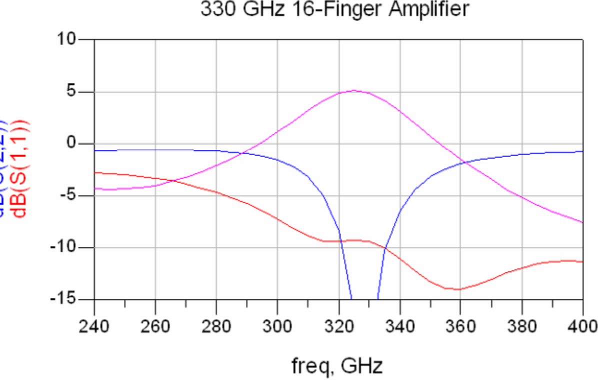
Challenges:

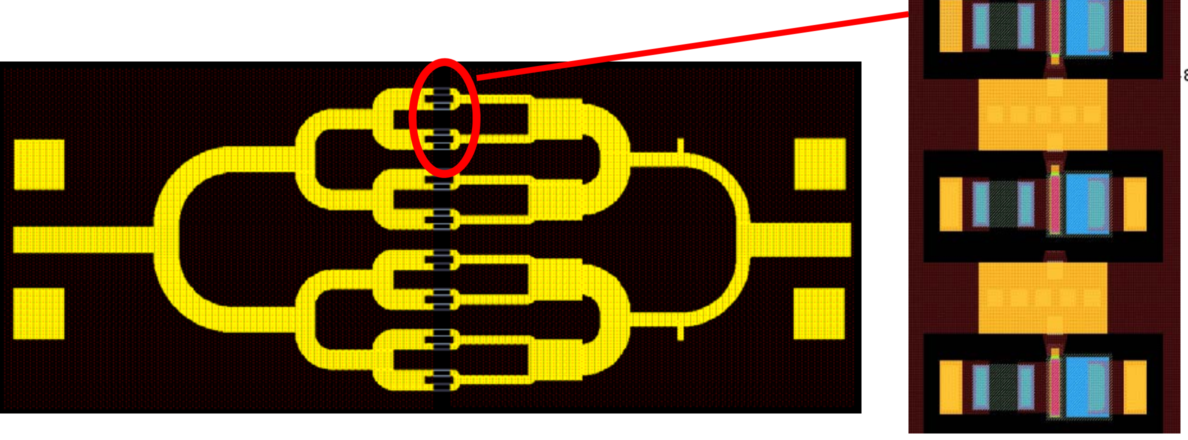
line losses are very high

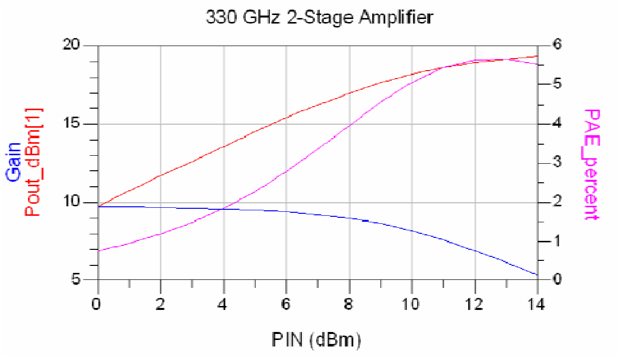
lines > 60 Ω are not feasible → increases Q of output tuning

lines of required impedance are narrow → limits on DC current

small unmodeled parasitics will de-tune design
....must maintain microstrip environment to device vias
with negligible lengths of unmodeled random interconnects







Open Design Issues

- RF CMOS design are by and large lumped circuits
- mm-Wave design are traditionally distributed circuits
- How will mm-Wave CMOS be designed?
  - Assuming that we will integrate an entire transceiver, should each block be impedance-matched?
  - Do we need new design flow / methodology?
  - Should all interconnect be modeled as T-line and be impedance-controlled?
  - Do we need a well-controlled global ground (plane)?
- How to optimize CMOS device performance?

CMOS Device Parameter Scaling Trend

Process	0.25 μm ('98)	0.18 μm ('00)	0.13 μm ('02)	90 nm ('04)
V_{dd} (V)	2.5 (1x)	1.8 (0.7x)	1.2 (0.5x)	1.0 (0.4x)
I_{dsat} (μA/μm)	600 (1x)	600 (1x)	550 (1x)	850 (1.4x)
I_{off} (nA/μm)	0.01 (1x)	0.02 (2x)	0.32 (32x)	7 (700x)
I_{gate} (nA/μm)	2.5e-5 (1x)	1.8e-3 (100x)	0.65 (5e4)	6.3 (70000x)
I_{on}/I_{off} (10e6)	60 (1x)	30 (0.5x)	1.7 (0.03x)	0.12 (0.002x)
g_m (mS/μm)	0.3 (1x)	0.4 (1.3x)	0.6 (2x)	1.0 (3.3x)
g_{ds} (μS/μm)	7.7 (1x)	15 (2x)	42 (5.4x)	100 (13x)
g_m / g_{ds}	39 (1x)	27 (0.7x)	14 (0.36x)	10 (0.26x)
f_T (GHz)	30 (1x)	60 (2x)	80 (2.7x)	140 (4.7x)
Delay (ps/gate)	45 (1x)	30 (0.7x)	15 (0.3x)	11 (0.24x)
C_g (fF/gate)	0.47 (1x)	0.35 (0.7x)	0.25 (0.5x)	0.16 (0.34x)
C_j (fF/gate)	0.83 (1x)	0.80 (1x)	0.88 (1.1x)	0.66 (0.8x)

- **Positive**: f_T, f_{max}, F_{min}, I_{dsat}, g_m, C_g and C_j
- **Negative**: V_{dd} and g_{ds}

Challenges for RF/mm-Wave in 0.13-μm CMOS and Beyond

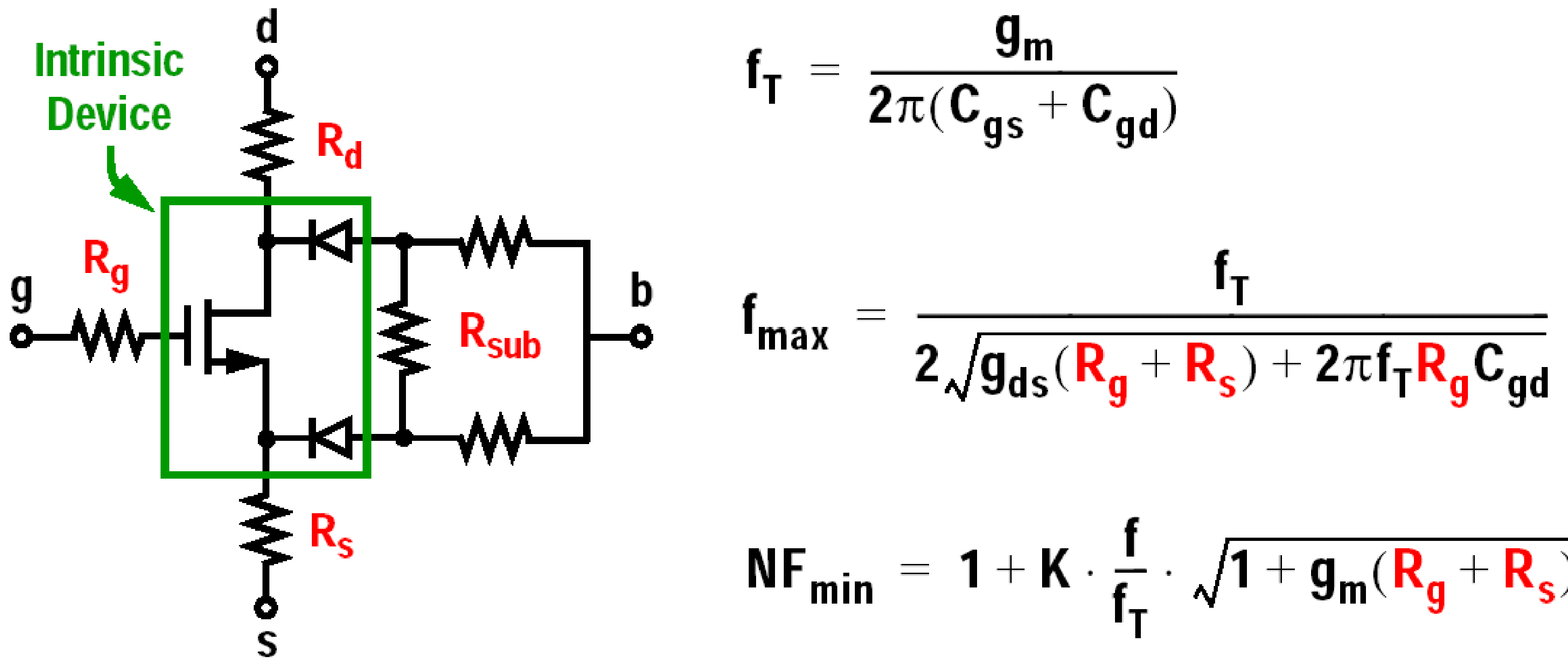
- High mask cost ($0.5M – $1M)
  - only makes sense if integration level increases, e.g. RF + large DSP, or mm-wave transceiver
- Lack of a streamline RF/mm-wave design flow
- Negative impact of technology scaling
  - Device
    - Process variations
    - Model uncertainty
    - Interconnect parasitic variations

    } Strongly depend on layout
  - Circuit
    - Low voltage headroom due to reduced Vdd

➔ Develop a parasitic-aware design methodology

➔ Explore low-voltage circuit techniques

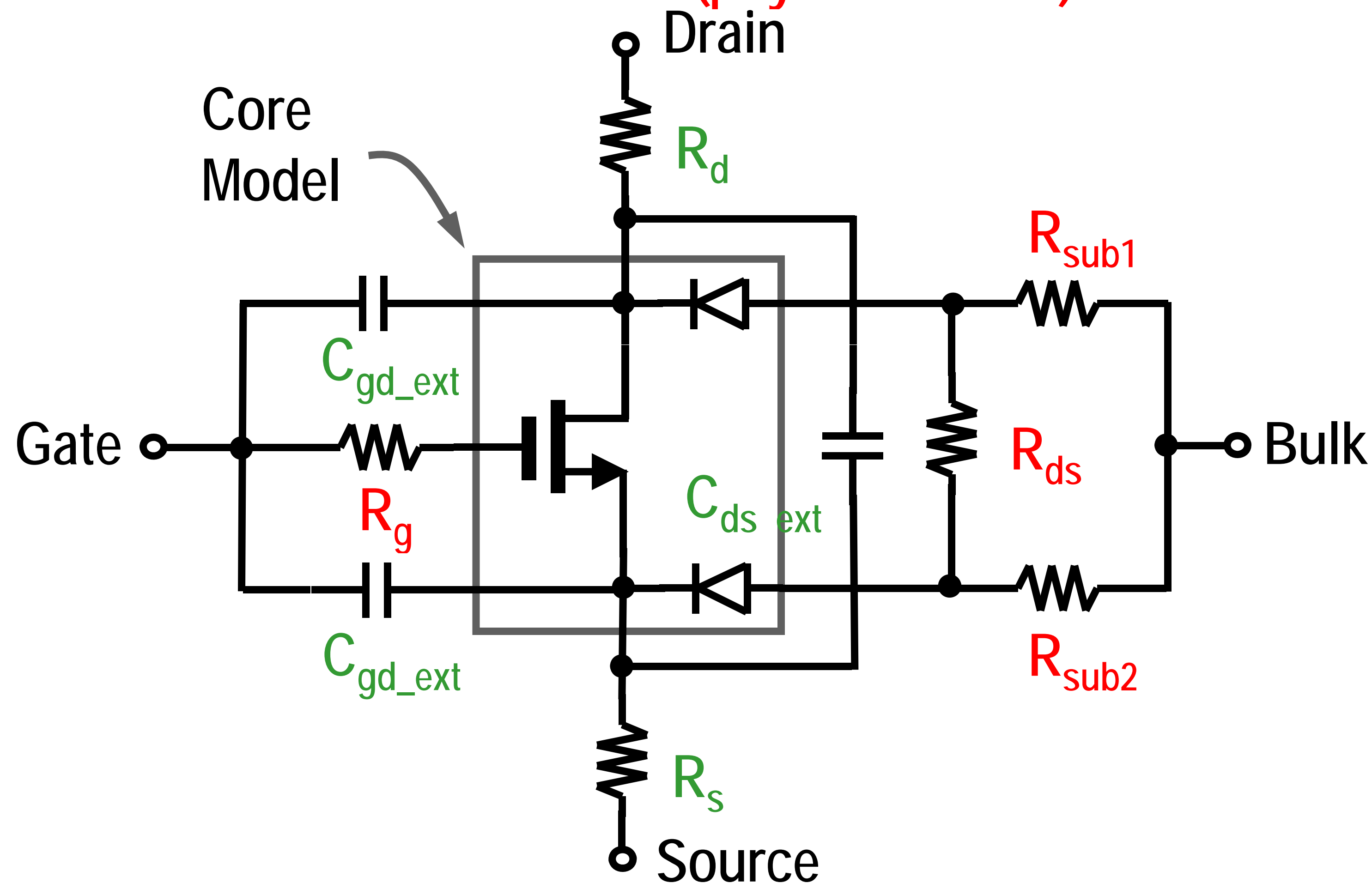
High Frequency Figures of Merit



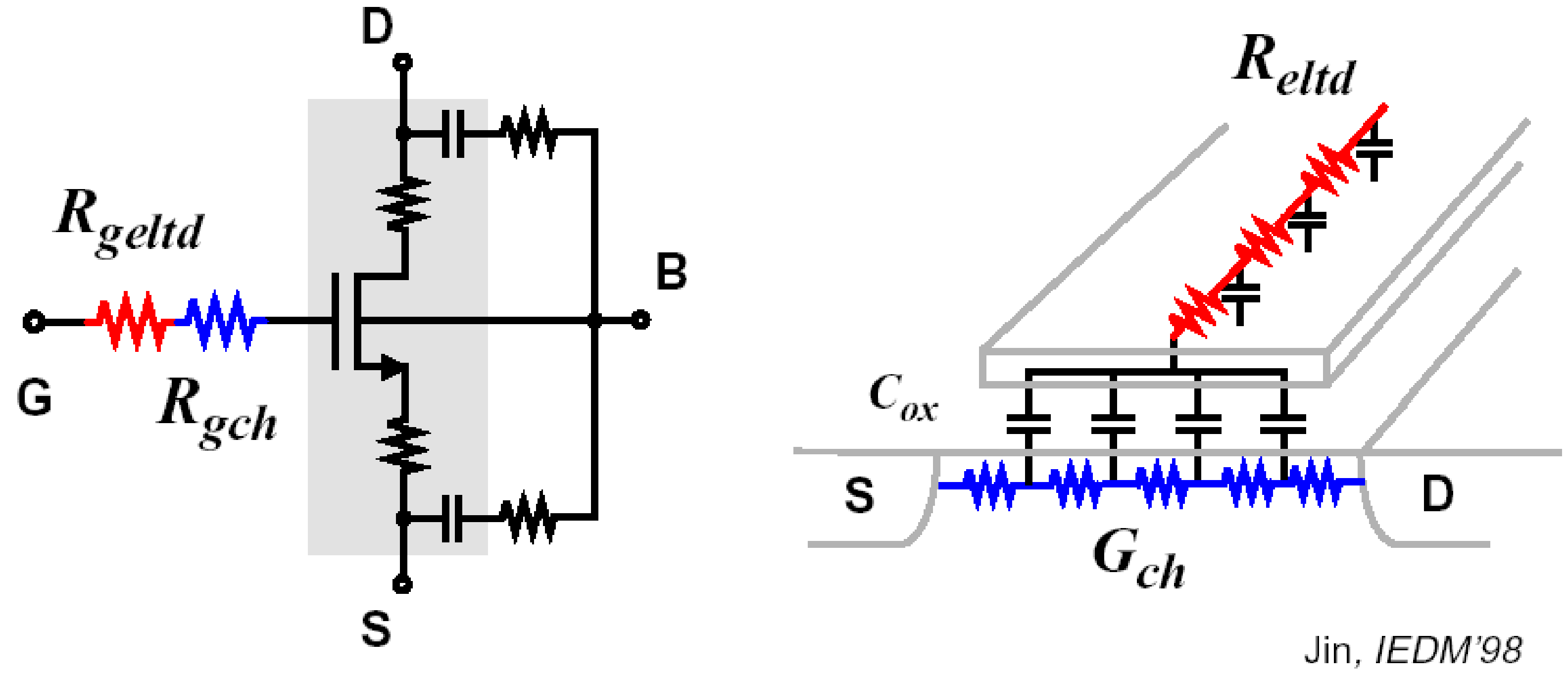
- Minimize R_g, R_s, and R_{sub} for better performance
- Layout and biasing are both critical

Complete Macro Model

- Core model (baseline BSIM model)
- Interconnect RC (3D EM field solver)
- Gate and substrate resistances (physical model)



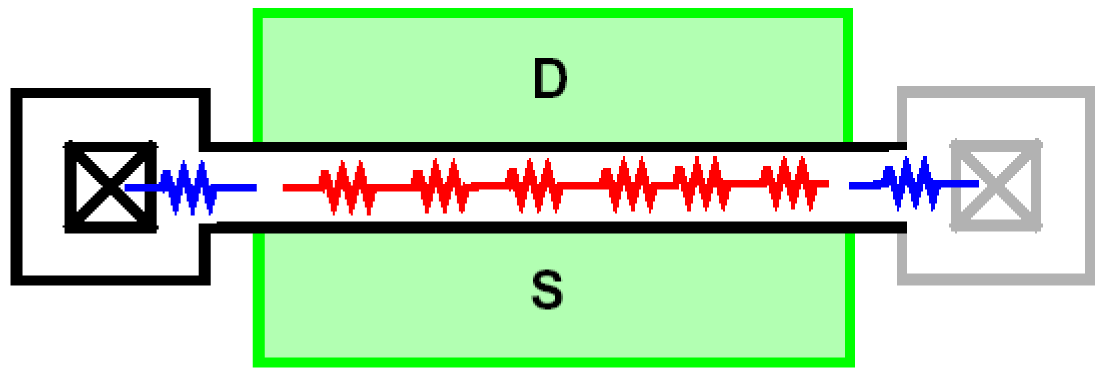
Gate Resistance Components



- R_{geltd}: distributed gate electrode resistance
- R_{gch}: channel induced gate resistance

Ref. 16

Gate Electrode Resistance

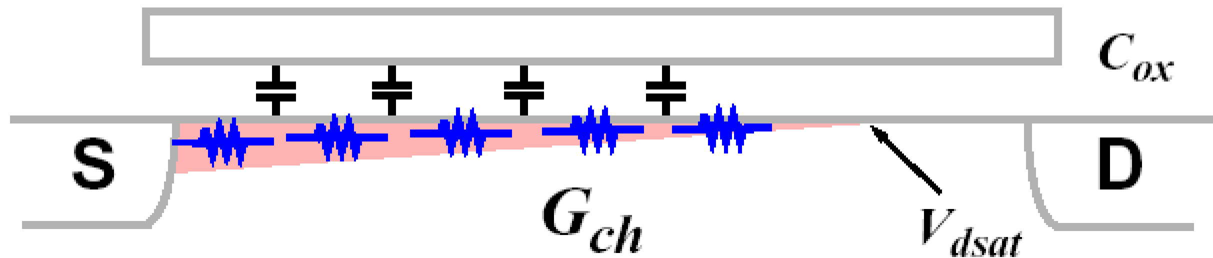


$$R_{geltd} = R_{eltd}\left(\alpha\frac{W}{L} + \beta\right) \qquad \alpha = \begin{cases} 1/3 & \text{one side connected} \\ 1/12 & \text{two sides connected} \end{cases}$$

- α models distributed effect of gate electrode
- β models external gate resistance

Ref. 16 & 18

Channel Conductance



Two components in G_{ch}: $G_{ch} = G_{st} + G_{ed}$

- **Static** channel conductance $\propto \frac{L}{W}$

$$G_{st} = \frac{1}{\int dR} = \frac{I_d}{\int dV} = \begin{cases} I_d / V_{dsat} & \text{in saturation} \\ I_d / V_{ds} & \text{in triode} \end{cases}$$

- **Excess-diffusion** conductance

$$G_{ed} = \eta \frac{kT}{q} \mu_{eff} C_{ox} \frac{W}{L} \qquad \eta \sim 1$$

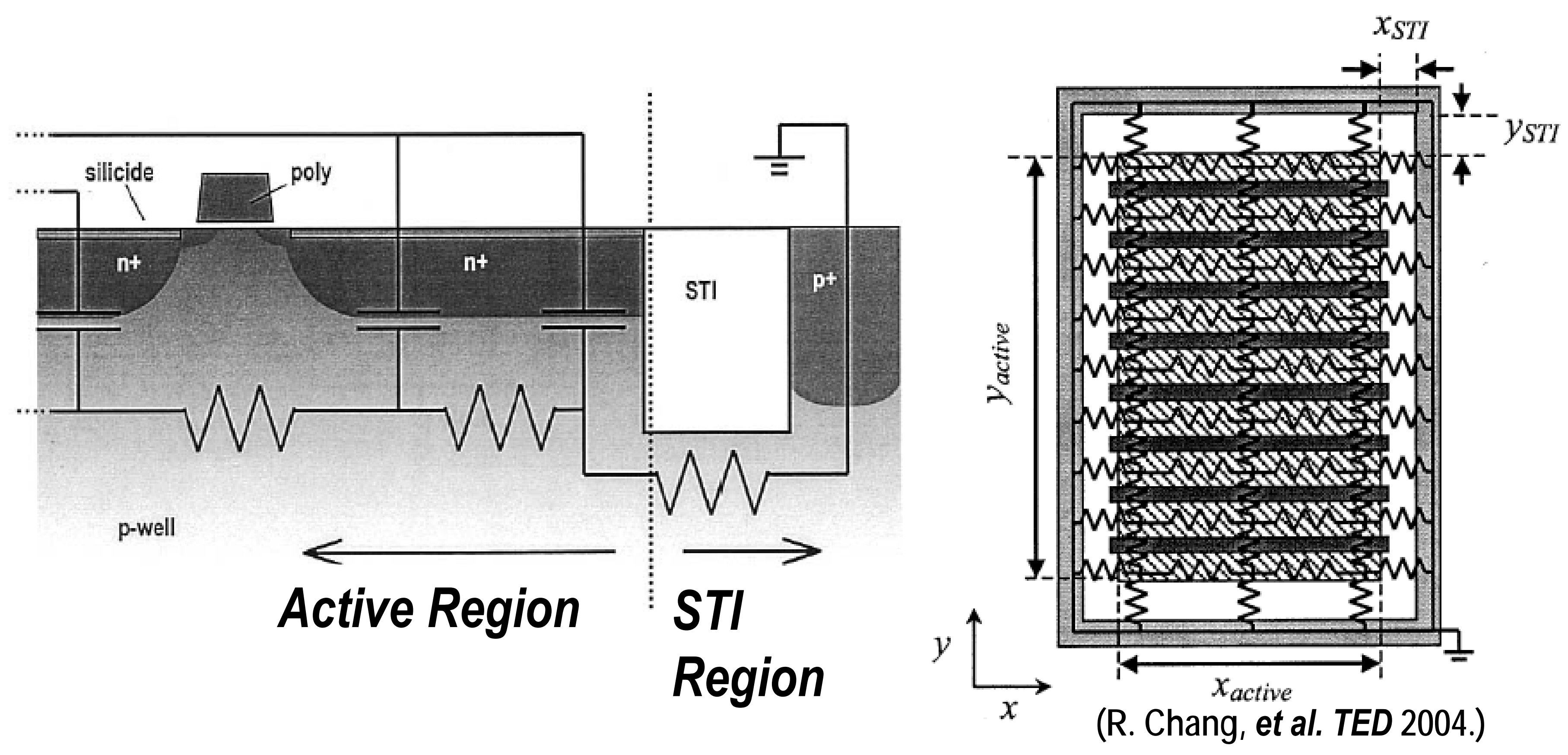
Ref. 16

(ac effect – channel charge distribution modulated by gate voltage, derived based on diffusion current)

Layout Guideline for Gate Resistance

- Multi-finger layout in RF MOSFET is common to minimize Rgate (at the expense of more parasitic capacitance)
- Typical finger width for 0.25um device is about 5 um whereas in 0.13um CMOS is 1.5 um
- Total gate width ranges from a few 10's of micron for LNA, mixer & VCO to a few millimeters for PA
- R_{eltd} (poly resistance) scales with $1/n^2$
- External portion of R_{geltd} (contact resistance) scale with 1/n
- R_{ch} is independent of n to the first order

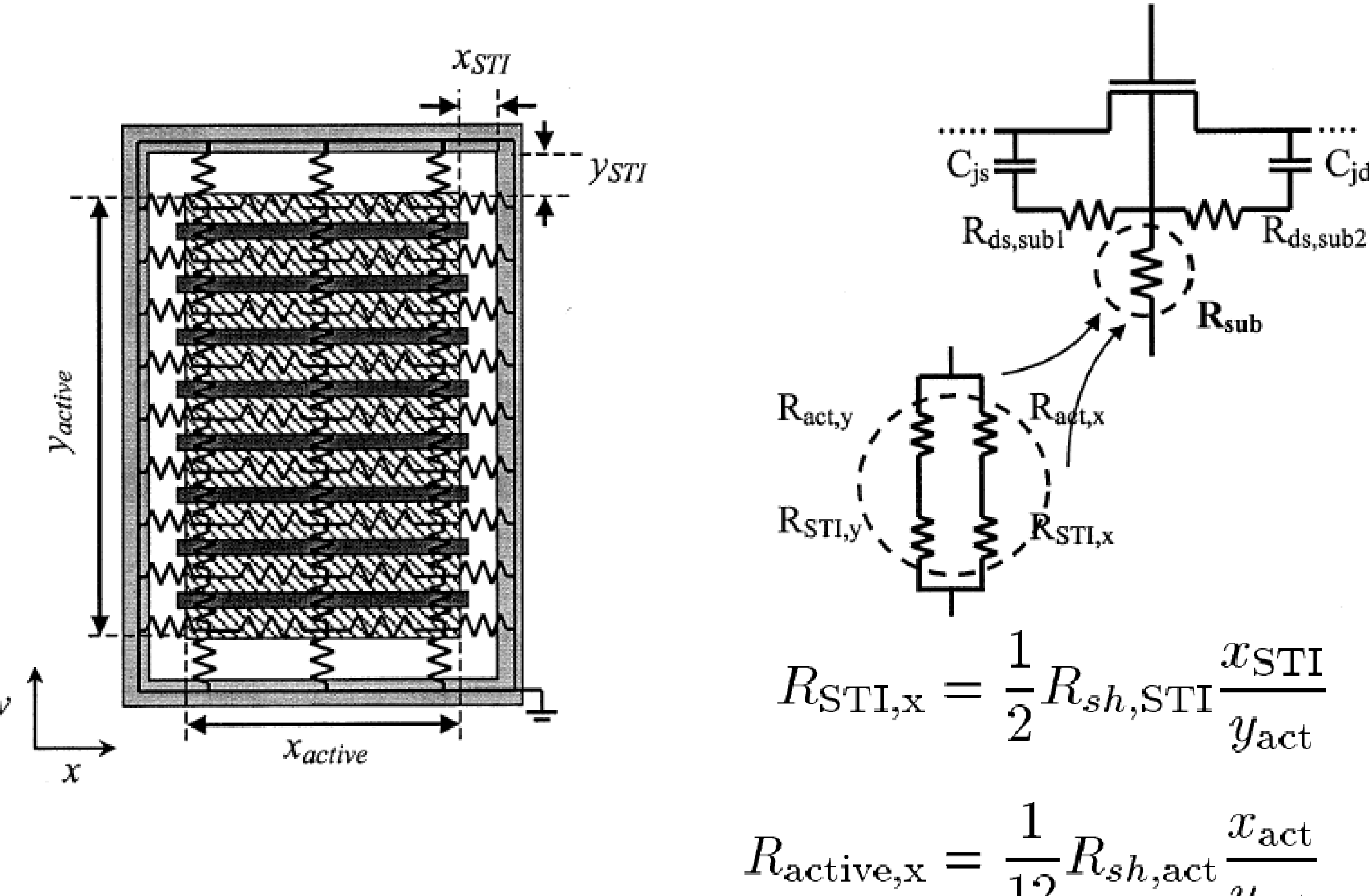
Substrate Resistance Model



(R. Chang, ***et al. TED*** 2004.)

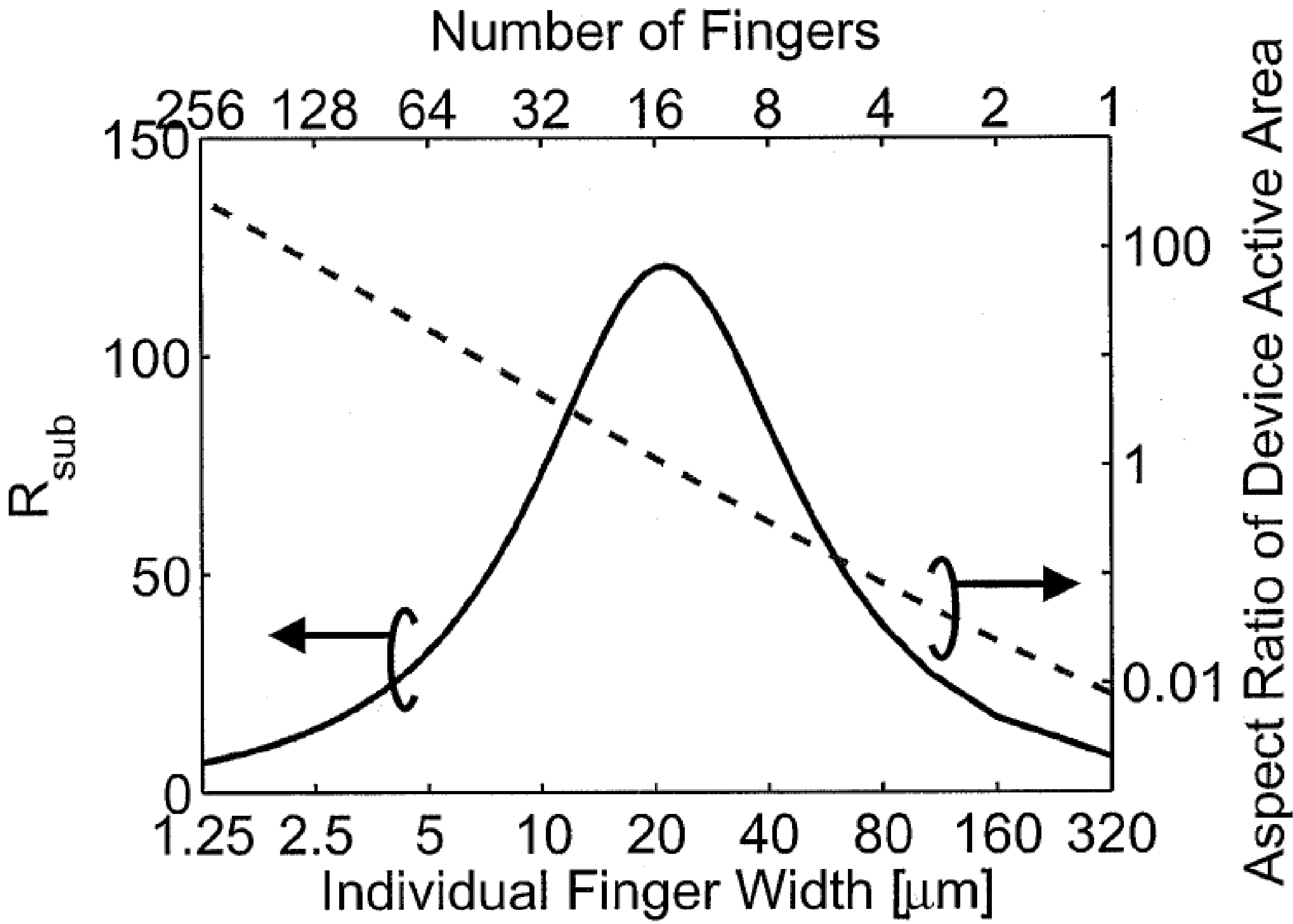
- Active and STI regions have different sheet resistances
- Resistances in x and y directions modeled as parallel resistors

Analytical Model of Substrate Resistance



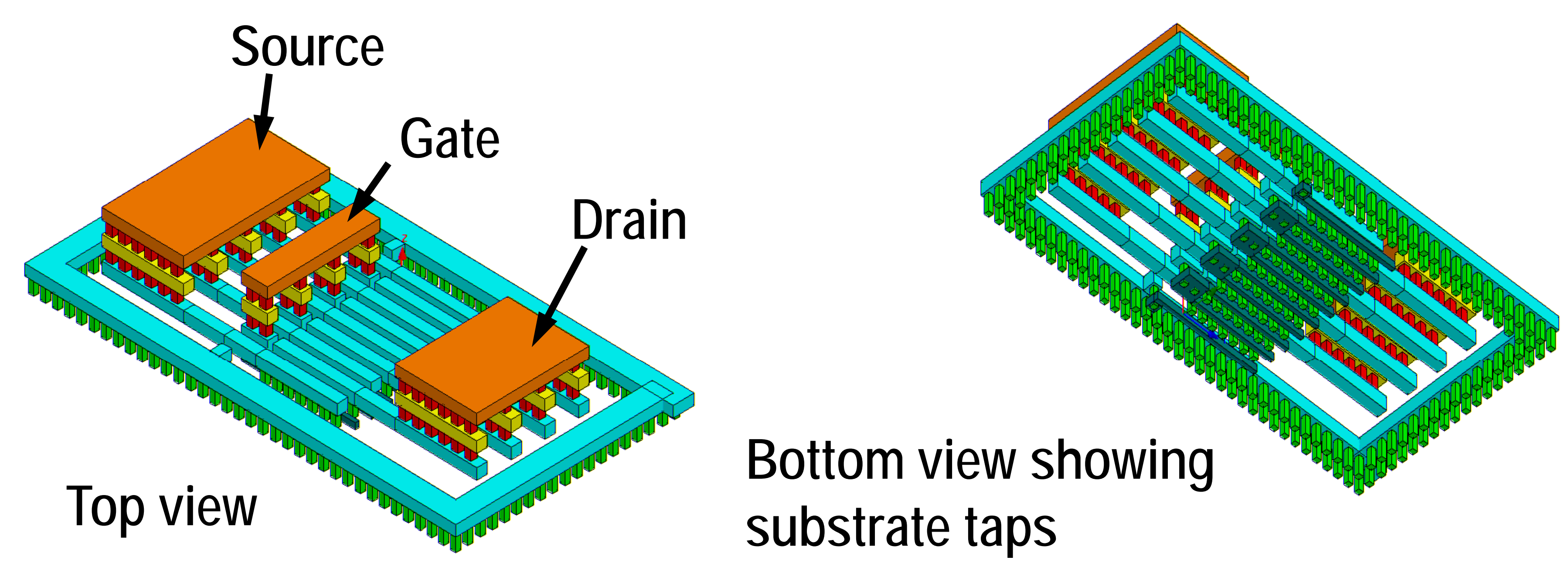
Ref. 17

Optimization of Substrate Resistance



Ref. 17

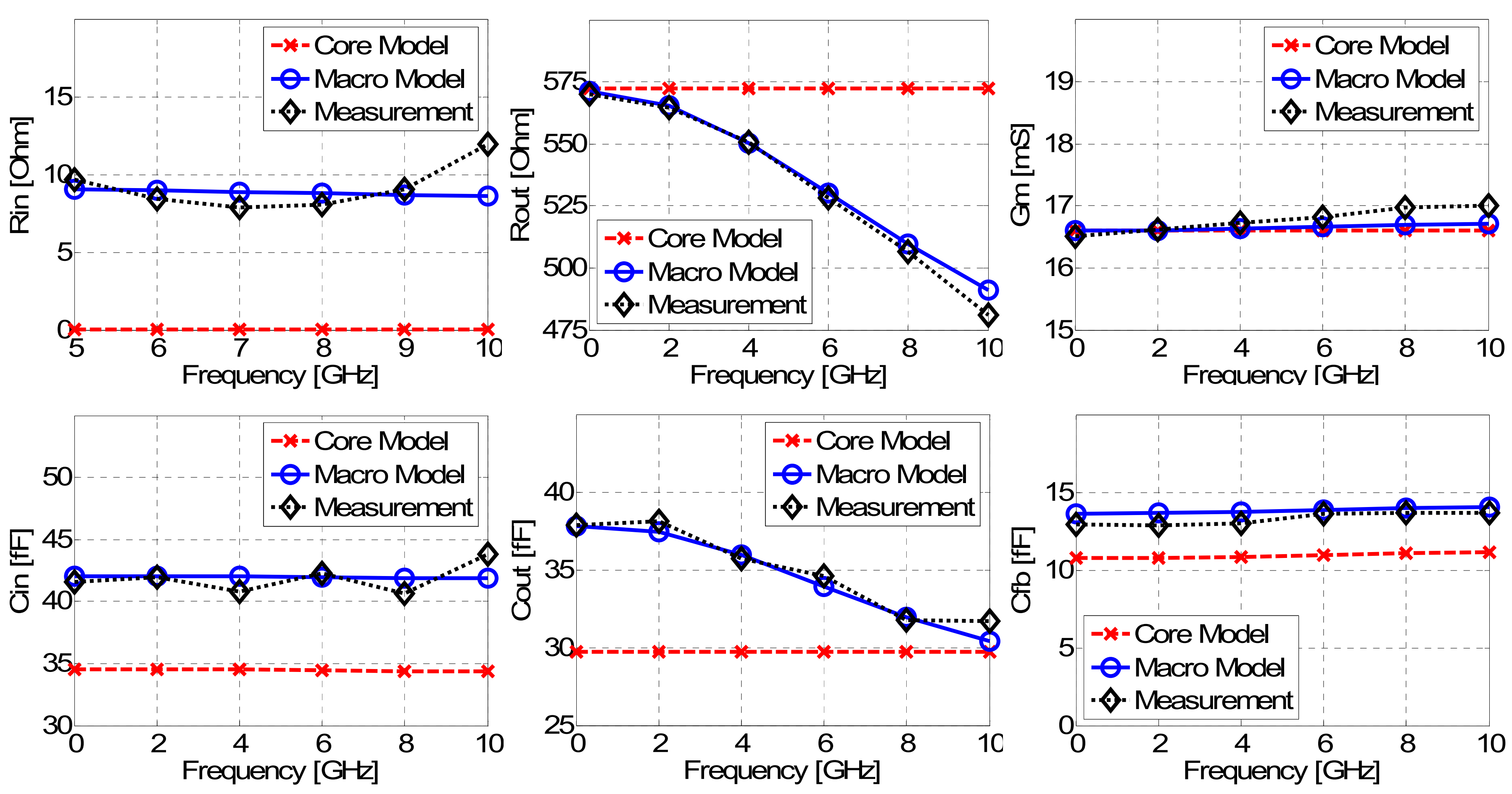
Interconnect RC Modeling Using 3D Field Solver



Width (μm)	nf	C_{gs_wire} (fF)	C_{gd_wire} (fF)	C_{ds_wire} (fF)
2.0	4	2.42	1.61	1.41

- Wire capacitance per finger is extracted

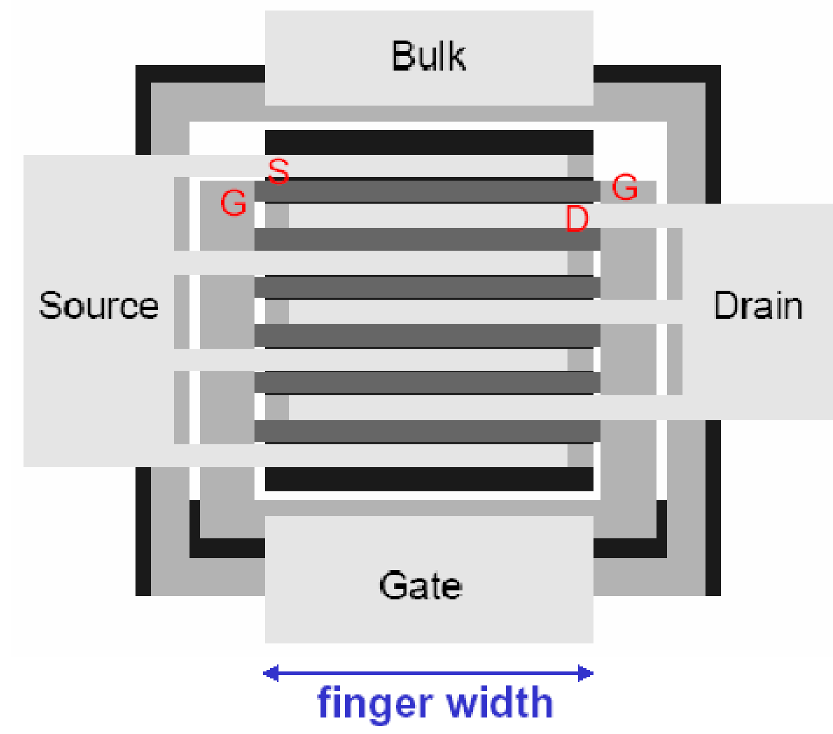
RF Macro Model vs. Measurement (16 x 2μm/0.12 μ m)



R_g = 9.8 Ω, R_{sub} = 475 Ω, C_{gs_ext}= 4 fF, C_{gd_ext}= 2.9 fF, C_{ds_ext}= 5.2 fF

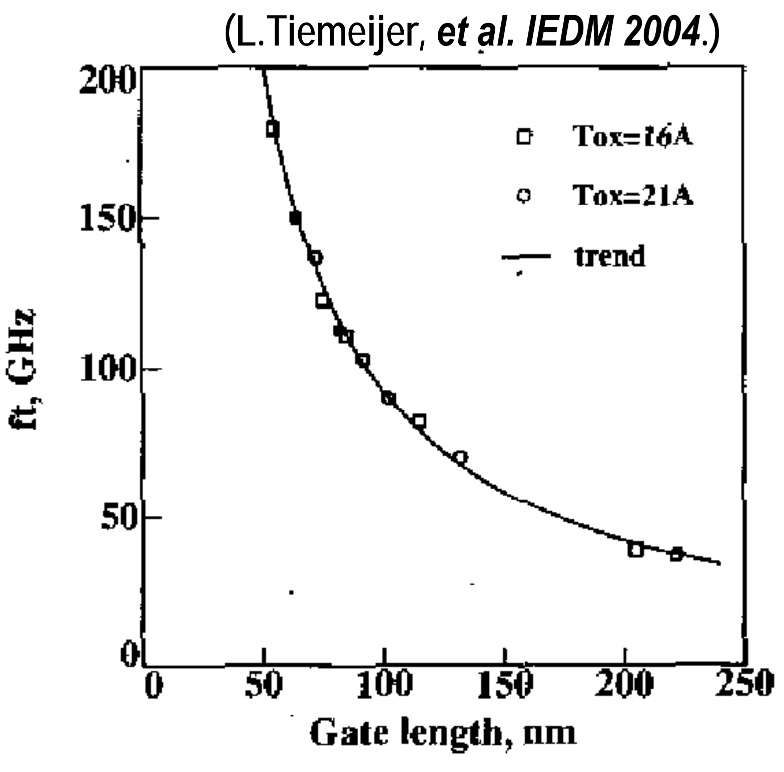
Optimized Layout for fT, fmax and NF

- Parallel Rg improves f_{max} and NF_{min}
- Gate connected at both ends
- Source drain metals do not overlap
- Bulk contacts surround device

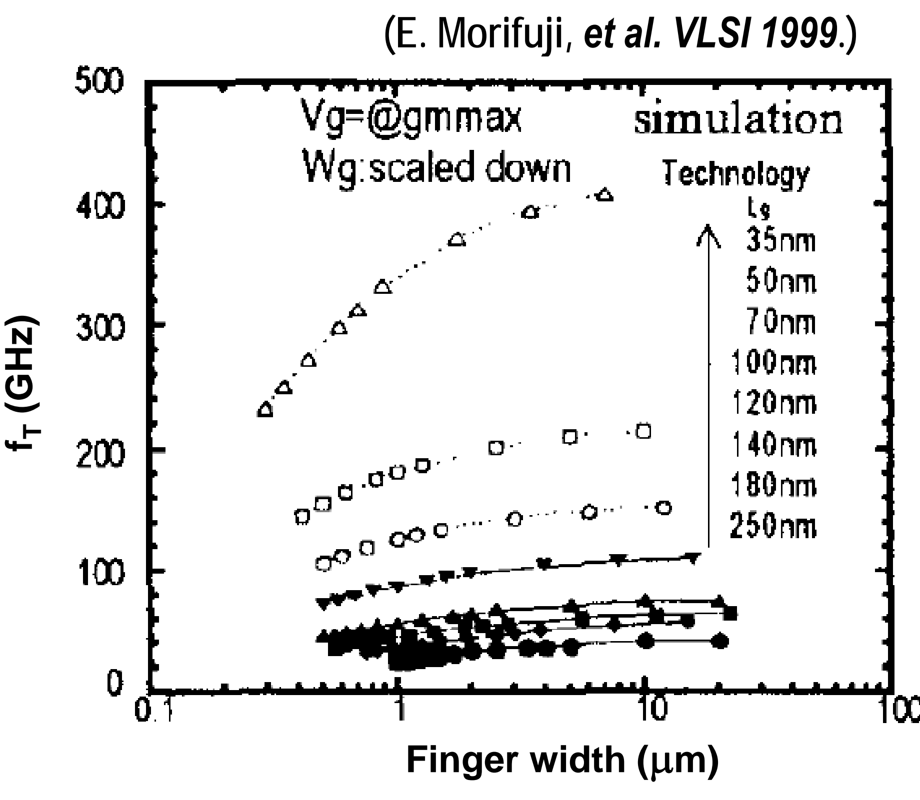


Optimal Finger Width for fT

(L.Tiemeijer, ***et al. IEDM 2004***.)



(E. Morifuji, ***et al. VLSI 1999***.)



- fT approaches vsat / L deep in velocity saturation

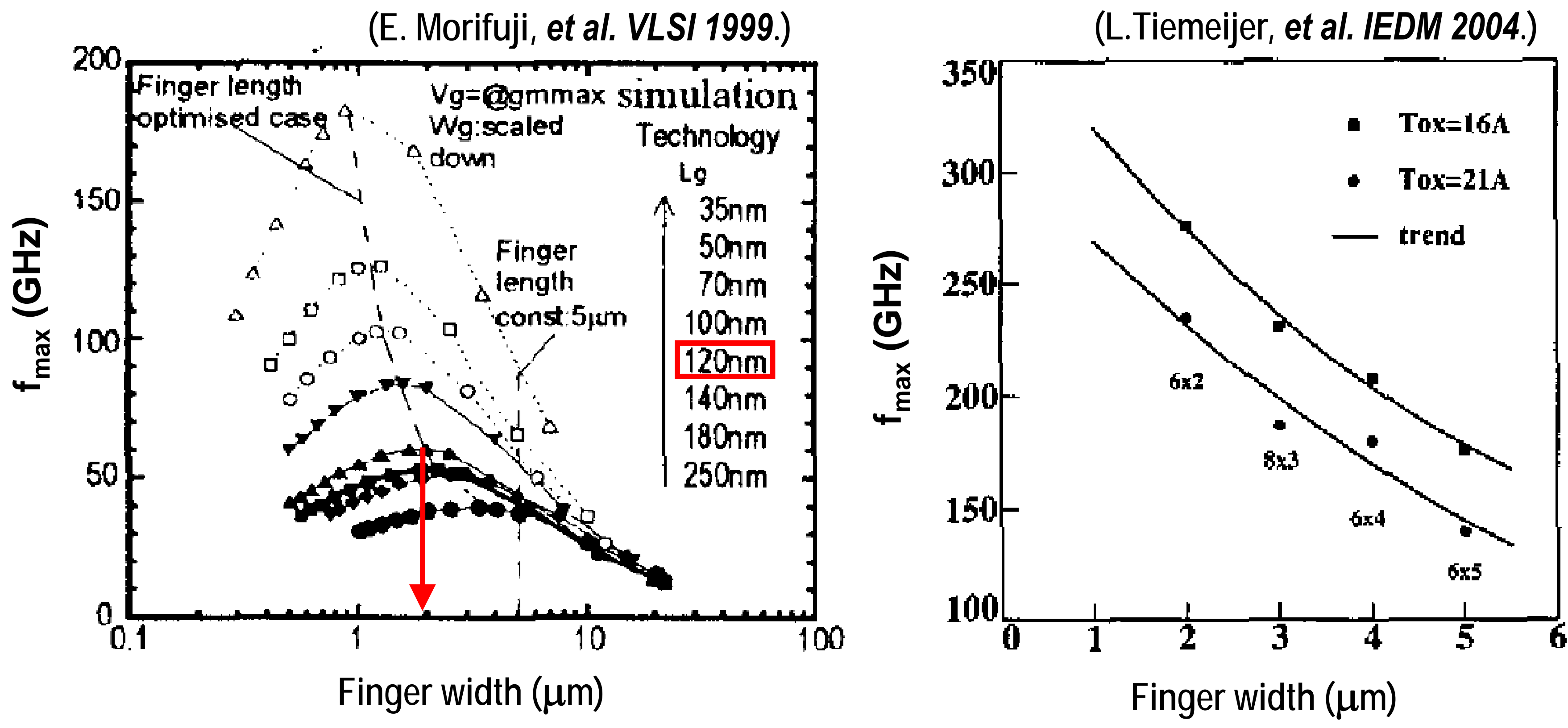
Finger width ↓

⇨No. of fingers ↑

⇨Capacitance ↑

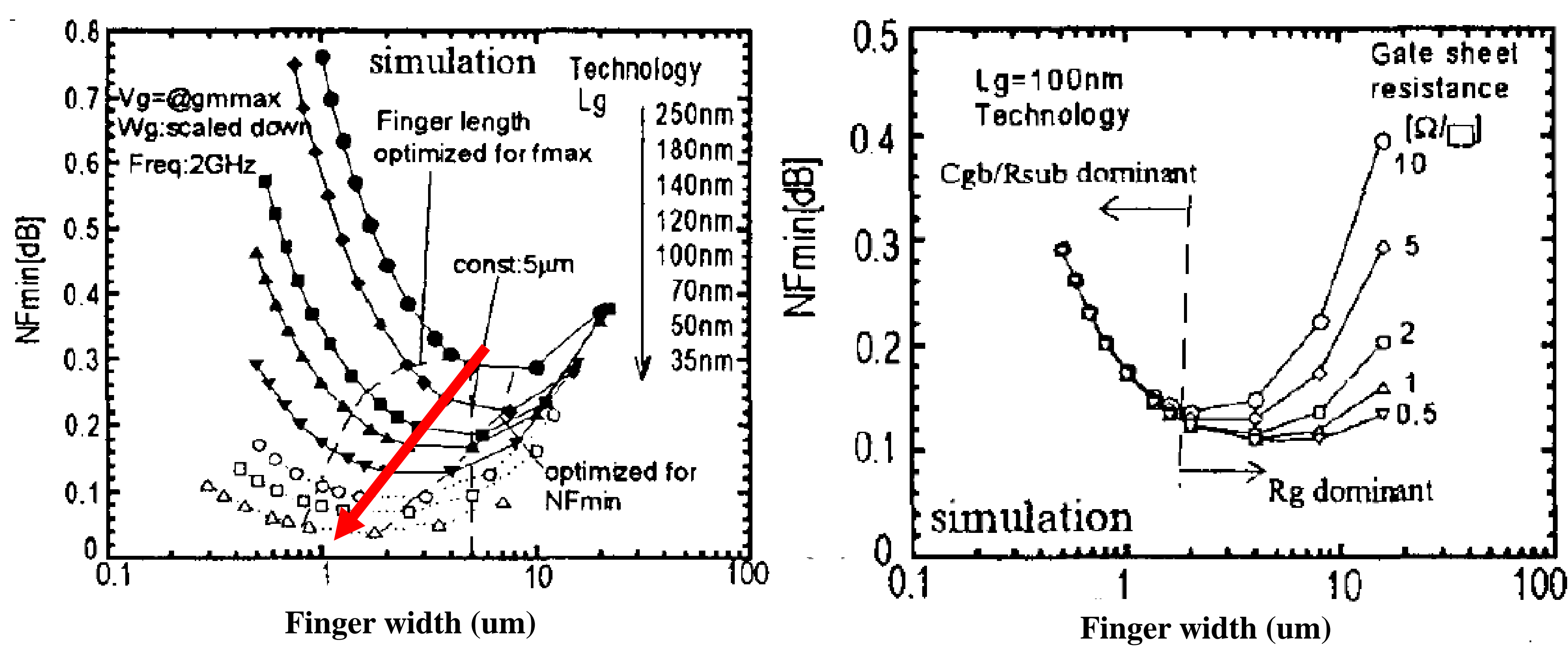
⇨f_T ↓

Optimal Finger Width for f_{max}



- Reducing R_g vs. increasing C_{gg}
- For 0.13-µm, optimal finger width is ~2 µm
- Optimal finger width decreases with device scaling

Optimal Finger Width for NF

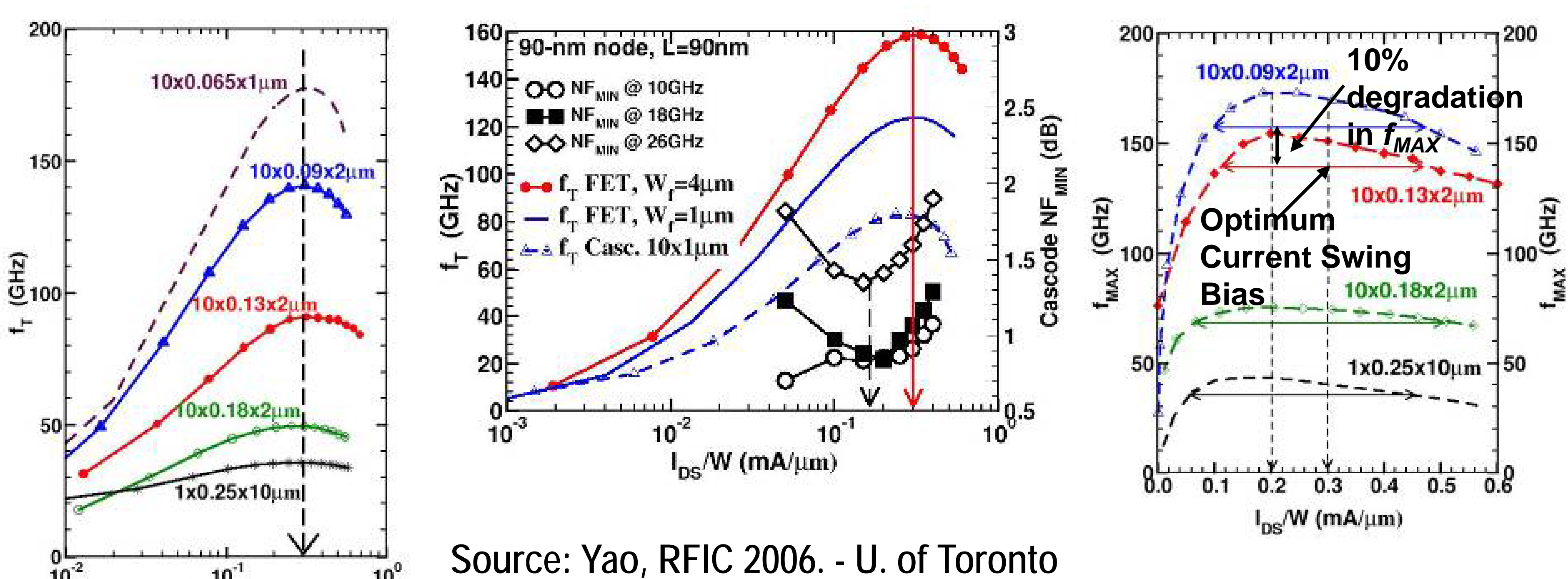


- Noise due to Rg and Rsub can be minimized through layout optimization

Ref. 11

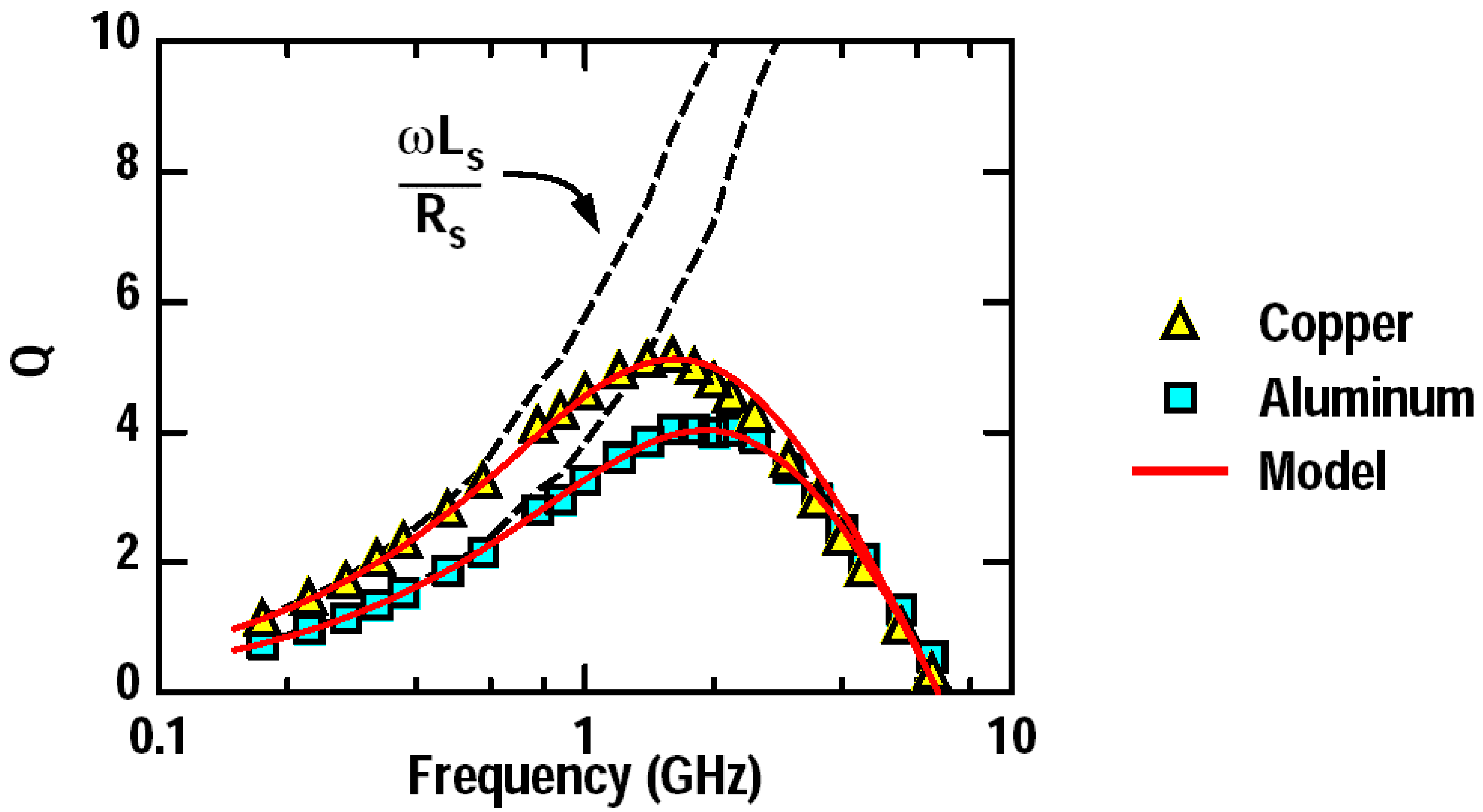
Optimal Biasing for f_T, f_{MAX} and NF_{MIN}

- Peak f_T, f_{MAX} and NF_{MIN} characteristic current densities largely unchanged across technology nodes and foundries
- NF_{MIN} (0.15mA/μm) and peak f_{MAX} (0.2mA/μm) are close → LNAs simultaneously optimized for noise and high gain
- In CMOS PAs optimum current swing when biased at 0.3mA/μm

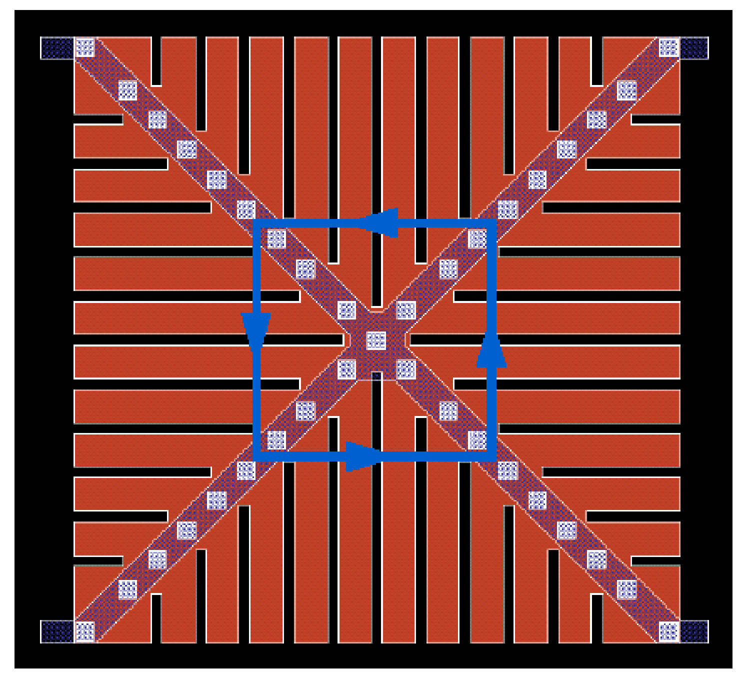


Source: Yao, RFIC 2006. - U. of Toronto

Frequency Response of On-Chip Inductor Q



First Patterned Ground Shield (PGS)

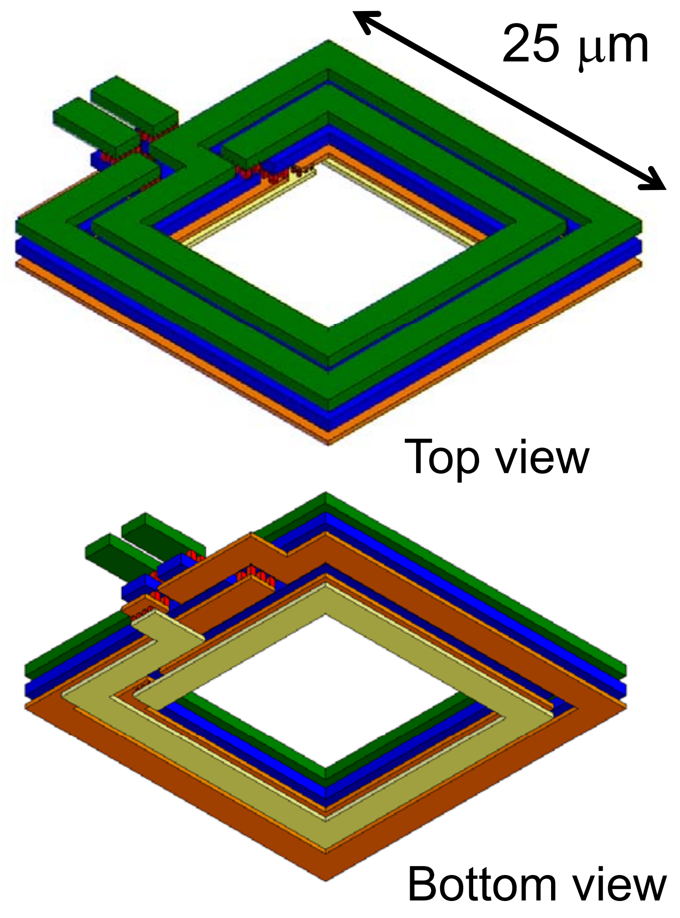


Silicided polysilicon

Induced eddy current

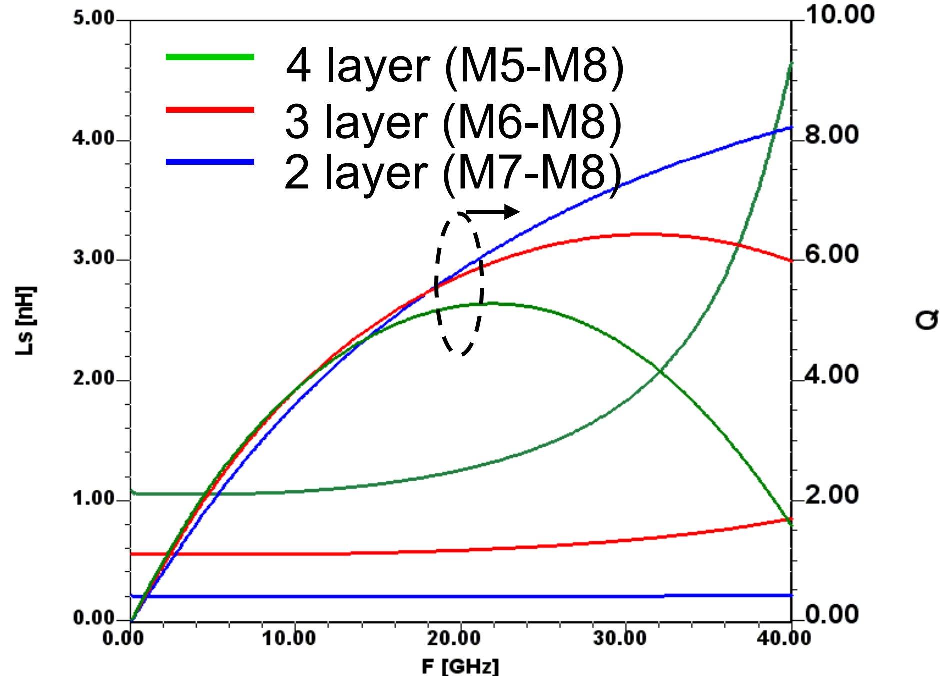
- Inserted between the inductor and substrate
- PGS fingers connected in a “star” shape
- Terminates the E field
- No effect on the H field
- Improves isolation

Self-Shielded Stacked Inductors for high SRF



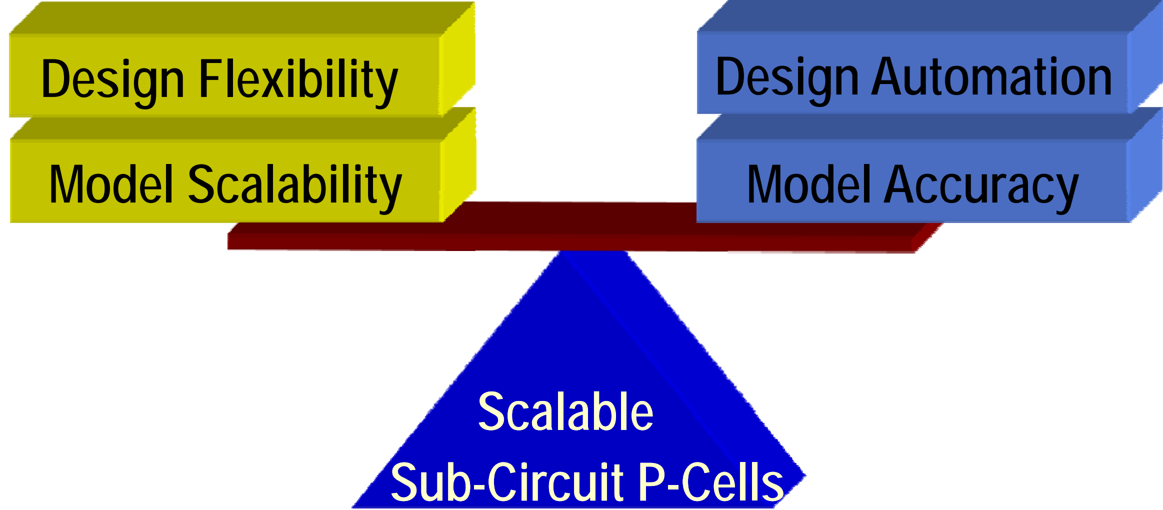
- Self-shielded layout can effectively boost-strap the overlap capacitance *
- 1-nH inductor can be achieved in 25x25 μm^2 using M5 through M8 in a 0.13-μm CMOS 8-metal process

* C.-C. Tang, ***JSSC***, April 2002.



Systematic mm-wave Design with P-Cells

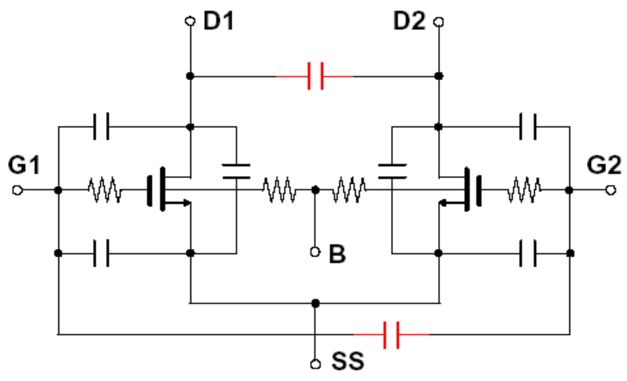
- Stand-alone single device model is insufficient
- Interconnect model accuracy limited by digital RC extraction
- Test structure layout $\neq$ actual circuit layout



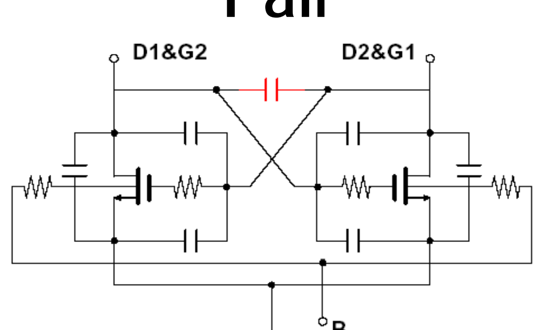
- Leverage the insight to device layout optimization
- Exploit the modularity at the sub-circuit level

Sample P-Cell Layouts and Circuit Models

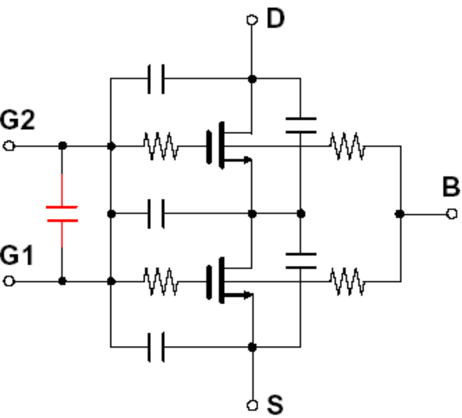
Diff Pair

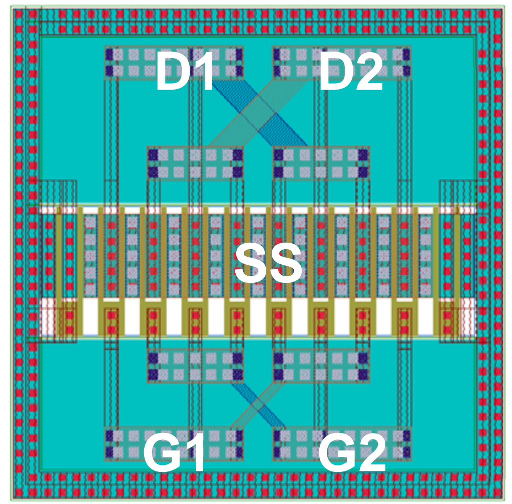


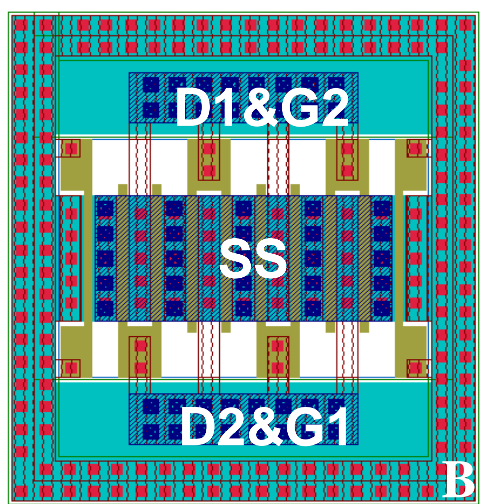
Cross-Coupled Pair

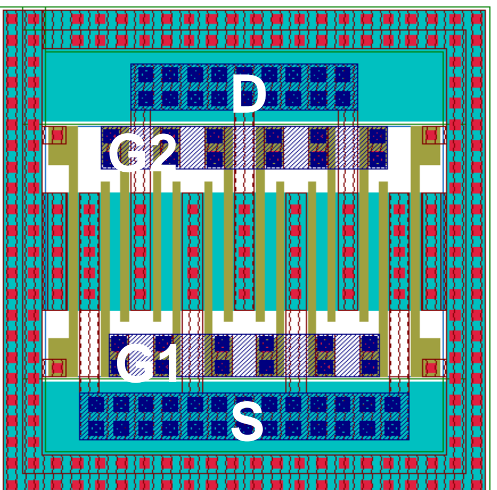


Cascode

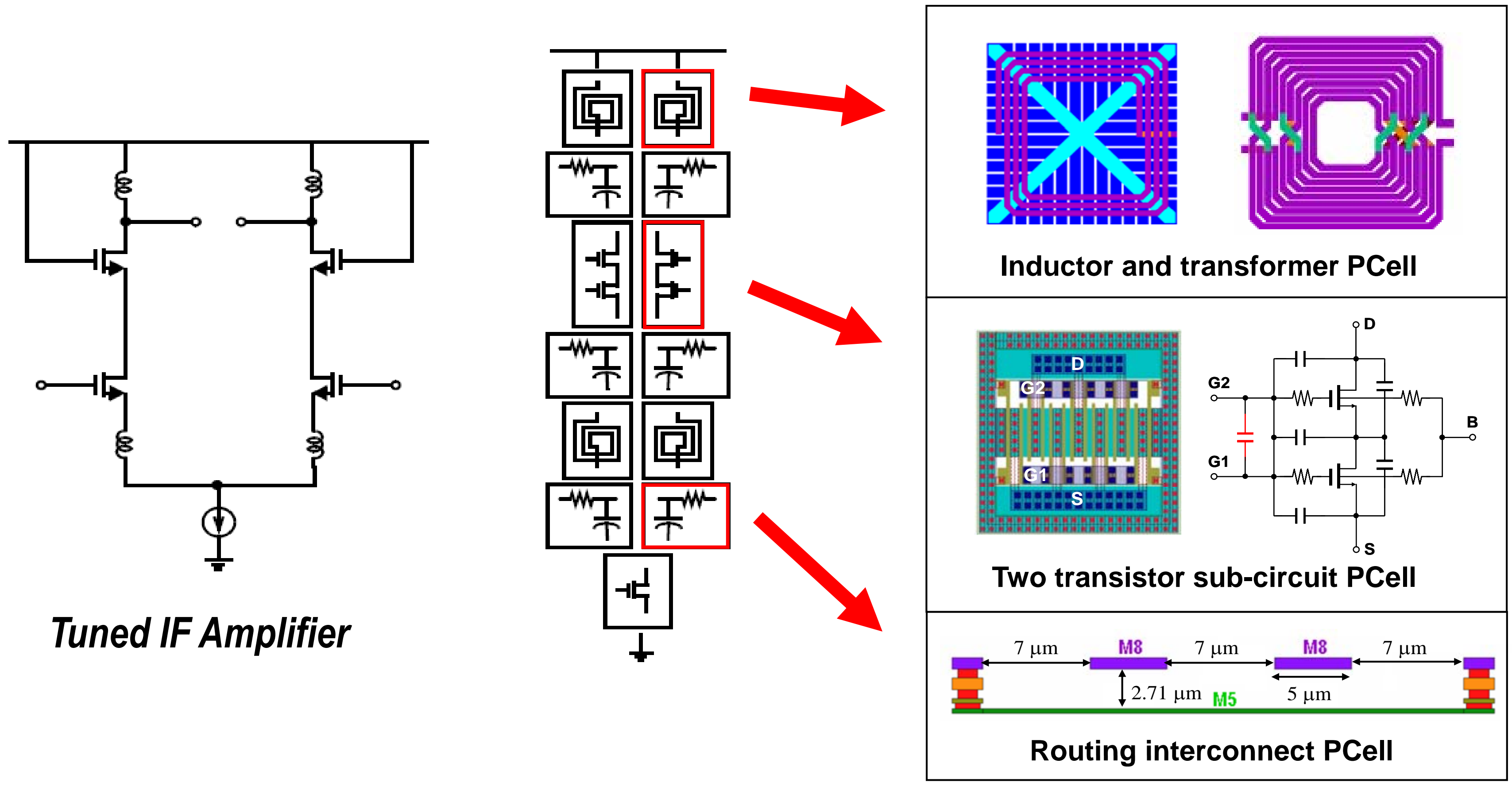








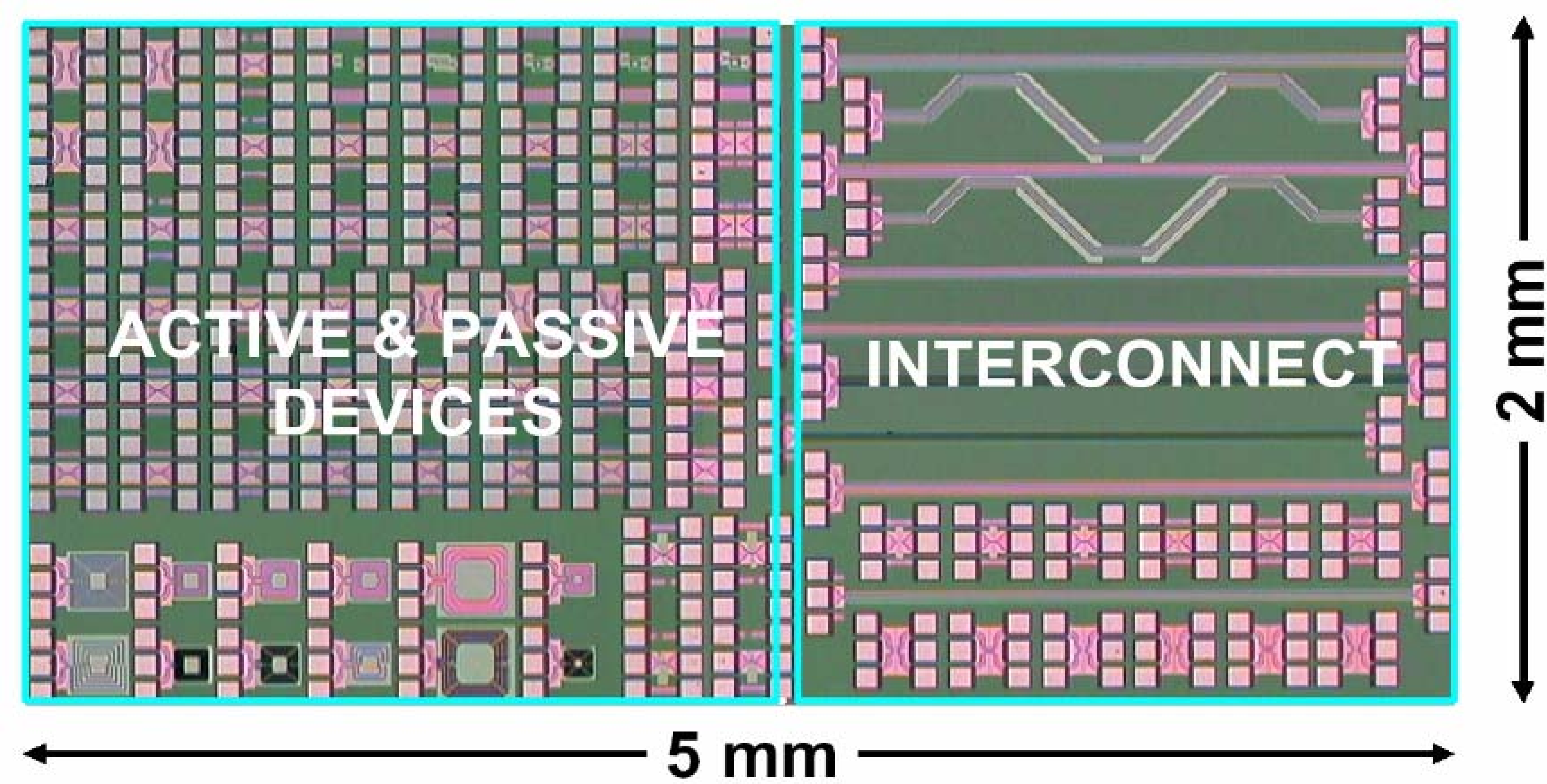
Sub-Circuit Cell Library for mm-wave Design



- A unified design and modeling framework
- Each sub-circuit P-Cell has its scalable circuit model

mm-wave P-Cell Characterization Test Structures

- Measured S-parameters to validate macro models
- UMC 0.13-μm CMOS with 8 copper layers



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140-220 & 220-330 GHz On-Wafer Network Analysis

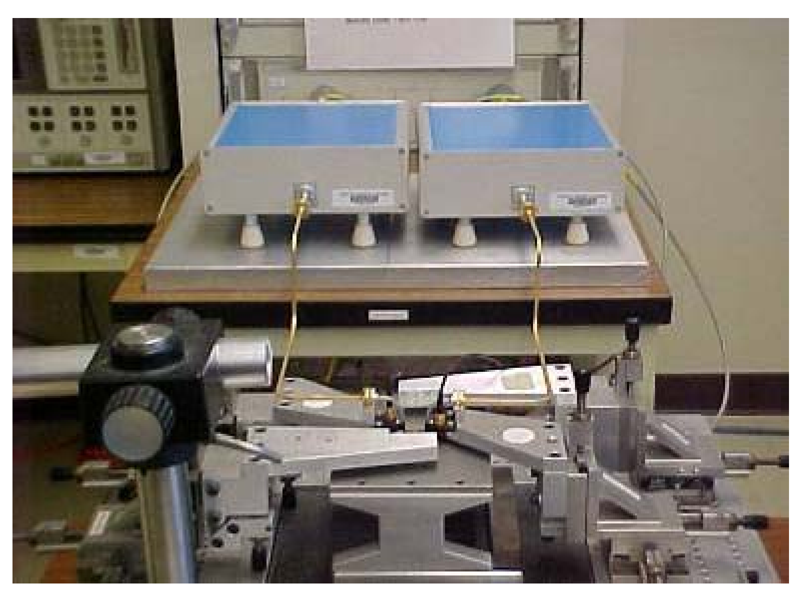
• HP8510C VNA,
Oleson Microwave Lab mm-wave Extenders

• coplanar wafer probes made by:
GGB Industries, Cascade Microtech

•connection via short length of waveguide

• Internal bias Tee's in probes for biasing active devices

•measurements to 100 GHz can be in coax.

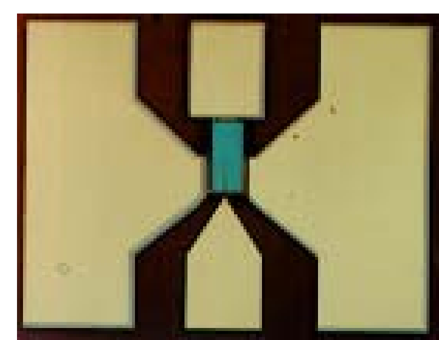


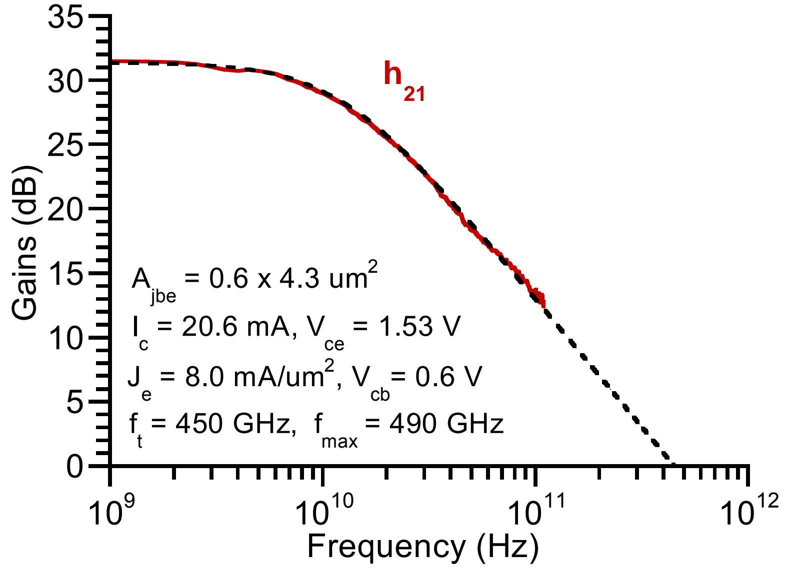
GGB Wafer Probes
330 GHz available with bias Tees

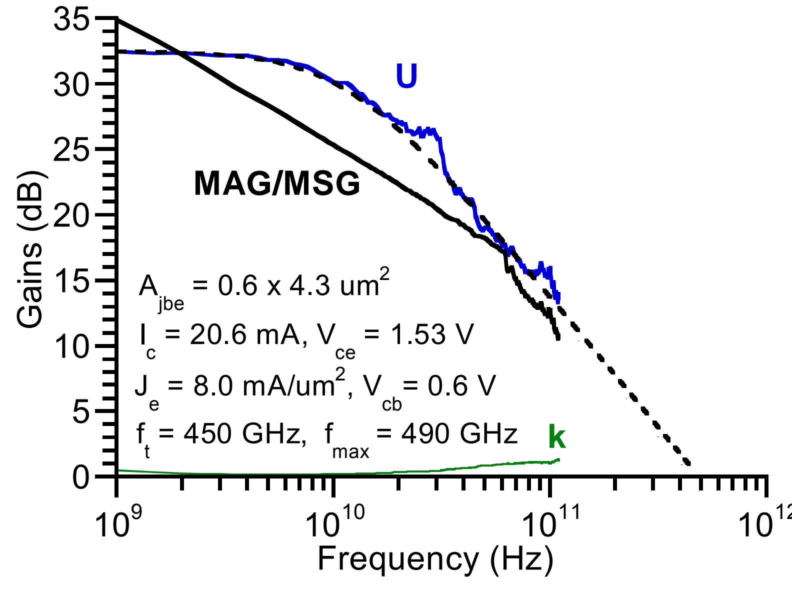
High Frequency Device Gain Measurements : Standard Pads

Measuring wideband transistors is very hard ! Much harder than measuring amplifiers. Determining fmax in particular is extremely difficult on high-fmax or small devices

Standard "short pads"
must strip pad capacitance
must strip pad inductance--or ft will be too high !
cal can be bad due to substrate coupling
make pads small, and shield them from substrate
cal can be bad due to probe coupling
use small probe pitch, use well-shielded probes





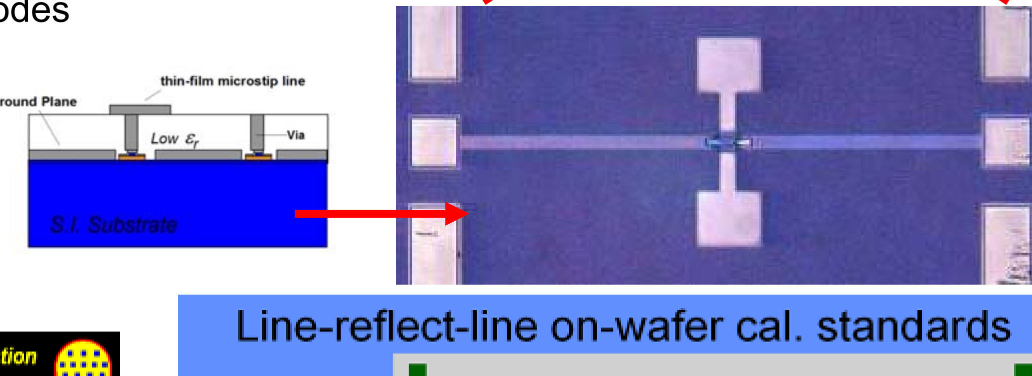


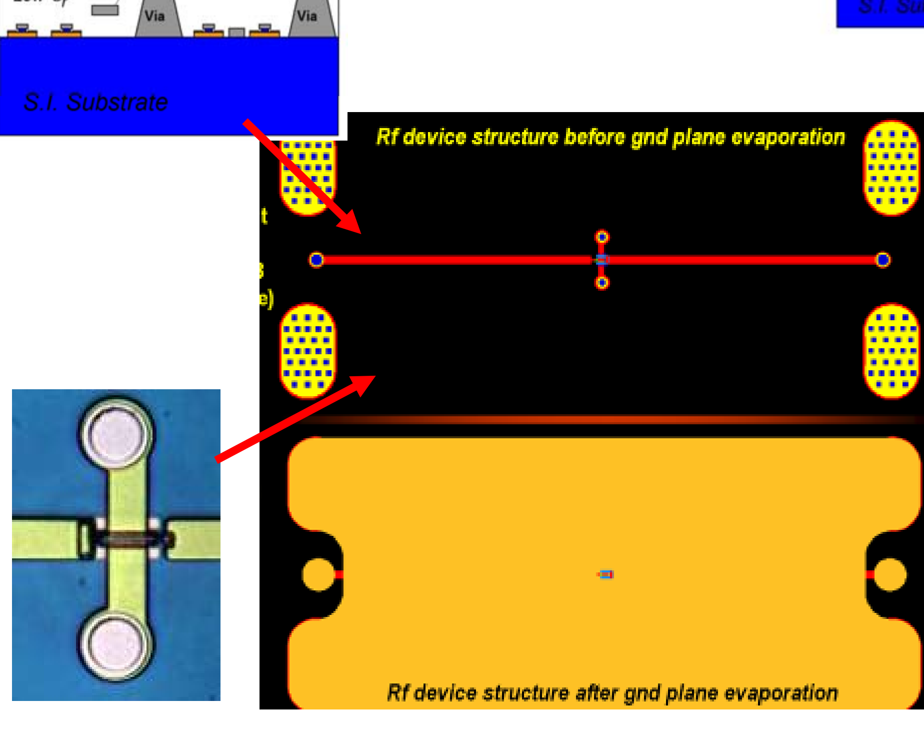
High Frequency Measurements : On-Wafer LRL

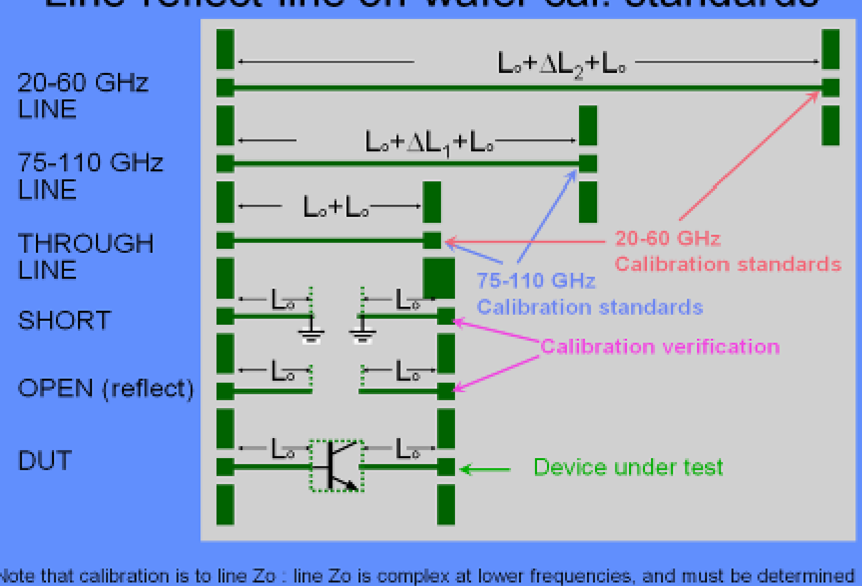
Extended Reference planes
transistors placed at center of long on-wafer line
LRL standards placed on wafer
large probe separation → probe coupling reduced
still should use the best-shielded probes available

Problem: substrate mode coupling
method will FAIL if lines couple to substrate modes
→ method works very poorly with CPW lines
need on wafer thin-film microstrip lines

CPW







Unilateral Power Gain

1) Cancel device feedback with external lossless feedback

$\rightarrow Y_{12} = S_{12} = 0$

2) Match input and output

Resulting power gain is Mason's Unilateral Gain

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}$$

Monolithic amplifiers are not easily made unilateral

$\rightarrow$ U mostly of historical relevance to IC design

For simple BJT model, U rolls off at -20 dB/decade

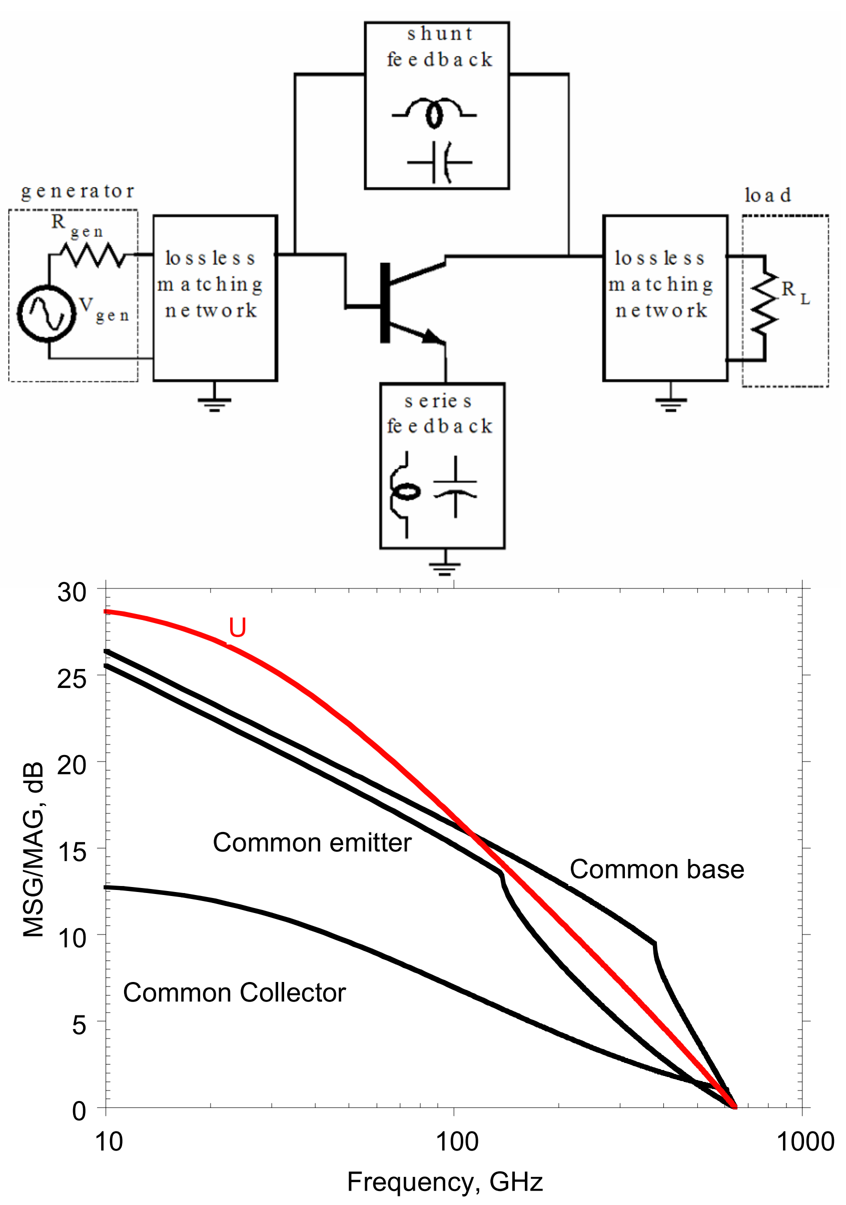
$\rightarrow$ U useful for extrapolation to find f_{max}

In III-V FETs, U shows peak from C_{ds} - R_s - R_d interaction

$\rightarrow$ U hard to use for f_{max} extrapolation

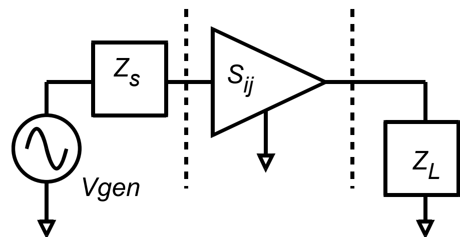
For bulk CMOS, C_{ds} is sheilded by substrate

$\rightarrow$ U should be OK for f_{max} extrapolation



Design Tools: Power Gain Definitions

Transducer Gain

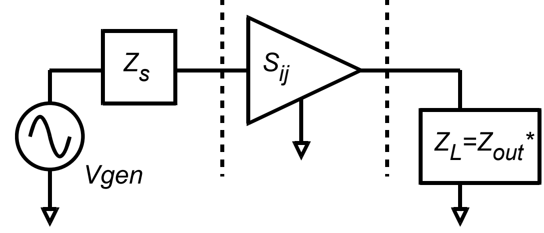


$$G_T = P_{load} / P_{av,gen}$$

$$= \frac{\text{load power}}{\text{power available from generator}}$$

$$= \text{general - case gain}$$

Available Gain

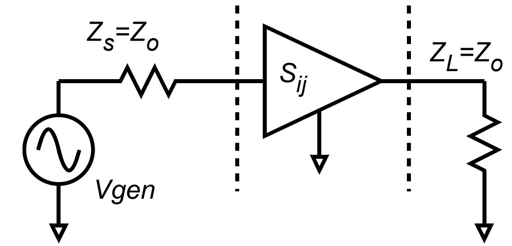


$$G_A = P_{av,a} / P_{av,gen}$$

$$= \frac{\text{power available from amplifier}}{\text{power available from generator}}$$

$$= \text{gain with output matched}$$

Insertion Gain

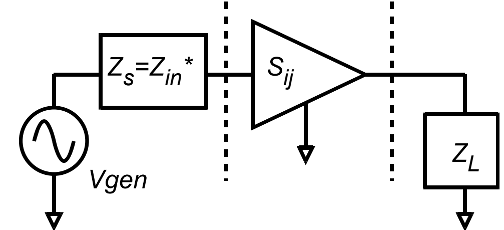


$$\|S_{21}\|^2 = P_{av,a} / P_{av,gen}$$

$$= \frac{\text{power delivered to } Z_o \text{ load}}{\text{power available from } Z_o \text{ generator}}$$

$$= \text{gain in a 50 Ohm enviroment}$$

Operating Gain

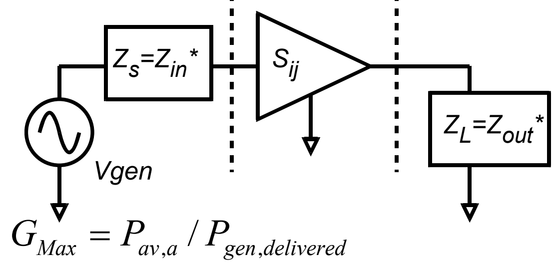


$$G_P = P_{load} / P_{gen,delivered}$$

$$= \frac{\text{load power}}{\text{power delivered from generator}}$$

$$= \text{gain with input matched}$$

Maximum Available Gain



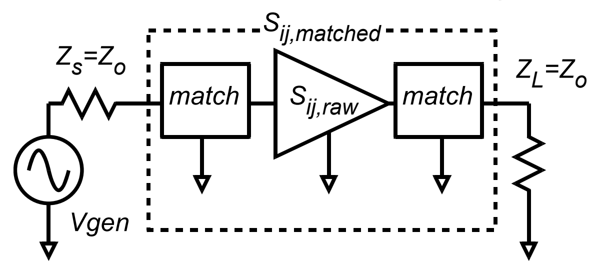
$$G_{Max} = P_{av,a} / P_{gen,delivered}$$

$$= \frac{\text{power available from amplifier}}{\text{power delivered from generator}}$$

$$= \text{gain with both ports matched}$$

...MAG may not exist...

After impedance-matching:



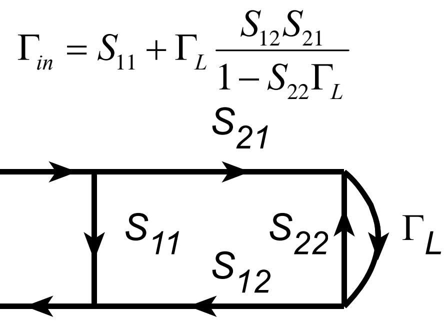
$$\|S_{21,matched}\|^2 = G_{\max,\text{raw}}$$

$$S_{11,matched} = S_{22,matched} = 0$$

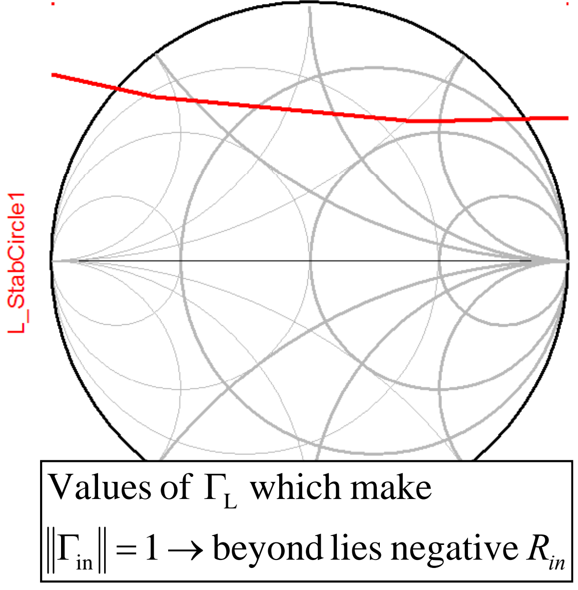
....but only if unconditionally stable...

Design Tools: Stability Factors, Stability Circles

$$\Gamma_{in} = S_{11} + \Gamma_L \frac{S_{12}S_{21}}{1 - S_{22}\Gamma_L}$$

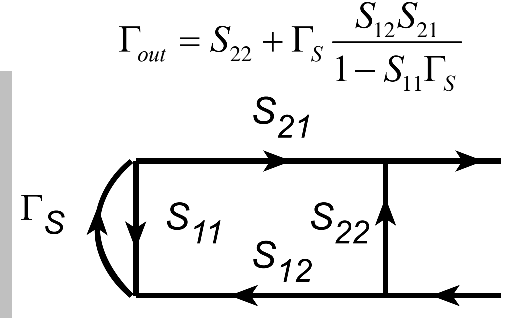


Load Stability Circle

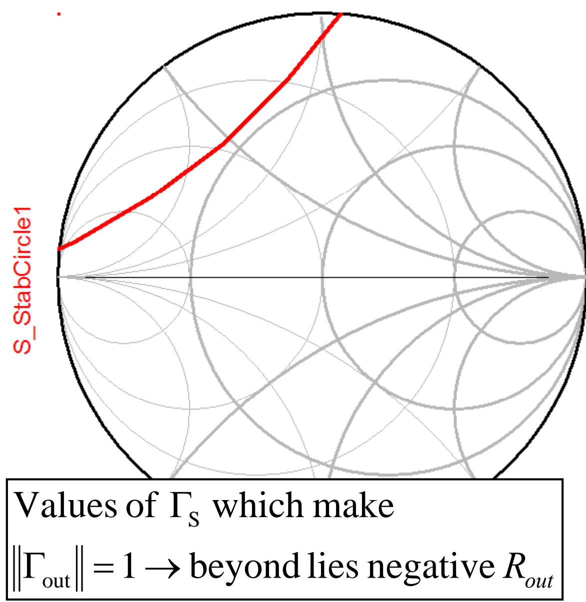


Values of Γ_L which make $\|\Gamma_{in}\| = 1 \rightarrow$ beyond lies negative R_{in}

$$\Gamma_{out} = S_{22} + \Gamma_S \frac{S_{12}S_{21}}{1 - S_{11}\Gamma_S}$$



Source Stability Circle



Values of Γ_S which make $\|\Gamma_{out}\| = 1 \rightarrow$ beyond lies negative R_{out}

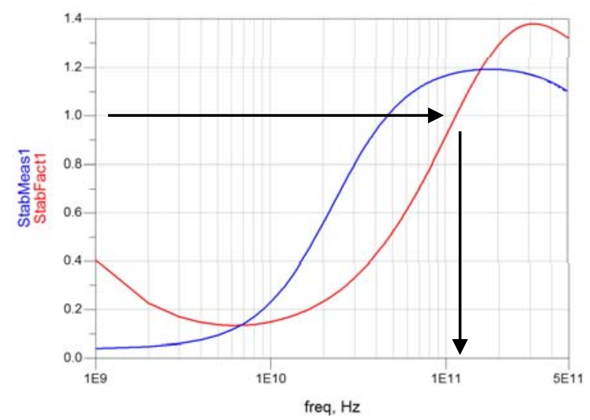
Unconditionally stable (stable with all (Γ_L, Γ_S) if :

K = Rollet stability factor

$$= \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \det^2[S]}{2|S_{21}S_{12}|} > 1$$

and B = stability measure

$$= 1 - |S_{11}|^2 - |S_{22}|^2 - \det^2[S] > 0$$

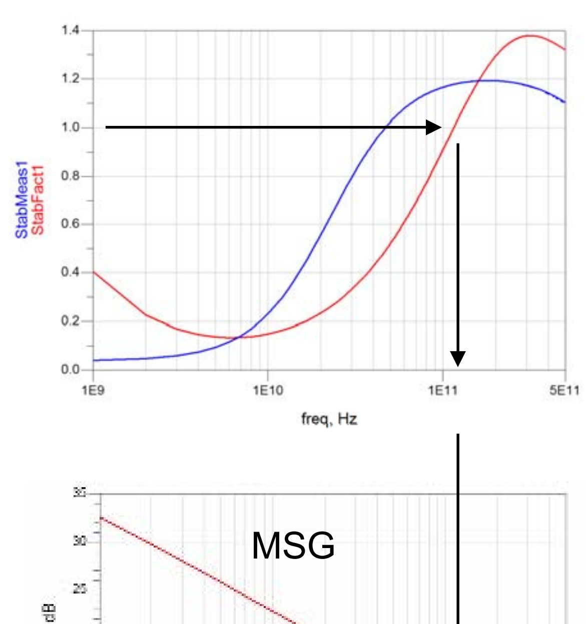


Negative port impedance→ negative-R oscillator
Tuning for highest gain→ infinite gain (oscillation)

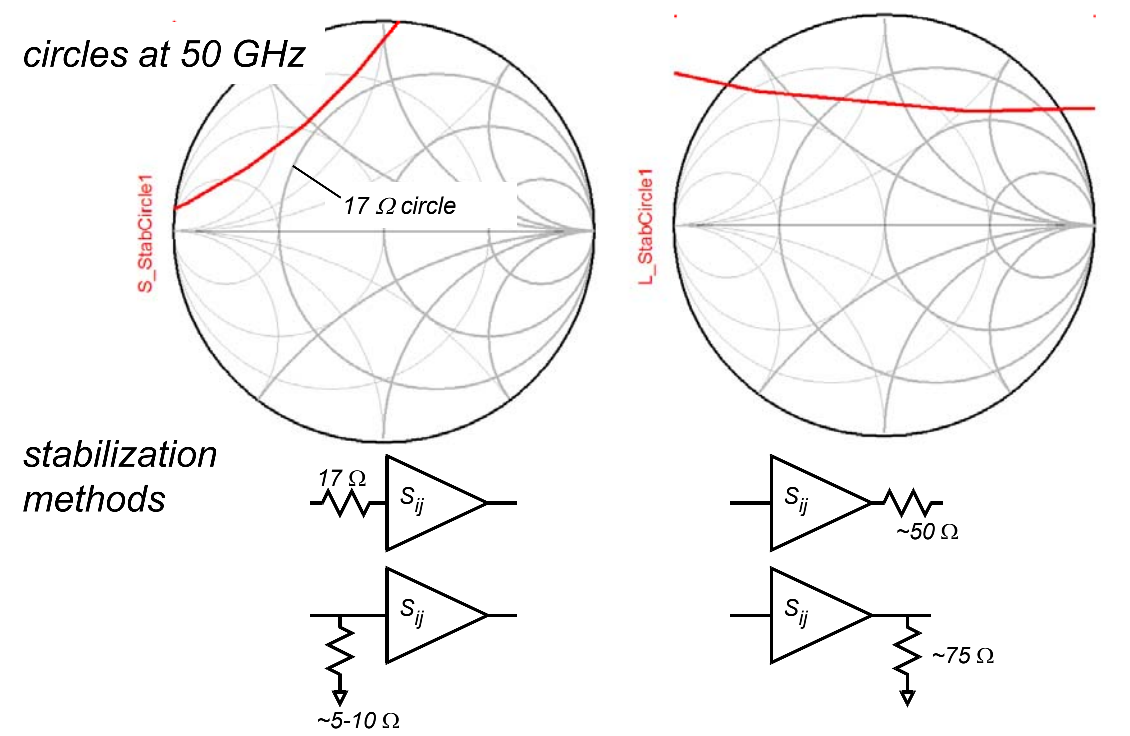
Design Tools: Maximum Stable Gain

Maximum stable gain = MSG

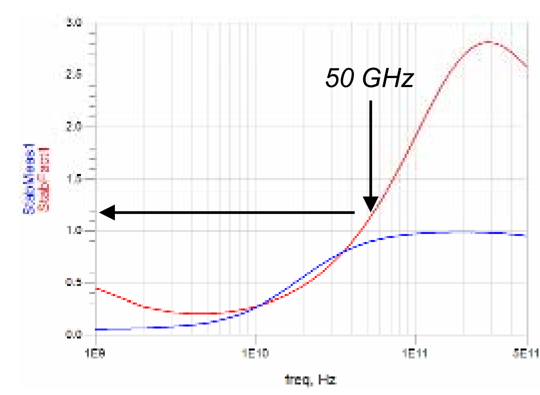
$$= \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} = \frac{|Z_{21}|}{|Z_{12}|}$$

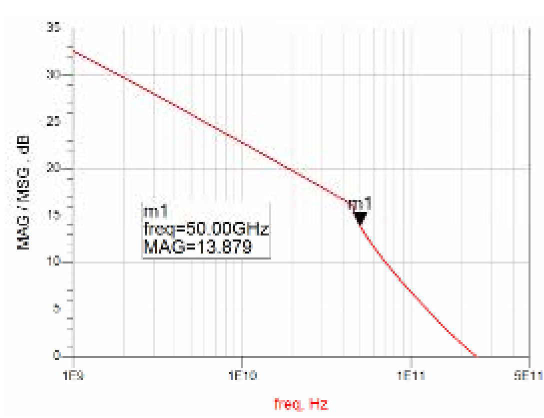


Adding series/shunt resistance excludes source or load from unstable regions → stabilizes



results

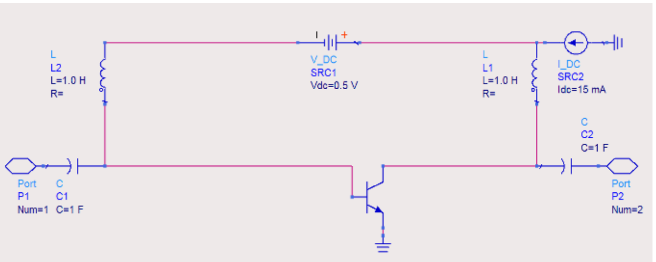




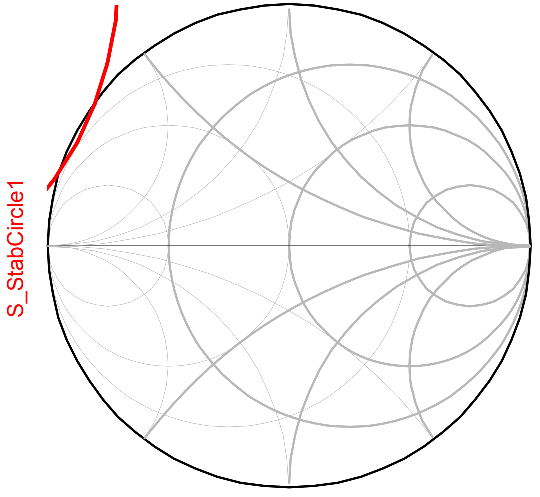
Design Procedure: Simple Gain-Matched Amplifier

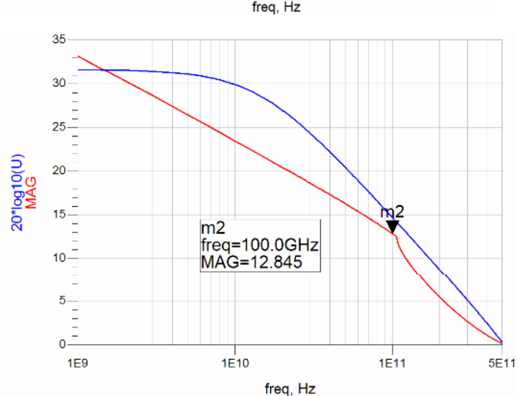
First:
stabilize at the design frequency

---device is potentially unstable at 100 GHz design frequency

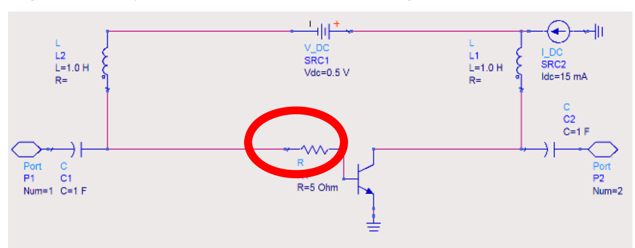


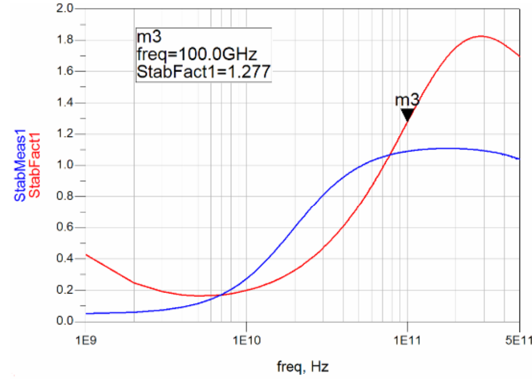
source stability circle:
~5 Ohm on input will overstabilize the device

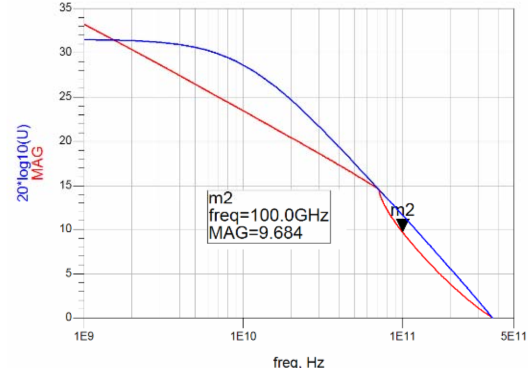




After stabilizing
(slightly over-stabilizing)





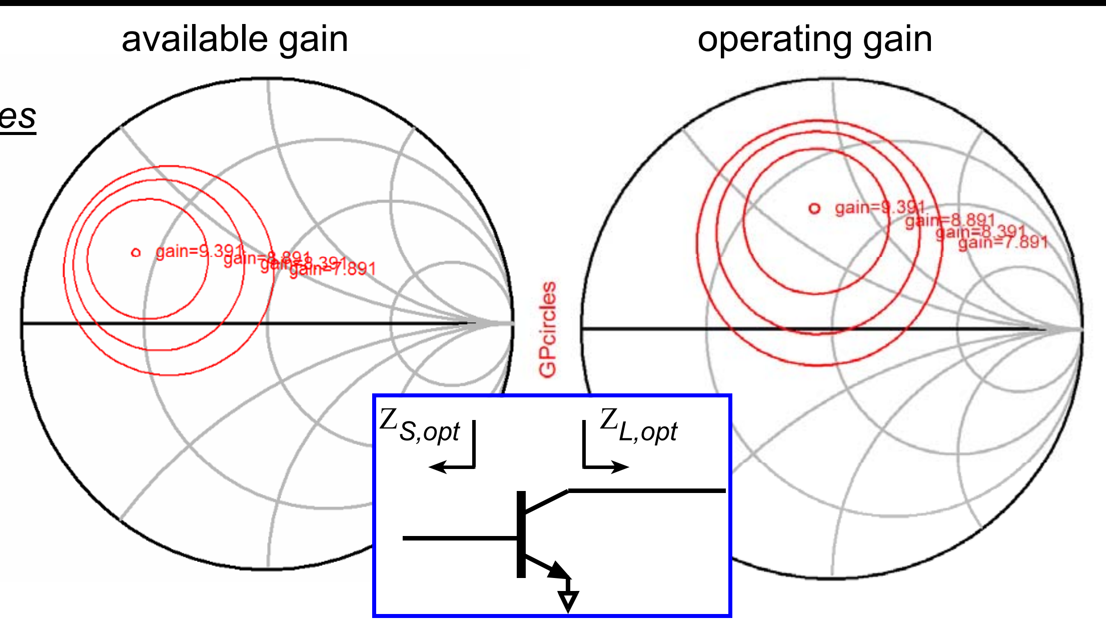


Design Procedure: Simple Gain-Matched Amplifier

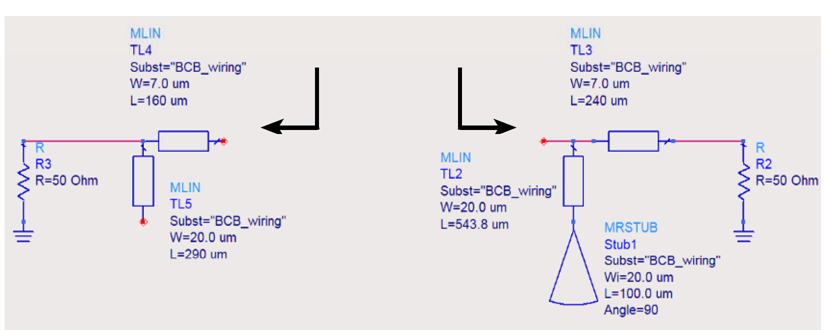
Second:
Determine required interface impedances

The Ga & Gp circles define the source & load impedances which the transistor must see

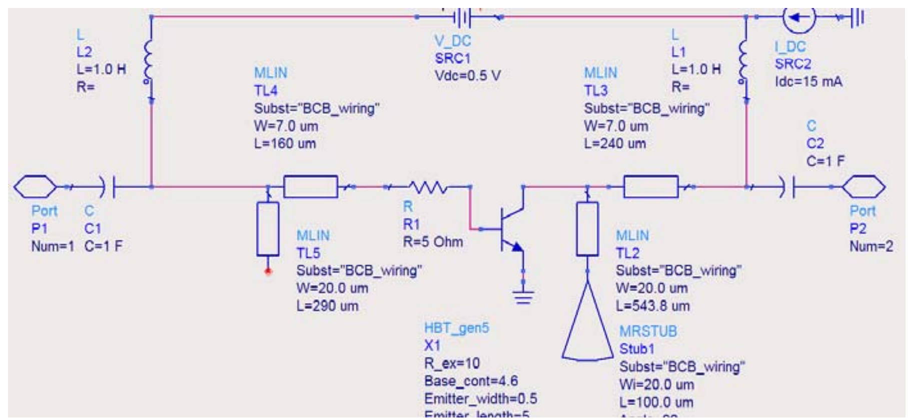
...it is necessary to OVERSTABILIZE the device to move the Ga & Gp circles towards the Smith chart center



Third:
Design Input & Output Tuning Networks
...to provide these impedances...

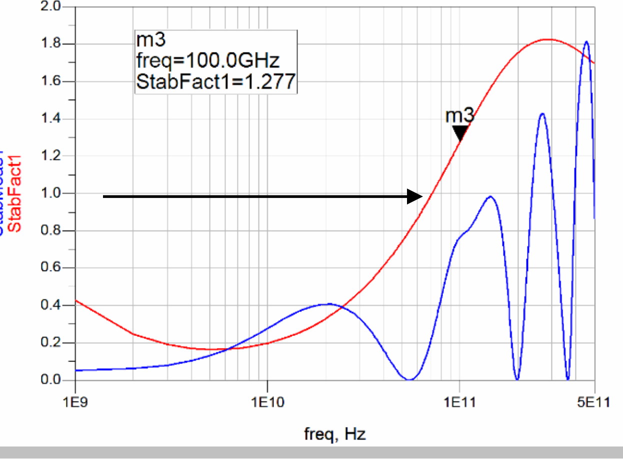


...added to device, the amplifier is not yet complete...

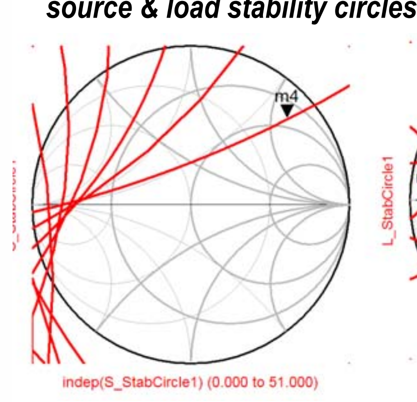


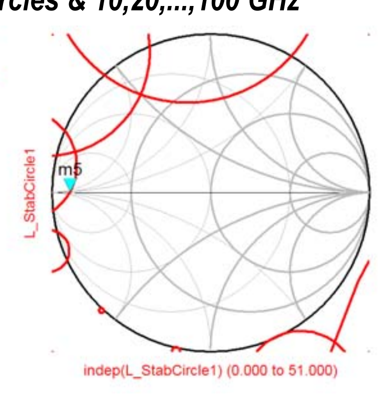
Design Procedure: Simple Gain-Matched Amplifier

Forth:
Add out-of-band stabilization
potentially unstable
below 75 GHz

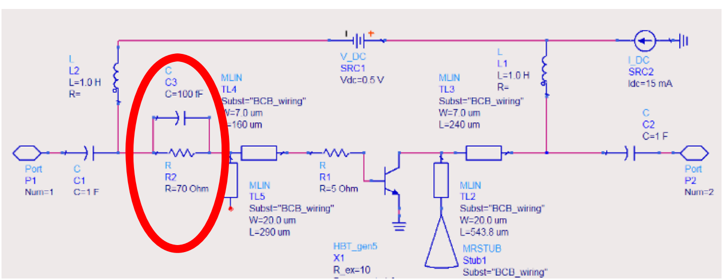


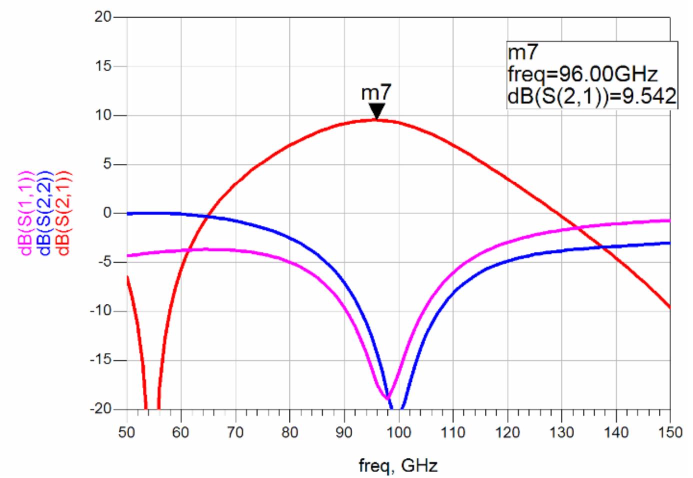
source & load stability circles & 10,20,...,100 GHz





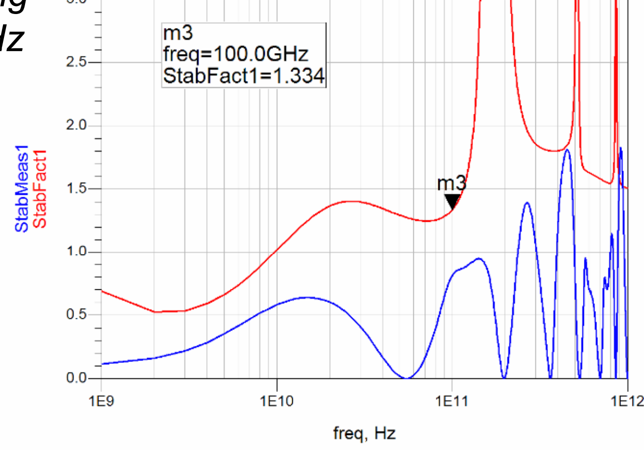
with frequency-selective series stabilization





...caused only slight mistuning & slight gain drop @ 100 GHz

...and is unconditionally stable above 10 GHz



Design Procedure: Effect of Line Losses

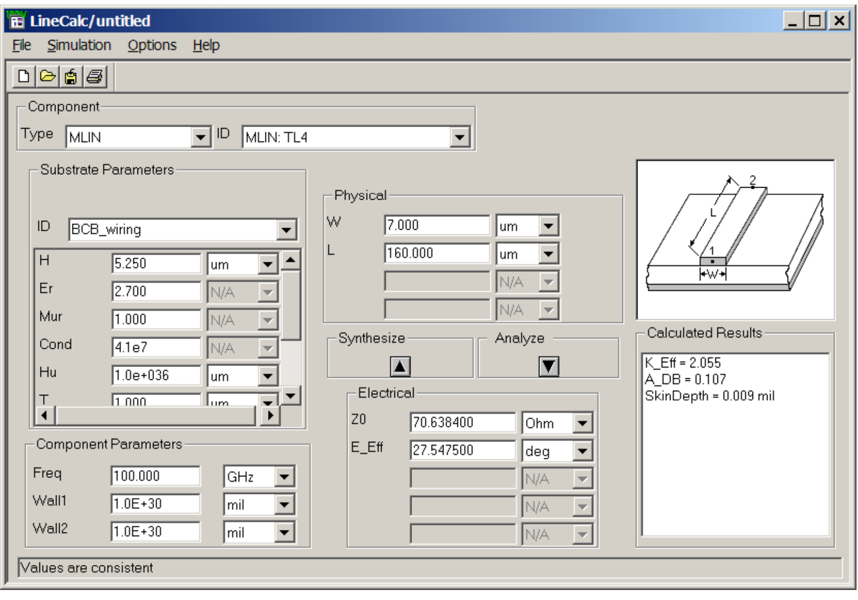
Finally:
adjusting for line losses

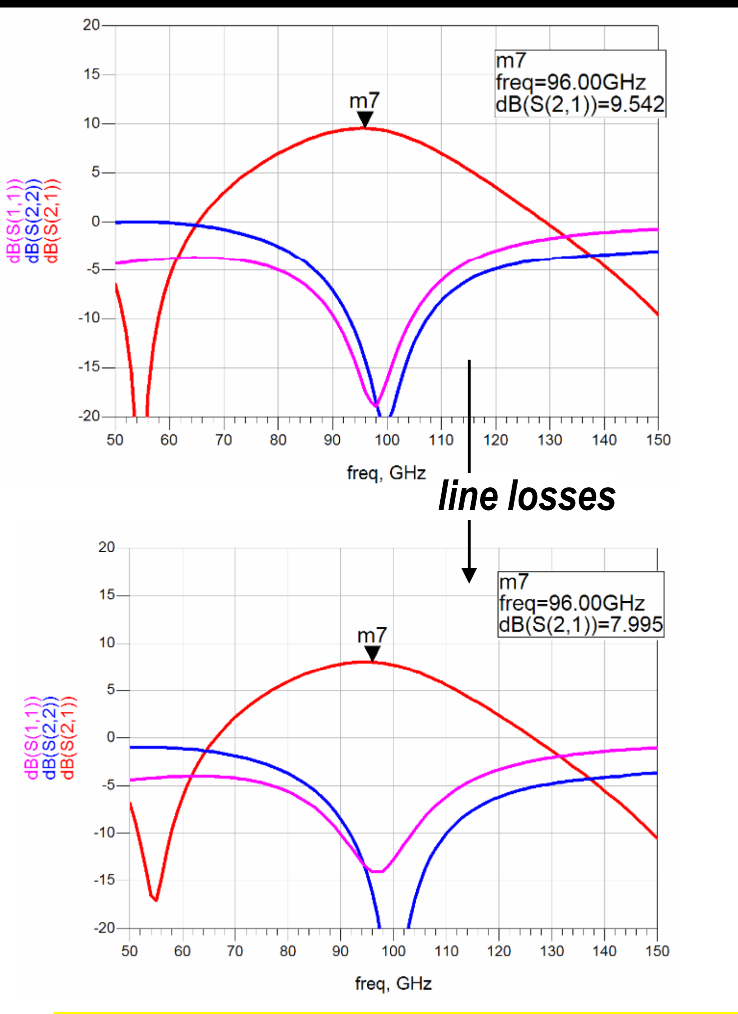
high line skin effect losses → reduced gain

but line losses also increase stability factor

loss in gain are partly recovered
by reducing stabilization resistance &
re-tuning the design

--no analytical procedure; just component tweaking

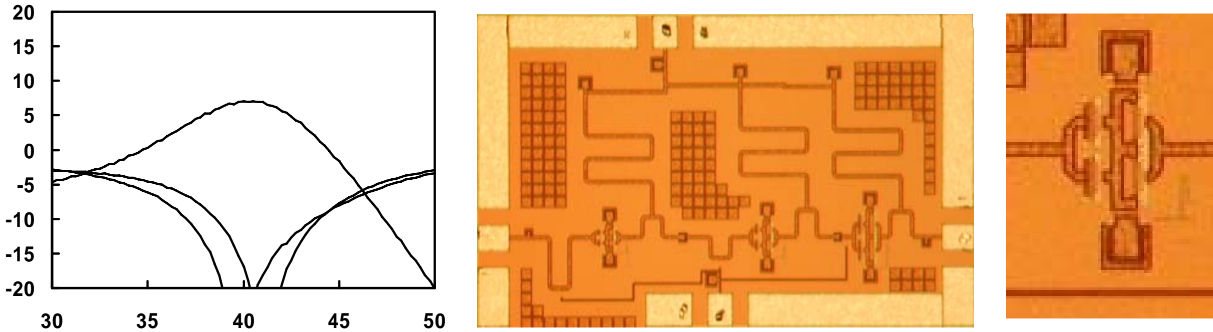


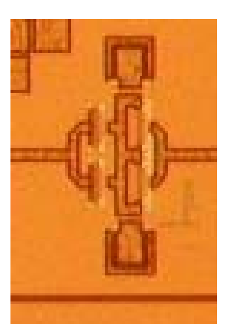


line losses have severe impact
...in VLSI wiring environment
...particularly at 50 + GHz
...particularly with high-power amplifiers

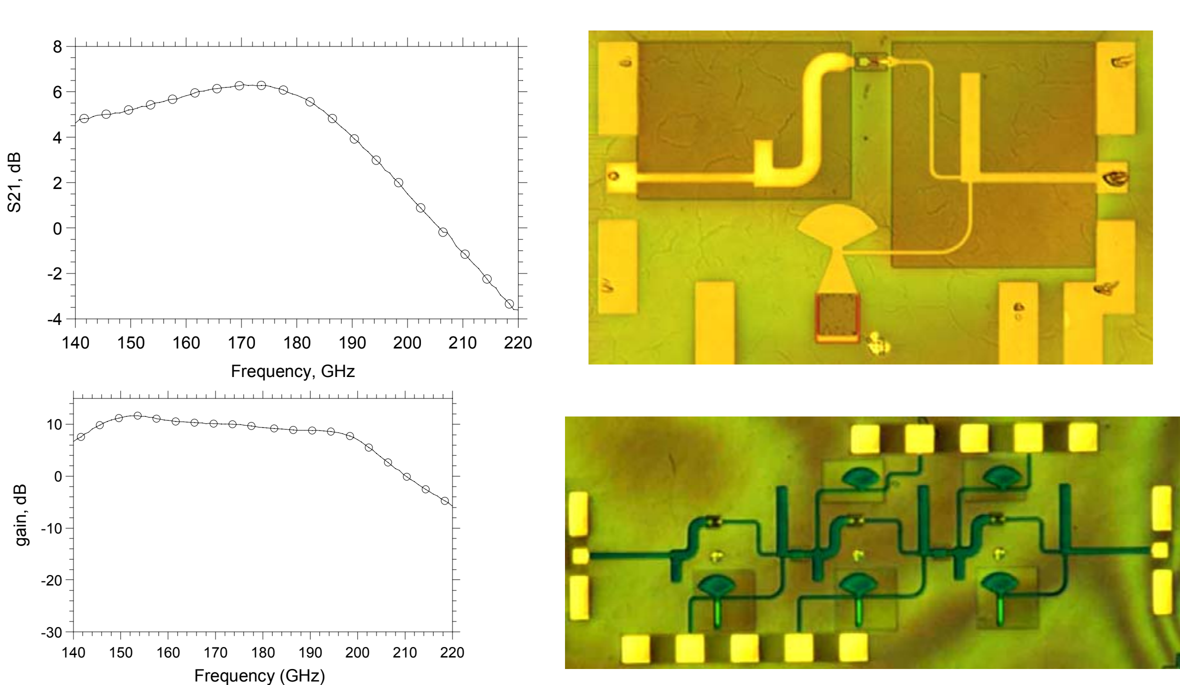
Tuned Amplifier Examples

3-stage cascode in 180 nm CMOS





III-V HBT small-signal amplifiers

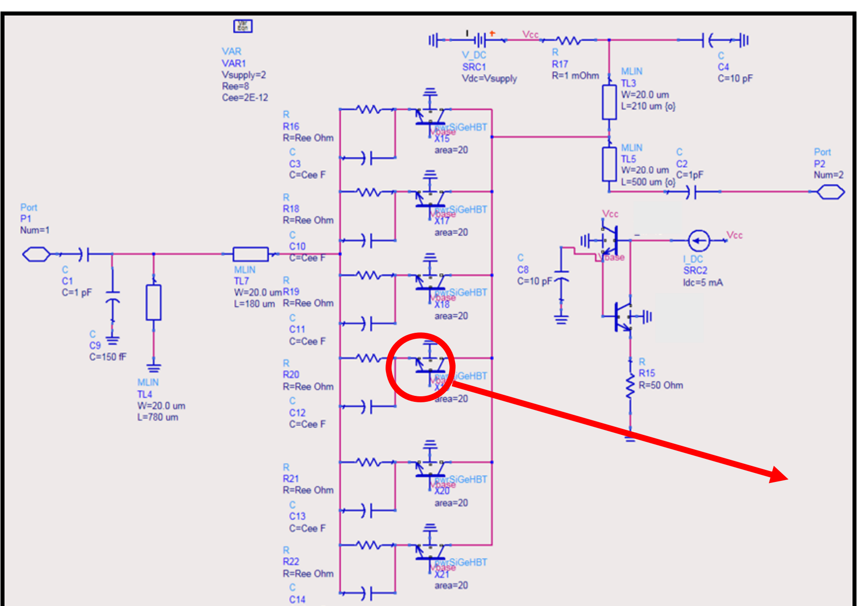


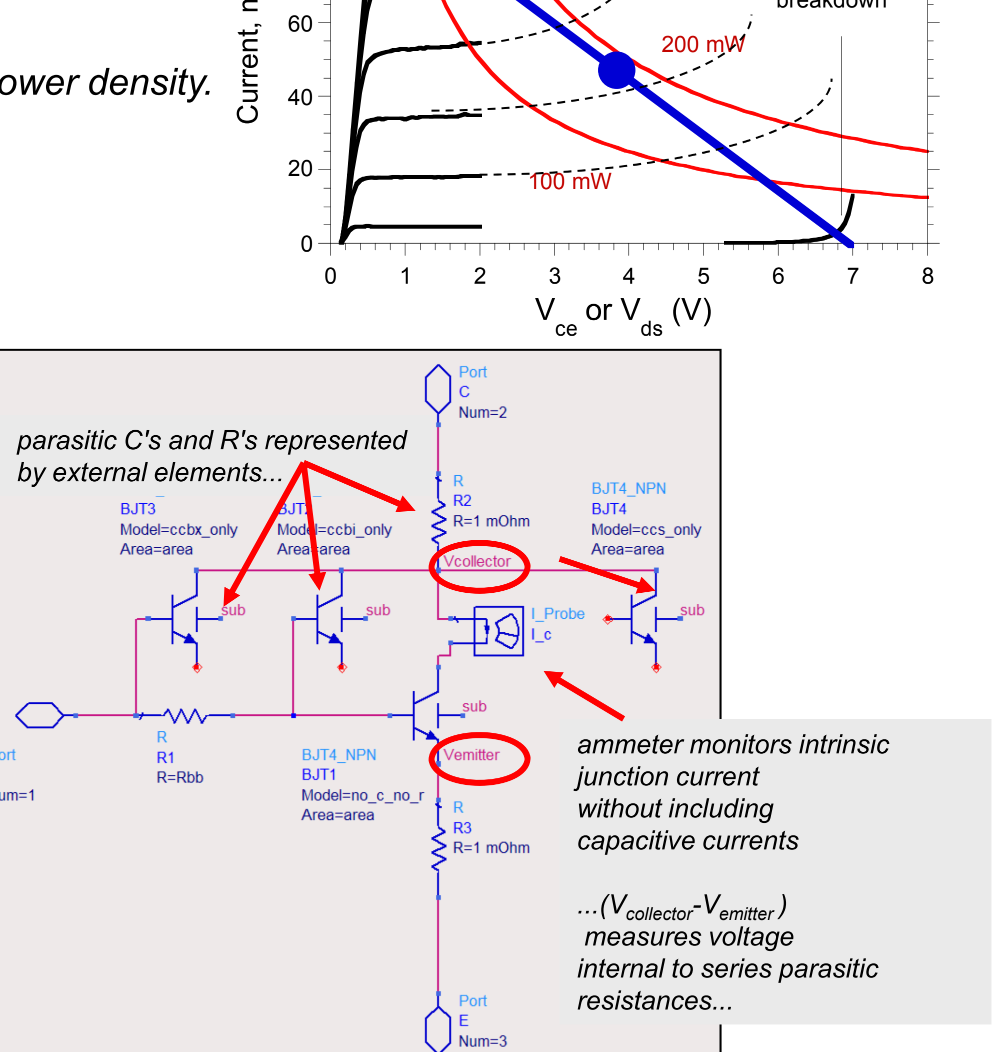
Note: simple gain-tuned amplifiers → limited applications
Transmitters need power amplifiers: need output loadline-match, not gain-match
Receivers need low-noise amplifiers: need input noise-match, not gain-match

Power Amplifier Design (Cripps method)

For maximum saturated output power,
& maximum efficiency
device intrinsic output must see
optimum loadline set by:
breakdown, maximum current, maximum power density.

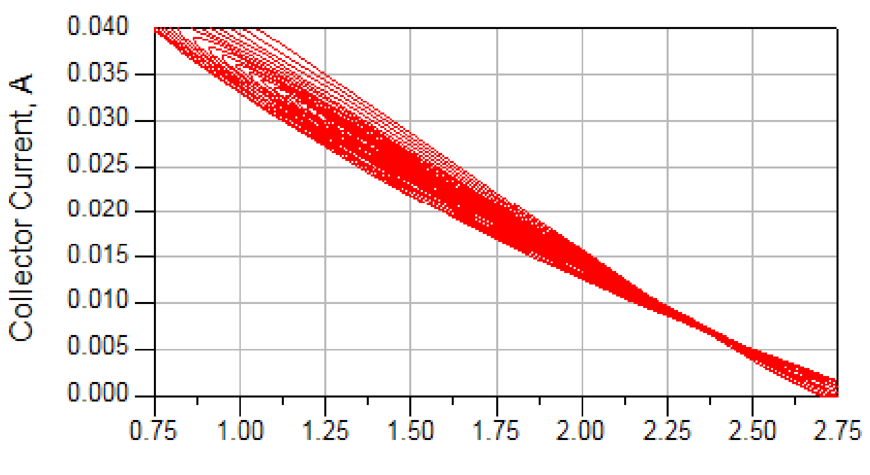
$$P_{max} = (1/8)(V_{max} - V_{min})I_{max}$$



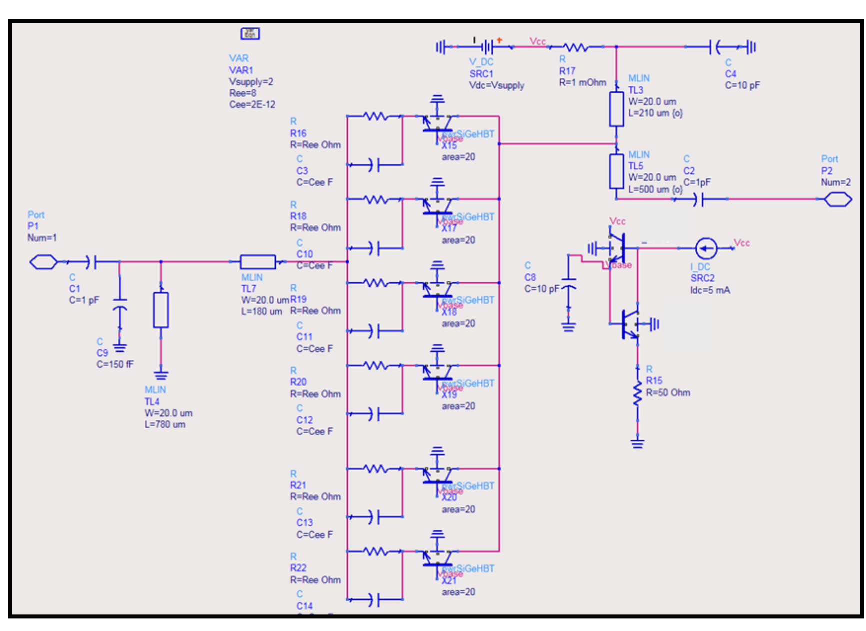


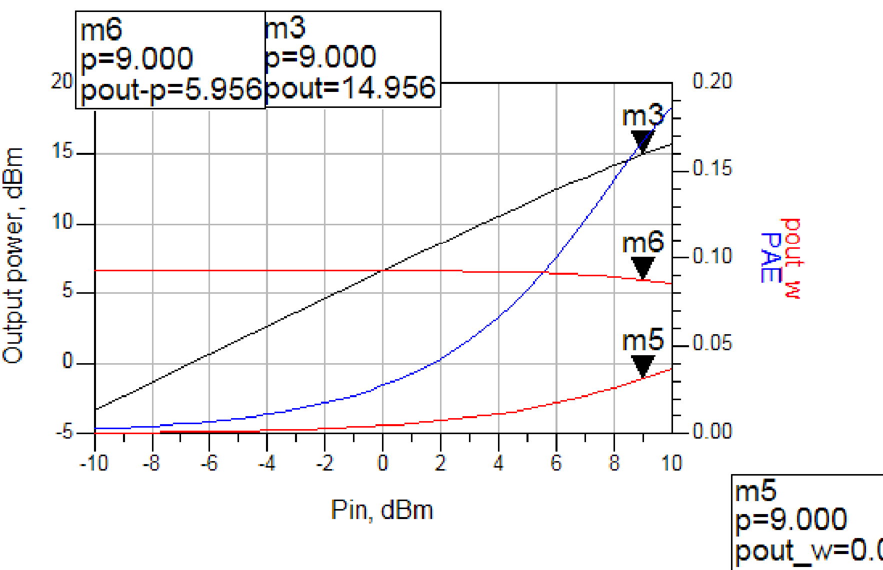
Power Amplifier Design (Cripps Method)

Design steps are
1) input stabilization (in-band)
2) output tuning for correct load-line
3) input tuning (match)
4) out-of-band stabilization

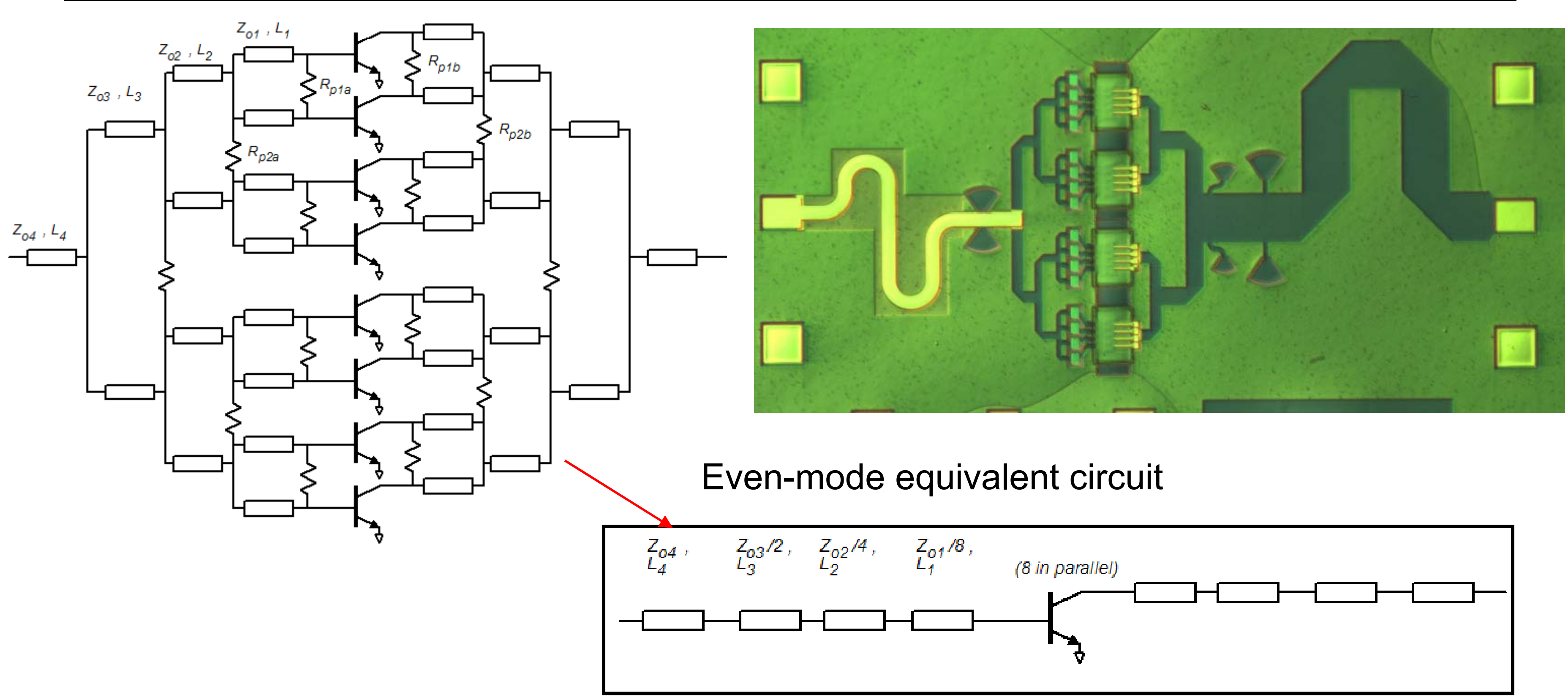


Example: 60 GHz, 30 mW PA, 130 nm BiCMOS





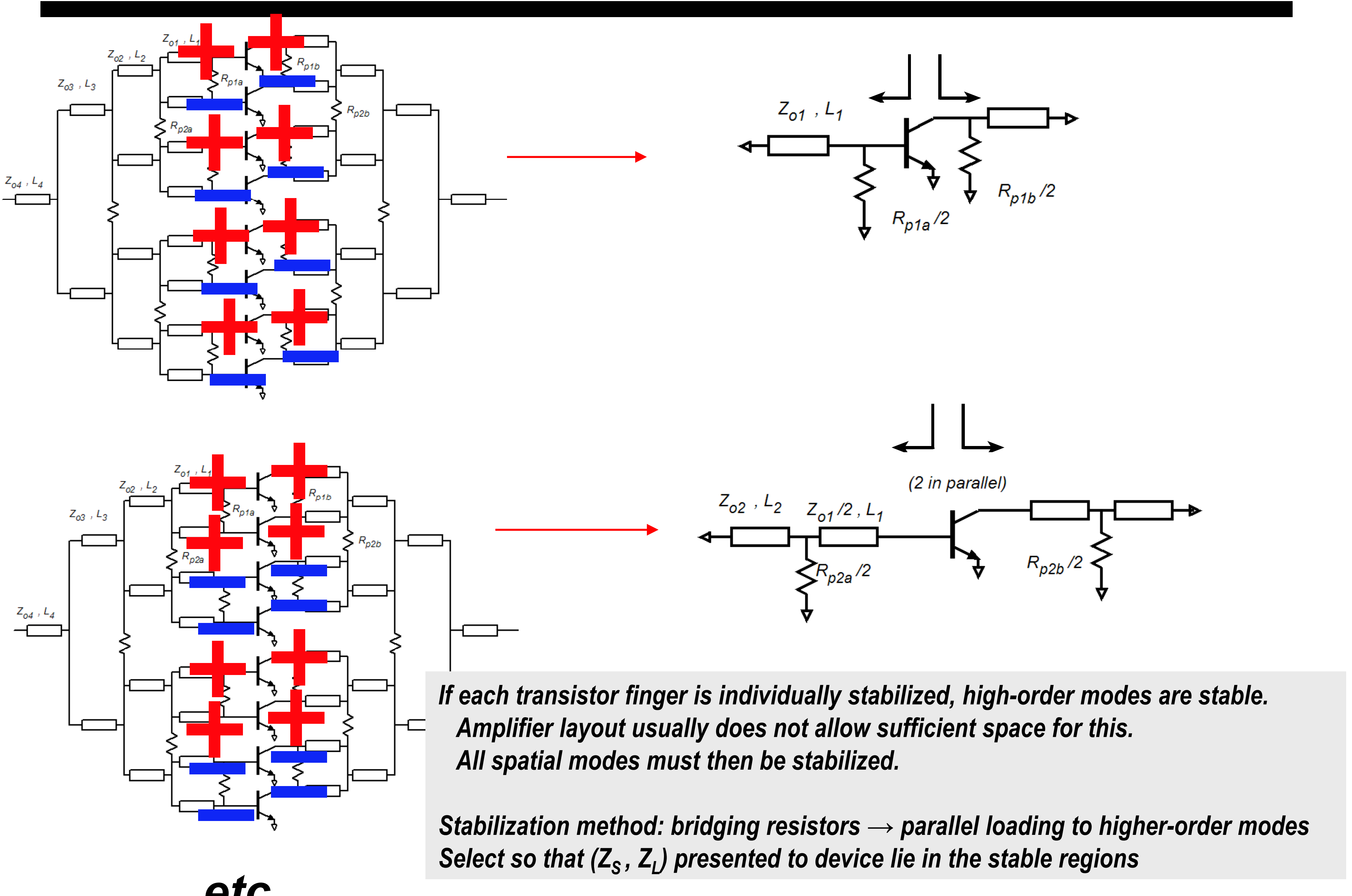
Design: Multi-Finger Power Amplifiers: Even-mode method



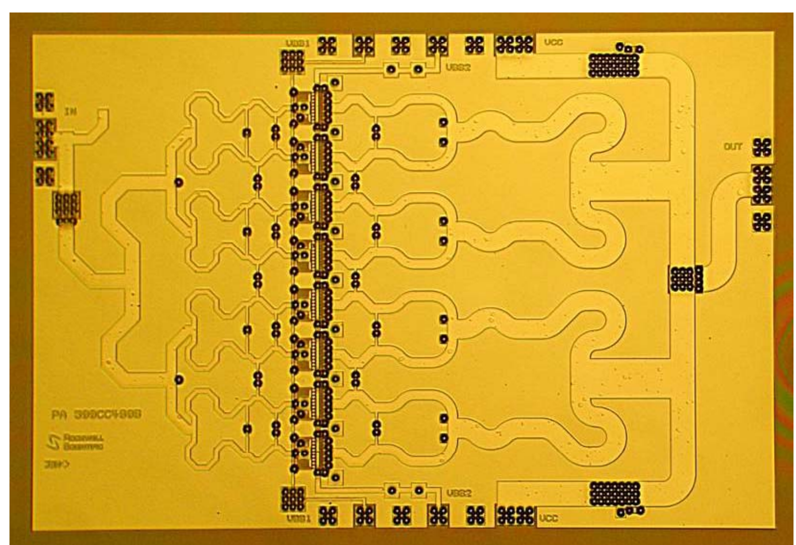
-- Most multi-finger amplifiers do not use Wilkinson combiners: lines are too long
Even-mode equivalent circuit maps combined design into single-device design
Final design tuning (E&M simulation) with full circuit model

This method explicitly models all feed parasitics in a large multi-finger transistor
<u>MUCH</u> more reliable than using single lumped model for multi-finger device

Design: Multi-Finger Amplifiers: spatial mode instabilities

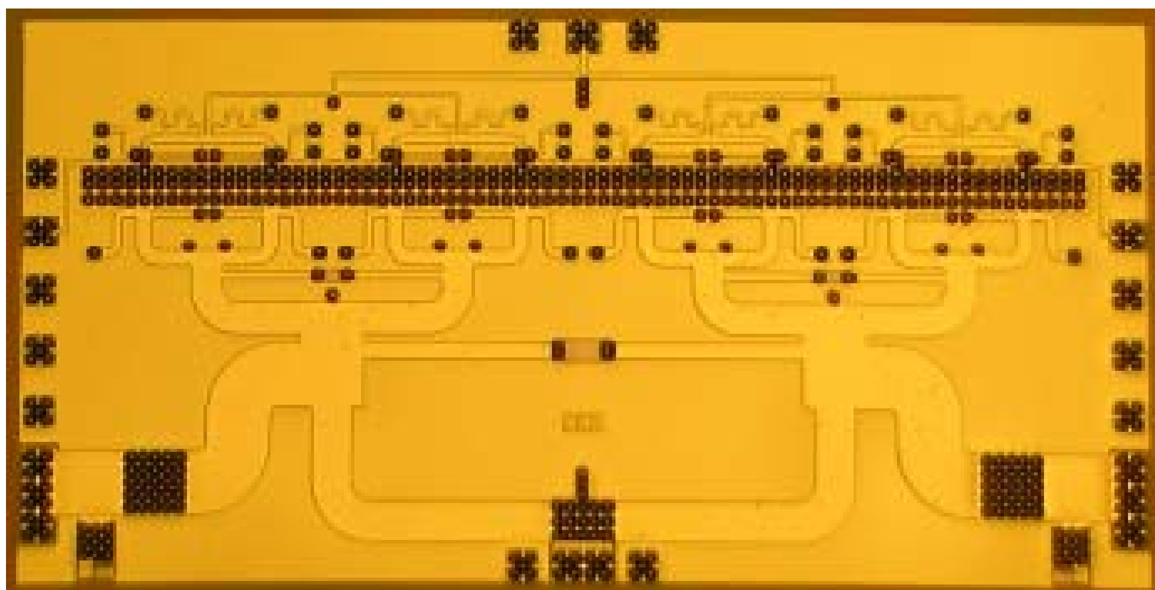


Design: Multi-Finger Amplifiers: Layout Examples



mm-wave InP HBT power amplifier - Rockwell

W-band InP HBT power amplifier - UCSB



mm-wave InP HBT power amplifier - Rockwell

Low-Noise Amplifier Design-- device model

Basic model : Van der Ziel

$$S_{VV,R_g} = 4kTR_g \quad (V^2/Hz)$$

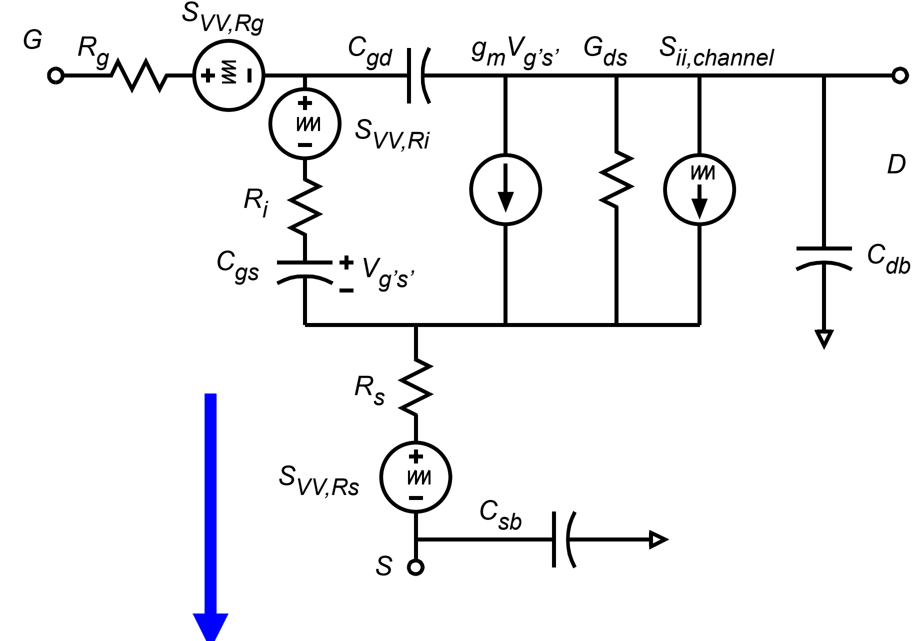
$$S_{VV,R_i} = 4kTR_i \quad (V^2/Hz)$$

$$S_{VV,R_s} = 4kTR_s \quad (V^2/Hz)$$

$$S_{II,channel} = 4kT\Gamma g_m \quad (A^2/Hz)$$

$$\Gamma = \begin{cases} 2/3 : \text{long channel, constant mobility} \\ > 2/3 \text{ under high field} \end{cases}$$

Cross spectral - densities can be neglected (B. Hughes, IEEE Trans MTT)



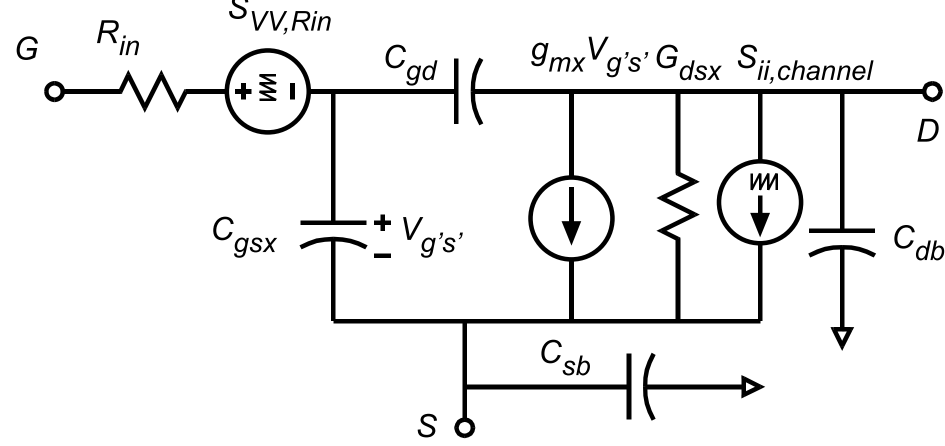
Simplified noise model

$$S_{VV,R_{in}} = 4kTR_{in} \quad (V^2/Hz)$$

$$S_{II,channel} = 4kT\Gamma' g_m$$

$$\Gamma' \to \Gamma \text{ as } g_mR_s \to 0$$

$$\Gamma' \to 1 \text{ as } g_mR_s \to \infty$$



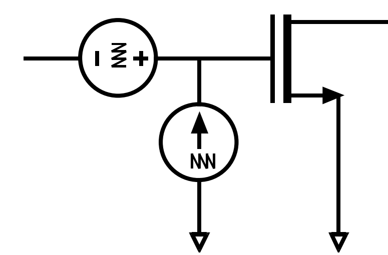
Low-Noise Amplifier Design-- sketch of steps in F_{min} calculation

Total input noise voltage & current spectal densities :

$$S_{E_n}(f) = 4kTR_{in} + \frac{4kT\Gamma}{g_m}\left(1 + (2\pi f C_{gs})^2 R_{in}^2\right) \quad (V^2/Hz)$$

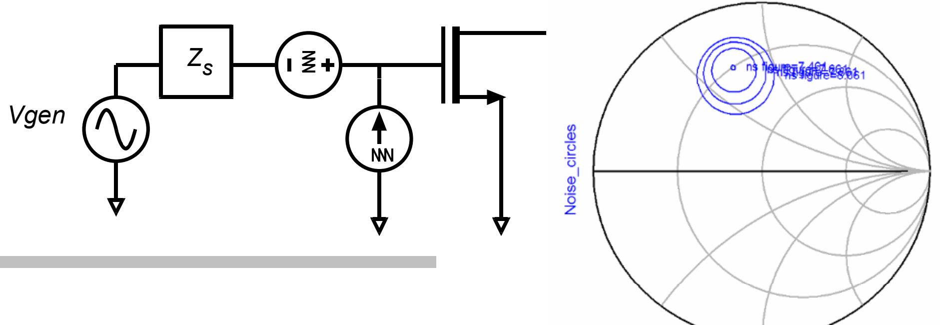
$$S_{I_n}(f) = \frac{4kT\Gamma}{g_m}(2\pi f C_{gs})^2 \quad (A^2/Hz)$$

$$S_{E_n I_n}(f) = \frac{4kT\Gamma}{g_m}(1 + j2\pi f C_{gs} R_{in})(j2\pi f C_{gs})^* \quad (V \times A/Hz)$$



Noise figure with a particular source impedance :

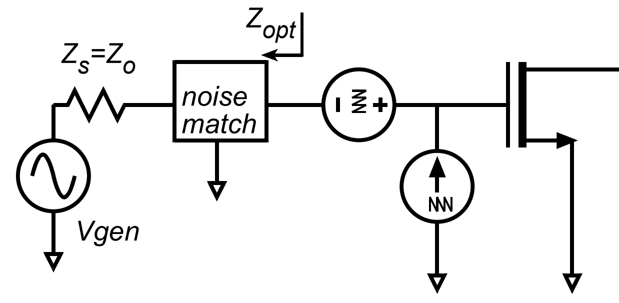
$$F = 1 + \frac{S_{E_n} + |Z_s|^2 S_{I_n} + 2 \cdot \mathrm{Re}(Z_s^* S_{E_n I_n})}{4kT\,\mathrm{Re}(Z_s)}$$



Minimum noise figure

$$F_{\min} = 1 + \frac{1}{4kT}\left[2\sqrt{S_{E_n} S_{I_n} - (\mathrm{Im}[S_{E_n I_n}])^2} + 2\,\mathrm{Re}[S_{E_n I_n}]\right]$$

$$Z_{opt} = R_{opt} + jX_{opt} = \sqrt{\frac{S_{E_n}}{S_{I_n}} - \left(\frac{\mathrm{Im}[S_{E_n I_n}]}{S_{I_n}}\right)^2} - j\frac{\mathrm{Im}[S_{E_n I_n}]}{S_{I_n}}$$



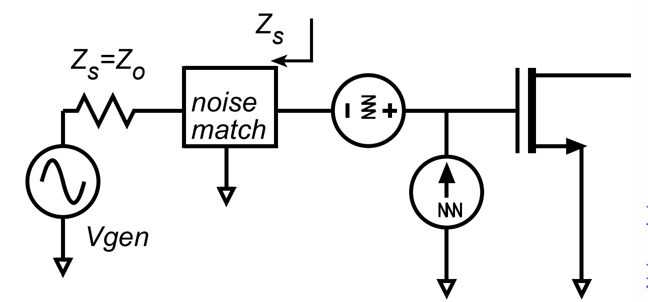
$\rightarrow$ Fukui Expression (rough)

$$F_{\min} \sim 1 + 2\sqrt{\Gamma(R_s + R_g + R_i) g_m} \cdot \left(\frac{f_{signal}}{f_\tau}\right)$$

$$Z_{opt} \sim \sqrt{\frac{R_s + R_g + R_i}{\Gamma g_{mx}}} \cdot \left(\frac{f_\tau}{f_{signal}}\right) + \frac{1}{j2\pi f_{signal} C_{gs}}$$

Low-Noise Amplifier Design

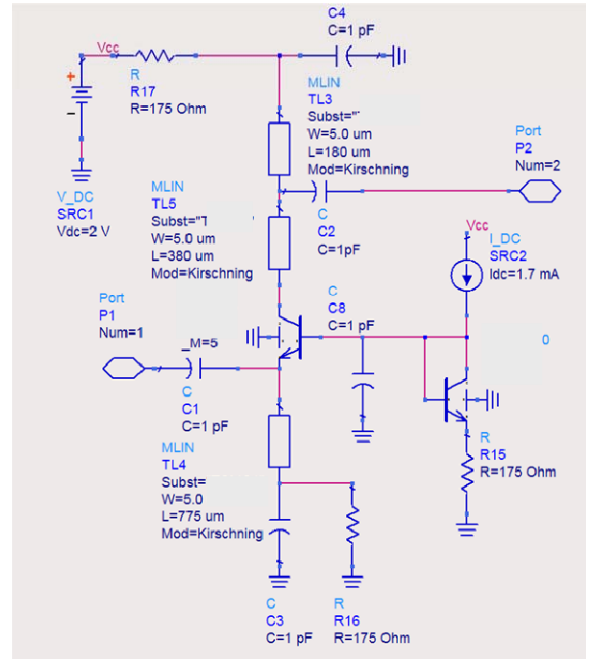
Design steps are
1) output stabilization (in-band)
2) input tuning for F_{min}
3) output tuning (match)
4) out-of-band stabilization

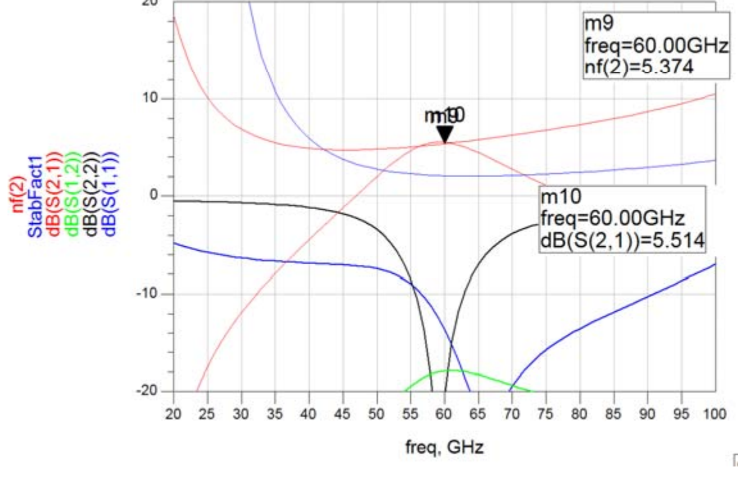


Noise and Available Gain Circles

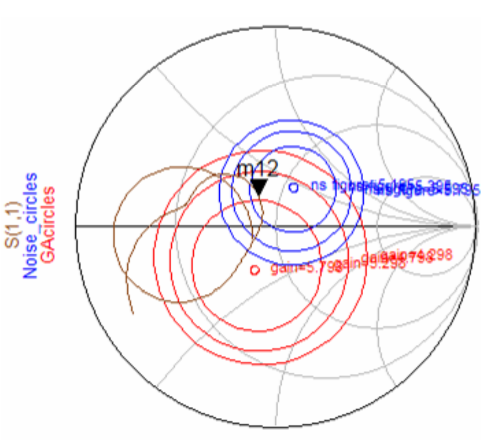
Discrepancy in input noise-match & gain-match
can be reduced by adding source inductance (R. Van Tuyl)

Example: 60 GHz, LNA, 130 nm BiCMOS

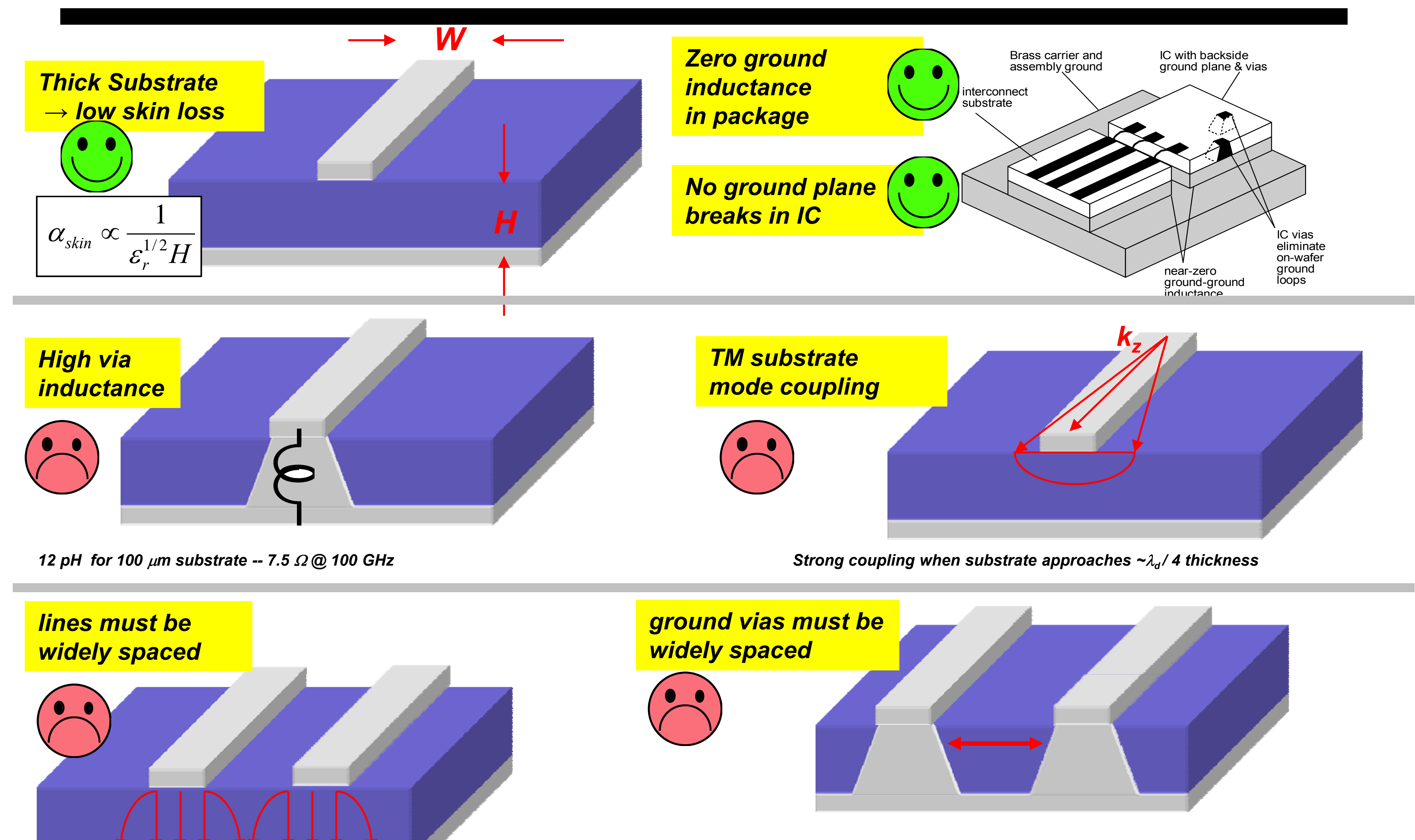




gain & noise circles after input matching
note compromise between gain & noise tune



III-V MIMIC Interconnects -- Classic Substrate Microstrip

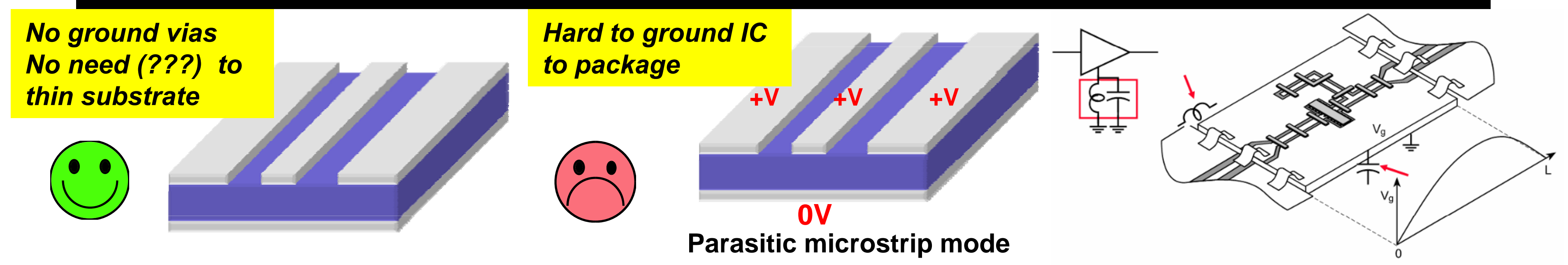


all factors require very thin substrates for >100 GHz ICs
→ lapping to ~50 μm substrate thickness typical for 100+ GHz

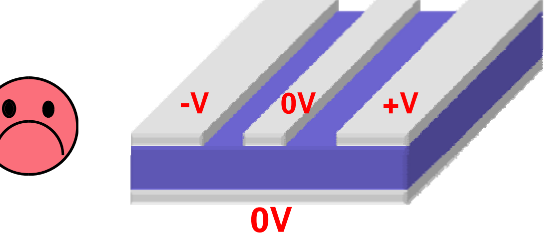
Coplanar Waveguide

No ground vias
No need (???) to thin substrate

Hard to ground IC to package



ground plane breaks → loss of ground integrity



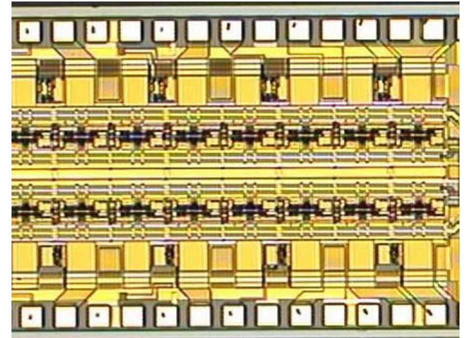
substrate mode coupling or substrate losses

k_z

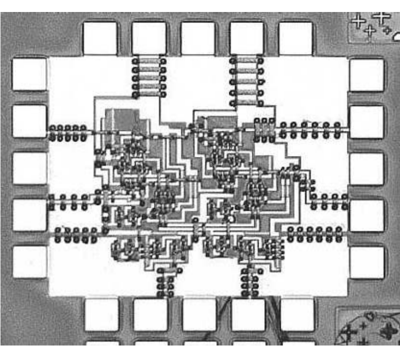
III-V: semi-insulating substrate→ substrate mode coupling

Silicon conducting substrate → substrate conductivity losses

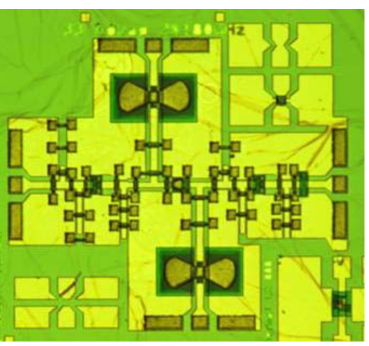
Repairing ground plane with ground straps is effective only in simple ICs
In more complex CPW ICs, ground plane rapidly vanishes
→ common-lead inductance → strong circuit-circuit coupling



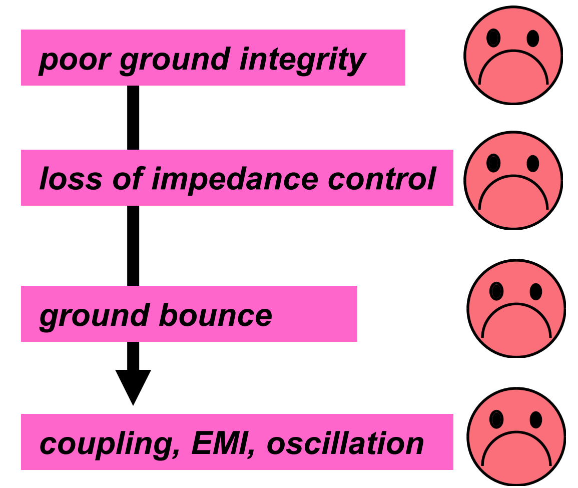
40 Gb/s differential TWA modulator driver
note CPW lines, fragmented ground plane



35 GHz master-slave latch in CPW
note fragmented ground plane

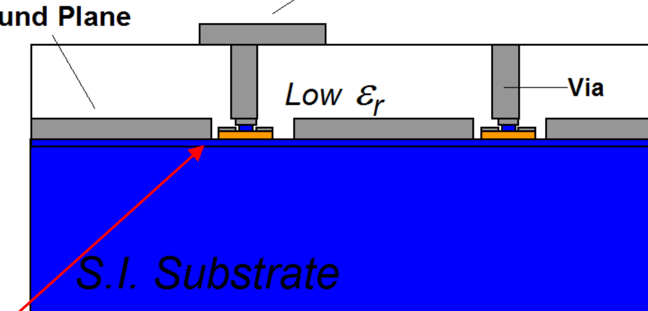


175 GHz tuned amplifier in CPW
note fragmented ground plane



III-V MIMIC Interconnects -- Thin-Film Microstrip

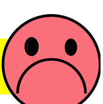
narrow line spacing → IC density

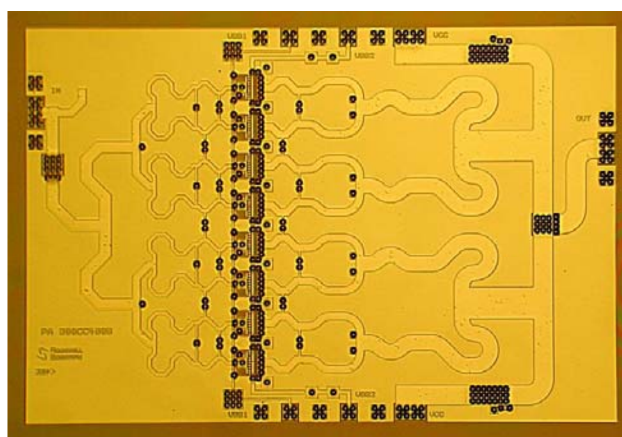


no substrate radiation, no substrate losses

fewer breaks in ground plane than CPW

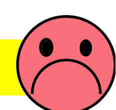
... but ground breaks at device placements





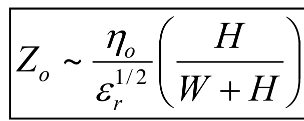
InP mm-wave PA (Rockwell)

still have problem with package grounding

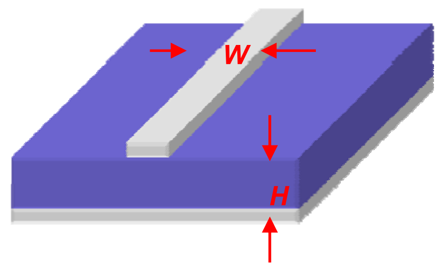


...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines

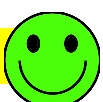


$$Z_o \sim \frac{\eta_o}{\varepsilon_r^{1/2}}\left(\frac{H}{W+H}\right)$$

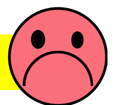


III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

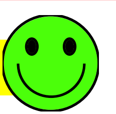
narrow line spacing → IC density



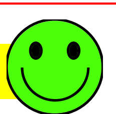
Some substrate radiation / substrate losses



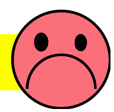
No breaks in ground plane



... no ground breaks at device placements

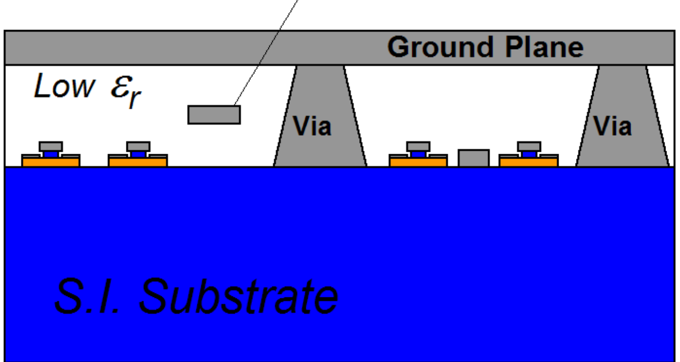


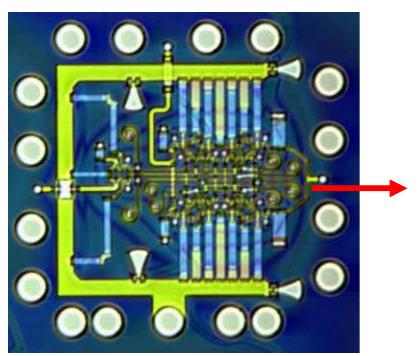
still have problem with package grounding

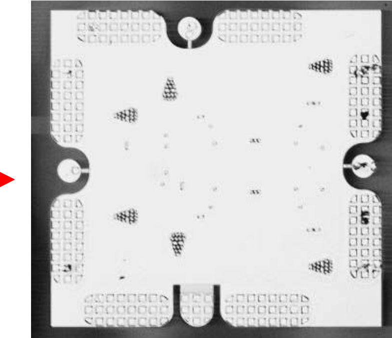


...need to flip-chip bond

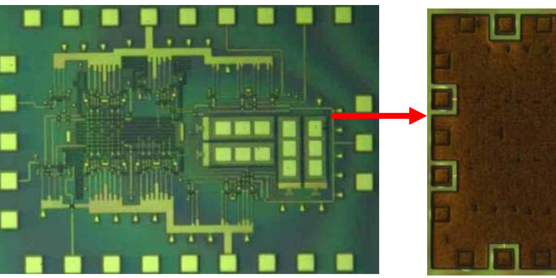
thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines

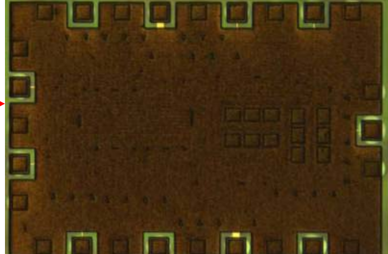






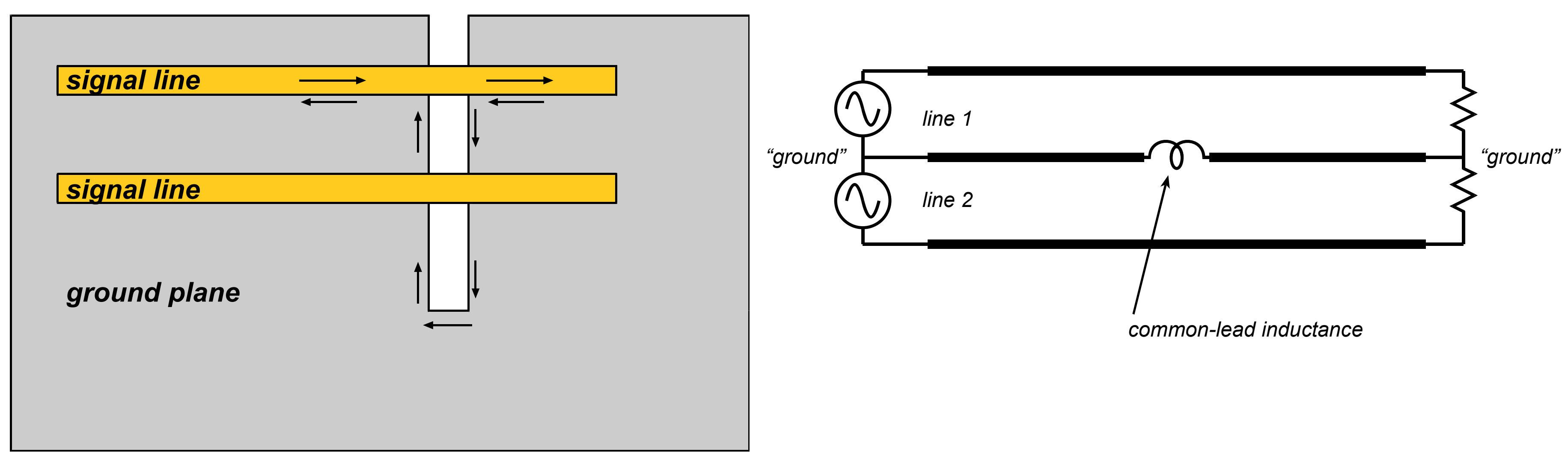
InP 150 GHz master-slave latch



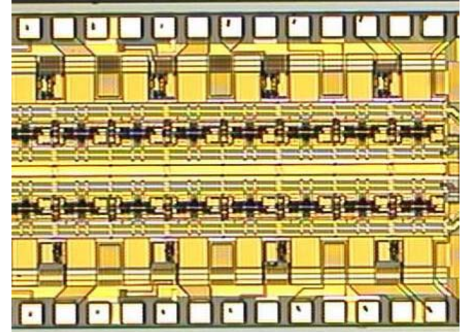


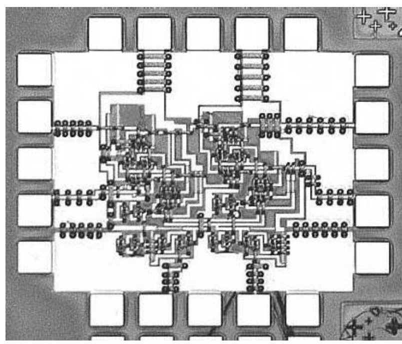
InP 8 GHz clock rate delta-sigma ADC

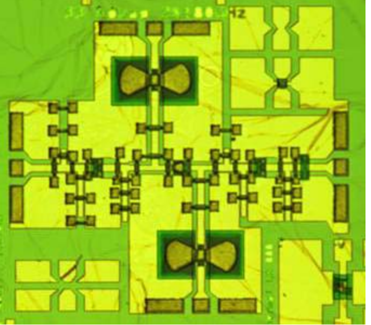
If It Has Breaks, It Is Not A Ground Plane !



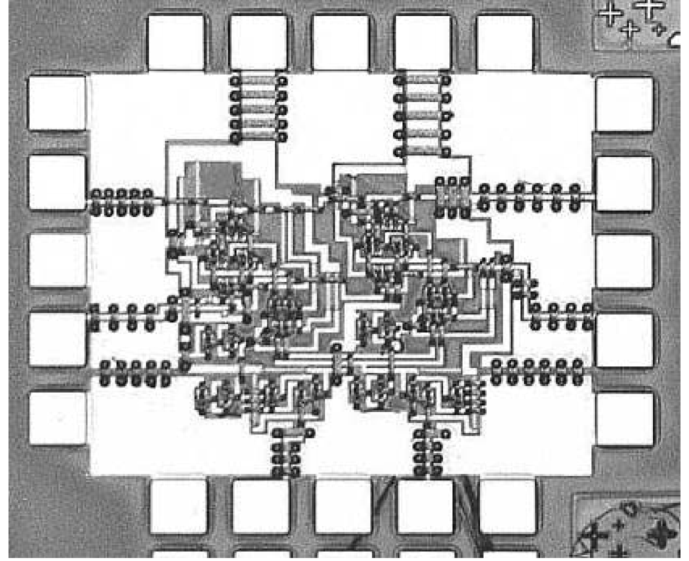
coupling / EMI due to poor ground system integrity is common in high-frequency systems
whether on PC boards
...or on ICs.



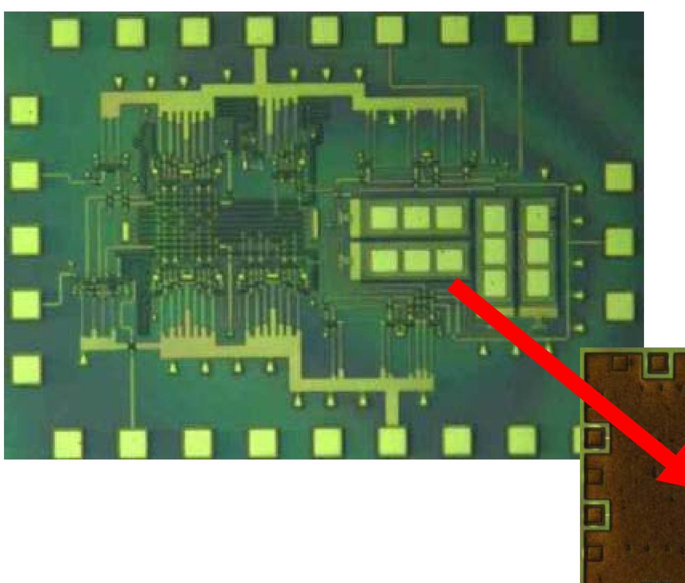




No clean ground return ? → interconnects can't be modeled !



35 GHz static divider
- *interconnects have no clear local ground return*
- *interconnect inductance is non-local*
- *interconnect inductance has no compact model*

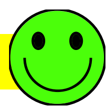


8 GHz clock-rate delta-sigma ADC
- *thin-film microstrip wiring*
- *every interconnect can be modeled as microstrip*
- *some interconnects are terminated in their Zo*
- *some interconnects are not terminated*
- *...but ALL are precisely modeled*

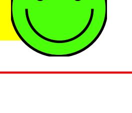
InP 8 GHz clock rate delta-sigma ADC

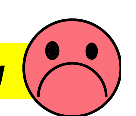
VLSI mm-Wave Interconnects with Ground Integrity

narrow line spacing → IC density

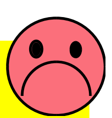
no substrate radiation, no substrate losses 

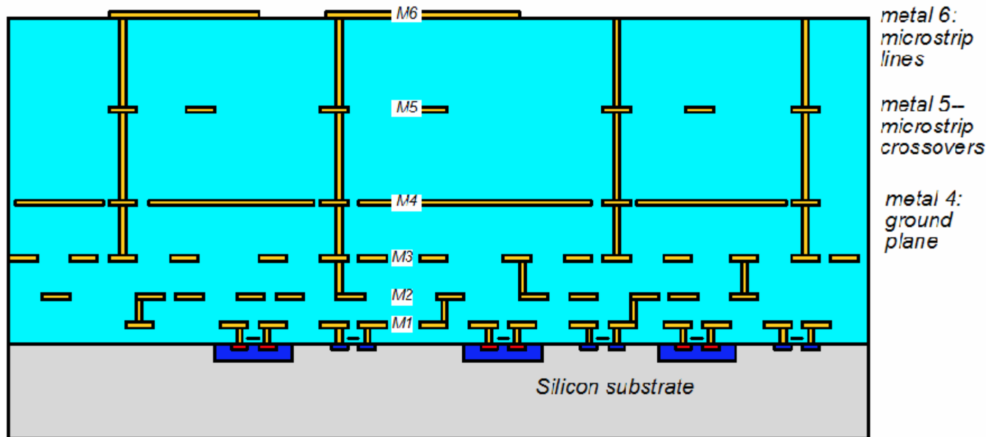
negligible breaks in ground plane

negligible ground breaks @ device placemen 

still have problem with package grounding 

...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines 

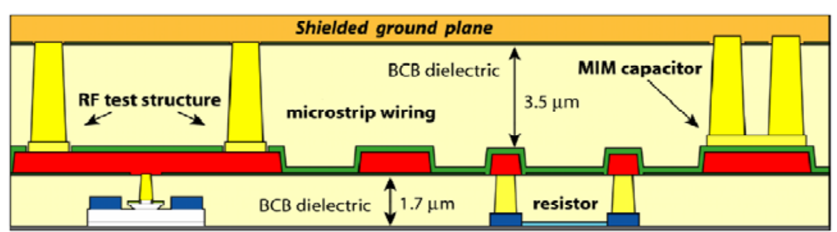


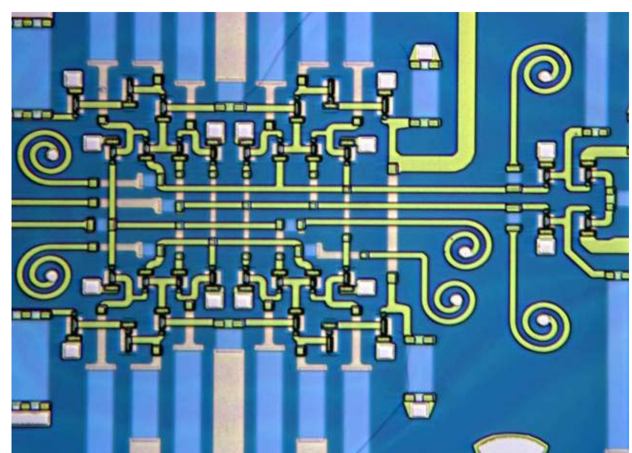
Example: 150 GHz Master-Slave Latch

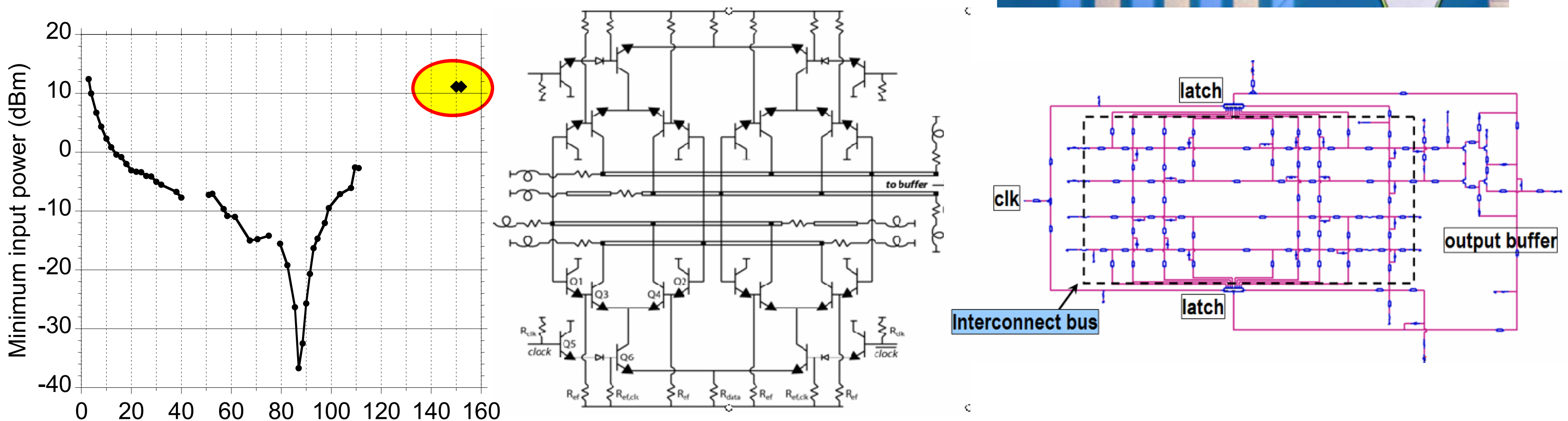
Device Technology:
500 nm InP HBT

Interconnects :
inverted thin-film microstrip

***Design**:*
All lines modeled as microstrip lines
representative lines simulated in Agilent / Momentum
fit to simple lossy line model (loss, Zo, velocity)







Example: 20 GHz DDFS Design (Rockwell)

designs in progress: MJ Choe

***design target**:*
20 GHz clock rate

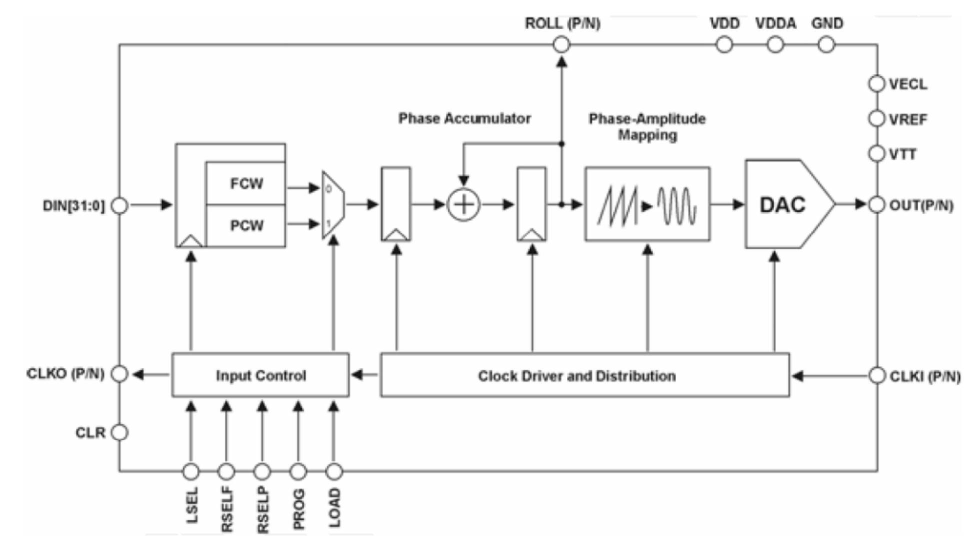
***circuit topology**:*
ECL

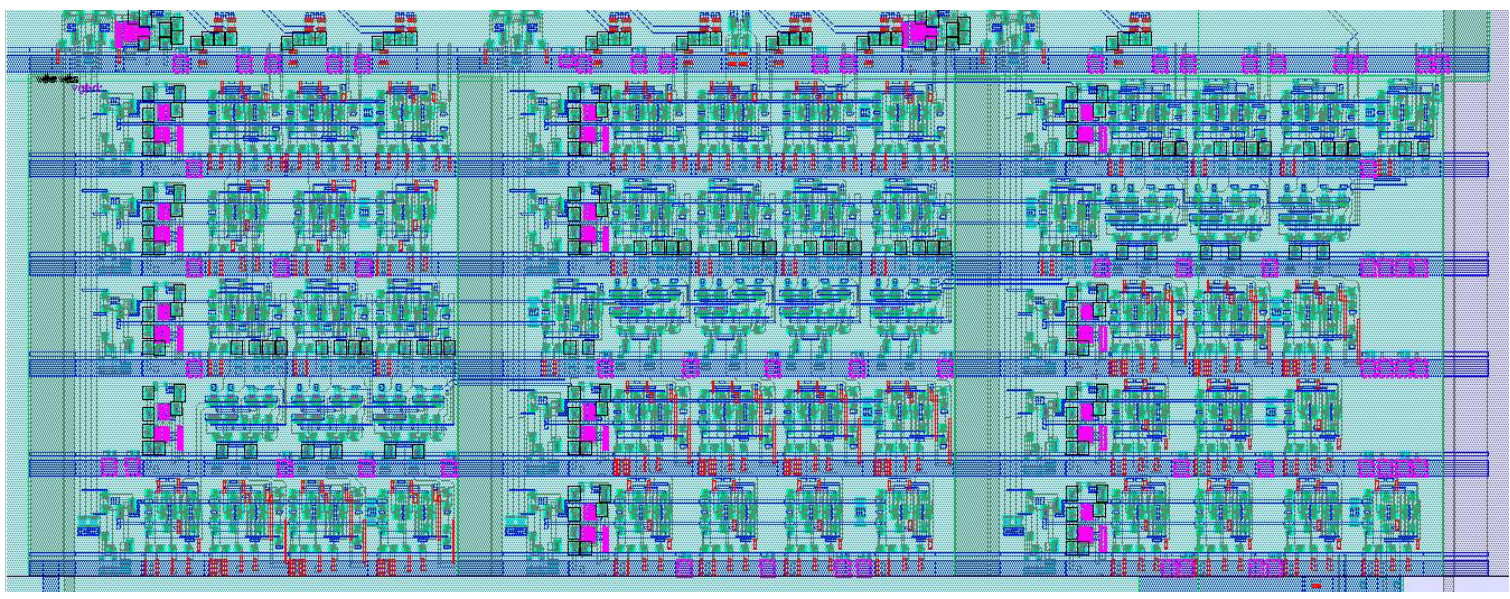
***device technology**:*
350 GHz (500 nm) InP HBT (Rockwell)

***Interconnect technology**:*
inverted thin-film microstrip throughout
→ all lines are controlled-impedance

<u>shorter lines:</u>
unterminated, but modeled

<u>longer lines:</u>
modeled and terminated





Summary

- At 90-nm or below, CMOS can be a cost-effective choice for highly integrated mm-wave circuits
- Consideration for optimizing device layout and biasing are very similar for mm-wave and RF
- Pre-characterized cell-based mm-wave design flow will be a key enabler

References on other mm-Wave CMOS Efforts

- Prof. B. Brodersen and Prof. A. Niknejad – "Design considerations for 60 GHz CMOS radios," ***IEEE Communications Magazine***, Dec. 2004.
- Prof. A. Hajimiri – "A fully integrated 24-GHz phased-array transmitter in CMOS," ***IEEE JSSC***, Dec. 2005.
- Prof. B. Razavi – "A 60-GHz CMOS receiver front-end" ***IEEE JSSC***, Jan. 2006.
- Prof. F. Chang – "A 60GHz CMOS VCO using on-chip resonator with embedded artificial dielectric for size, loss, and noise reduction," ***2006 ISSCC***.
- Prof. J. Laskar – "60-GHz direct-conversion gigabit modulator/demodulator on liquid-crystal polymer," ***IEEE TMTT***, Mar. 2006.

In case

of questions