Ultra-Low Resistance Ohmic Contacts to InGaAs/InP

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Very low resistance metal-semiconductor contacts are fundamental to the continued scaling of transistors towards THz bandwidths. The specific emitter contact restivity of heterojunction bipolar transistors (HBTs) and the specific source contact resistivity of III-V field-effect transistors must both decrease in proportion to the inverse square of transistor bandwidth. For both III-V HBTs and FETs, $\sim 1\cdot 10^{-8}\ \Omega\text{-cm}^2$ contact resistivity is required for transistors having simultaneous 1.5 THz f_t and f_{max} [1]. Emitter access resistance also plays a particularly strong role in determining gate delay in bipolar digital ICs [1]. We report extremely low resistance, non-alloyed ohmic contacts to $In_{0.53}Ga_{0.47}As$ with specific contact resistivity (ρ_c) $< 1\cdot 10^{-8}\ \Omega\text{-cm}^2$. We show that these contacts can be formed either *in situ* by metal deposition in the MBE chamber or *ex situ* with better surface cleaning techniques.

We studied two types of *in situ* contacts, contacts in which the metal is deposited in the MBE system without breaking vacuum. This ensures that no oxide is formed at the metal-semiconductor interface. The first approach was to form epitaxial ErAs/ $In_{0.53}Ga_{0.47}As$ semimetal-semiconductor contacts. ErAs can be grown epitaxially on InGaAs. The ErAs/InGaAs interface shows a continuous As sublattice without any broken bonds [2]. The Fermi level of ErAs is estimated to be ~100 meV above the conduction band of InAs [3]. In the second approach, *in situ* electron beam deposited Molybdenum (Mo) contacts to InAs/ $In_{0.53}Ga_{0.47}As$ were studied. The Mo Fermi level will pin above the conduction band of InAs [4]. Additionally, we studied *ex situ* TiW/$In_{0.53}Ga_{0.47}As$ contacts. In these, the wafer is grown by MBE and then removed from vacuum. The InGaAs surface was then oxidized by a UV ozone treatment, and the oxide was etched off in concentrated NH_4OH before depositing TiW contact metal on the wafer.

All the samples were grown by solid-source MBE on (100) semi-insulating InP substrate. The layer structures are shown in Fig. 1. For the *in situ* contact samples, 40 nm of Mo was deposited in an electron beam deposition system connected to MBE under ultra high vacuum. The Mo was deposited as a cap layer onto the ErAs to prevent its oxidation. The channel doping and thickness were chosen such that 1-D current-flow condition is satisfied in the transmission line measurement (TLM). The active carrier concentrations were confirmed by Hall measurements. The samples were then processed into TLM structures for contact resistance measurement using standard photolithography. The Mo and TiW layers were dry etched in SF_6/Ar with Ni as etch mask and the structures were isolated by wet etching the semiconductor (Fig. 2). The TLM pad spacing ranged from 0.6 µm to 25 µm. The pad spacings were verified by scanning electron microscopy imaging. The TLM geometry was designed such that at the smallest spacing the contact resistance is at least 50 % of the total measured resistance. All the contacts show linear Ohmic I-V behavior as formed. Fig. 3 plots the measured resistance vs. the pad spacing in the TLM structures. A four point probe method was employed in the measurement to minimize parasitic resistances. From the slope and intercept of the line, the sheet and contact resistances were calculated. The specific contact resistivities for the *in situ* ErAs/InAs, *in situ* Mo/InAs and *ex situ* TiW/ $In_{0.53}Ga_{0.47}As$ were $1.5\cdot 10^{-8}\ \Omega\text{-cm}^2$, $5\cdot 10^{-9}\ \Omega\text{-cm}^2$ and $7\cdot 10^{-9}\ \Omega\text{-cm}^2$ respectively. All the samples showed ~15-18 Ω sheet resistance. The transfer lengths for *in situ* ErAs/InAs, *in situ* Mo/InAs, and *ex situ* InGaAs contacts were 300 nm, 175 nm, and 190 nm, respectively.

Thermal stability studies on the contacts were carried out by annealing the contacts under N_2 flow for 1 minute at various temperatures. Fig. 4 plots the specific contact resistivity as a function of temperature. For *in situ* Mo/InAs, and *ex situ* TiW/InGaAs contacts the specific contact resistivity remains $<1\cdot 10^{-8}\ \Omega\text{-cm}^2$ even after annealing at 500 C. The ErAs contact resistance increases with annealing temperature. This could be due to reaction of ErAs with Mo, or lateral oxidation of ErAs. SIMS depth analysis on the contacts is shown in Fig 5. The refractory metals TiW and Mo are very effective as diffusion barrier to Au and Ti.

We show for the first time that extremely low *in situ* metal contacts can be formed to (In,Ga)As on InP. We also show that it is possible to form ultra low resistance *ex situ* contacts by improved surface treatment. However, unlike *in situ* contacts, *ex situ* contacts are very sensitive to surface preparation. Similar contact resistivities to InAs on GaAs were reported by Nittono *et al.* [5]. To our knowledge this is the first time such low metal-semiconductor contacts have been demonstrated in $In_{0.53}Ga_{0.47}As$ system that does not deteriorate at least upto 500 C. These thermally stable, extremely low resistance, Ohmic contacts are an enabling technology for THz bandwidth InGaAs/InP HBTs, mm wave InGaAs HEMT technologies, and the evolving III-V MOSFET technologies.

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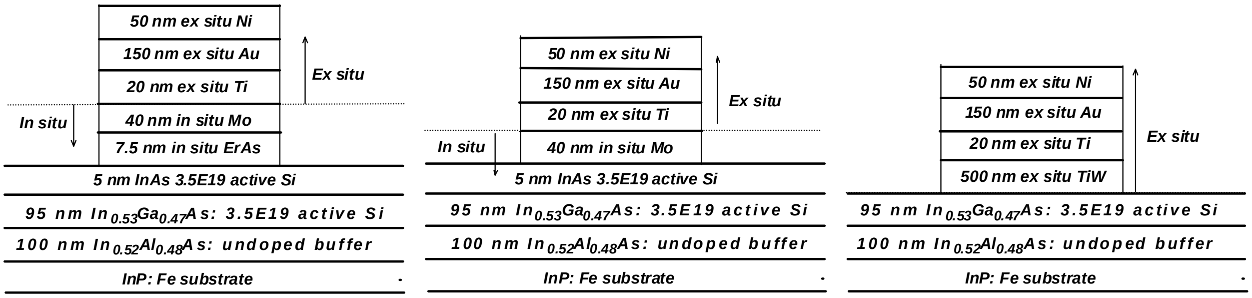
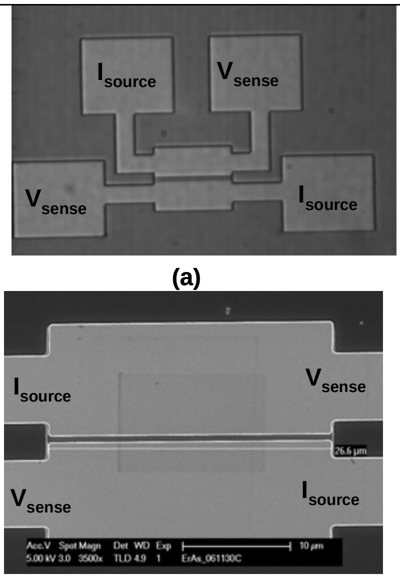


(a) **(b)** **(c)**

Fig. 1 : Cross-section schematic of the metal-semiconductor contact layer structure grown by solid source MBE, (a) *in situ* ErAs/InAs contact, (b) *in situ* Mo/InAs contact and (c) *ex situ* TiW/InGaAs contact. The Mo was deposited in an electron beam deposition system connected to MBE under ultra high vacuum. TiW is sputtered *ex situ* for the TiW/InGaAs contact.



(b)

Fig. 2: (a) Optical micrograph and (b) SEM image of the 600 nm gap TLM. A thick interconnect metal (Ti/Au/Ni) was used to minimize metal resistance.

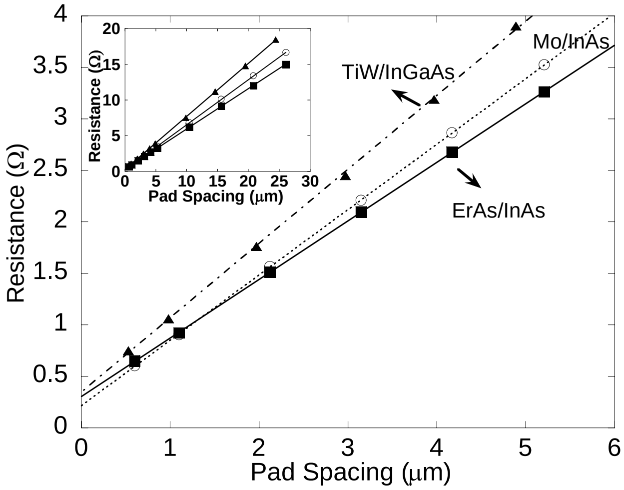


Fig. 3: Measured resistance vs. pad spacing for the contacts. At the smallest gap of 0.6 µm the contact resistance term is at least 50 % of the total measured resistance. The inset plots measured resistance vs. pad spacing ranging from 0.6 µm to 26 µm.

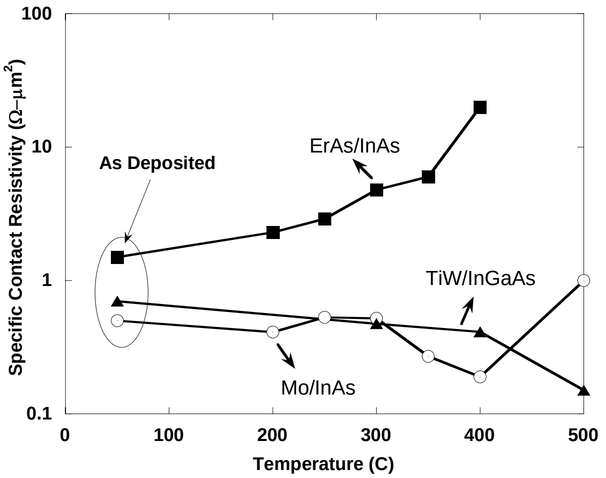


Fig 3: Specific contact resistivity as a function of annealing temperature.

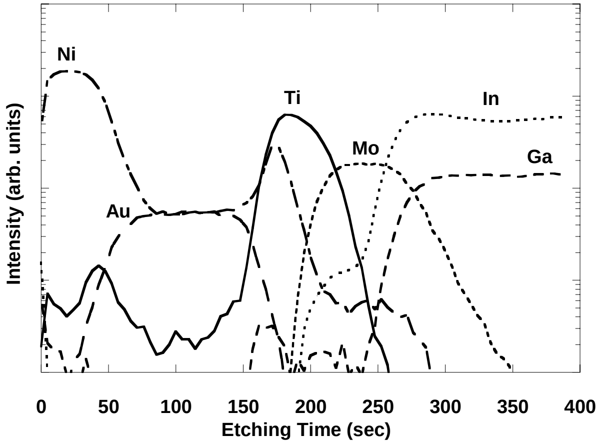


Fig 4: SIMS depth profile of Mo/InAs contact annealed at 400 C.