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THz Bipolar Transistor Circuits: Technical Feasibility, Technology Development, Integrated Circuit Results

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The End (of Moore's Law) is Near (?)

It's a great time to be working on electronics !

Things to work on:

InP HEMTs & HBTs: extend (f_τ, f_{max}) to 2-3 THz, build THz ICs

GaN HEMTs: develop V- and W-band power amplifiers

Si MOSFETs: work to keep them scaling past 22 nm

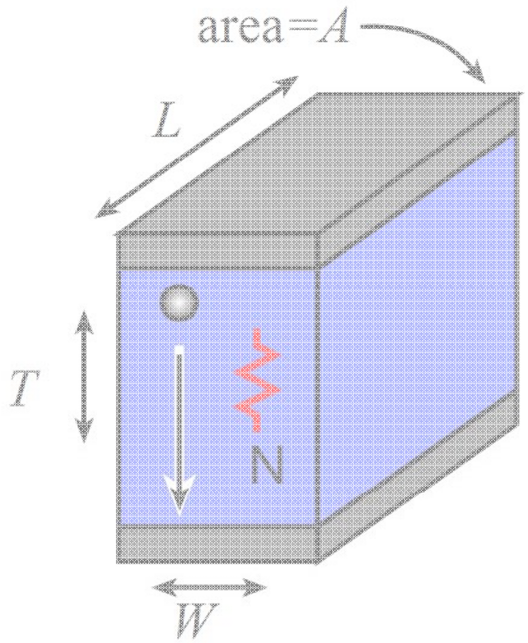
CMOS IC design: build ICs which bury the III-V's

InGaAs MOSFETs: help keep VLSI scaling (maybe)

Scaling for THz Transistors

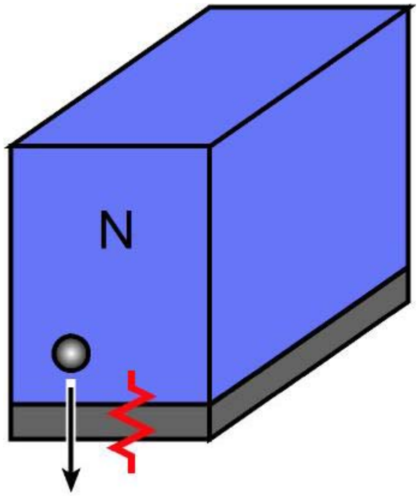
Simple Device Physics: Resistance

bulk resistance



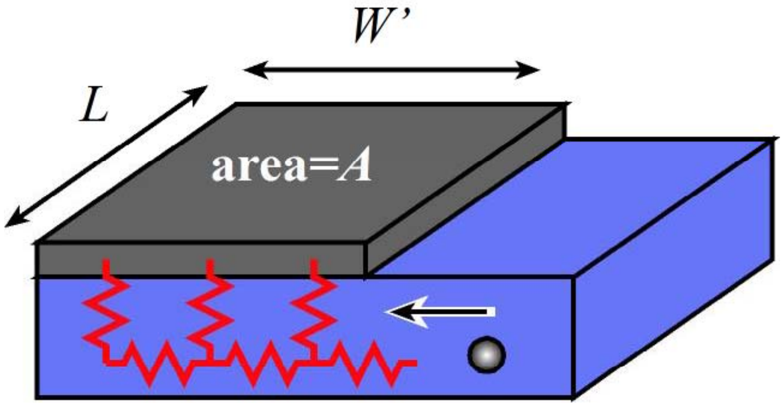
$$R = \frac{\rho_{bulk} \cdot T}{A}$$

contact resistance -perpendicular



$$R = \frac{\rho_{contact}}{A}$$

contact resistance - parallel

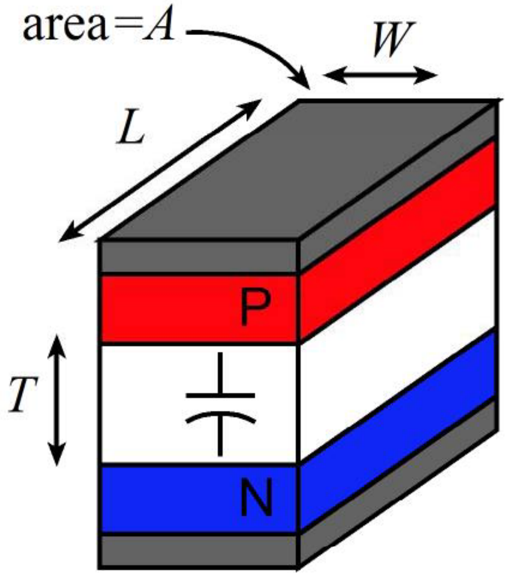


$$R = \frac{\rho_{contact}}{A} + \rho_{sheet} \cdot \frac{W'}{3L}$$

Good approximation for contact widths less than 2 transfer lengths.

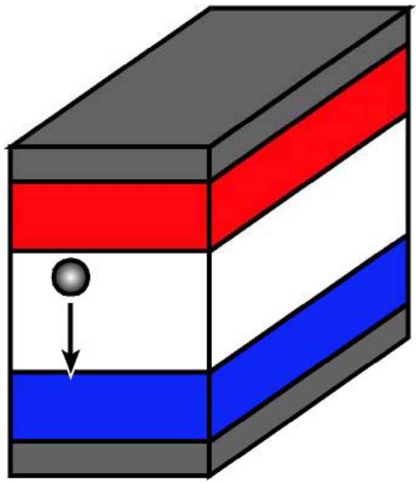
Simple Device Physics: Depletion Layers

capacitance



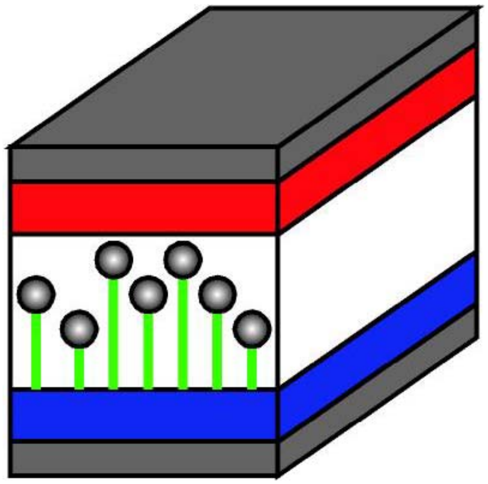
$$C = \varepsilon \cdot \frac{A}{T}$$

transit time



$$\tau = \frac{T}{2v}$$

space-charge limited current



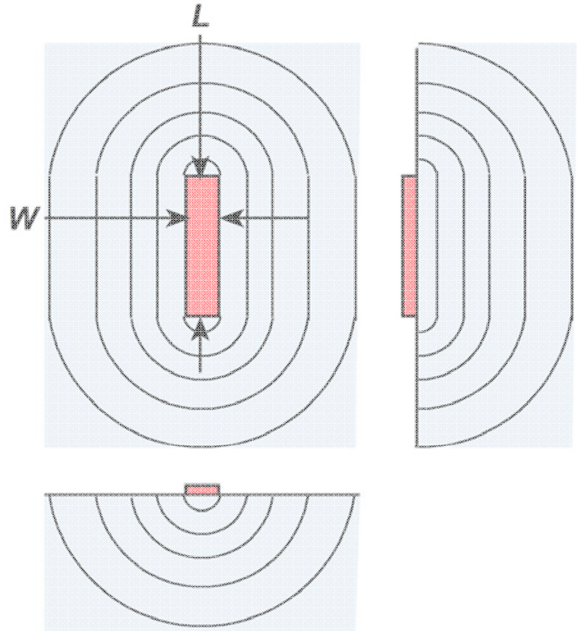
$$\frac{I_{\max}}{A} = \frac{2\varepsilon v}{T^2}\left(V_{applied} + V_{depletion} + 2\phi\right)$$

$$I = C\frac{\Delta V}{\Delta T} \text{ where } \frac{C}{I_{\max}} = \frac{\tau}{V_{applied} + V_{depletion} + 2\phi}$$

Simple Device Physics: Thermal Resistance

Exact

Carslaw & Jaeger 1959



$$R_{th} = \frac{1}{\pi K_{th} L} \sinh^{-1}\left(\frac{L}{W}\right) + \frac{1}{\pi K_{th} W} \sinh^{-1}\left(\frac{W}{L}\right)$$

Long, Narrow Stripe

HBT Emitter, FET Gate

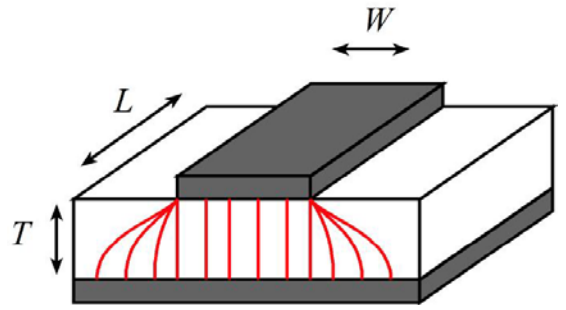
$$R_{th} \cong \underbrace{\frac{1}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)}_{\text{cylindrical heat flow near junction}} + \underbrace{\frac{1}{\pi K_{th} L}}_{\text{spherical heat flow far from junction}}$$

Square (L by L)

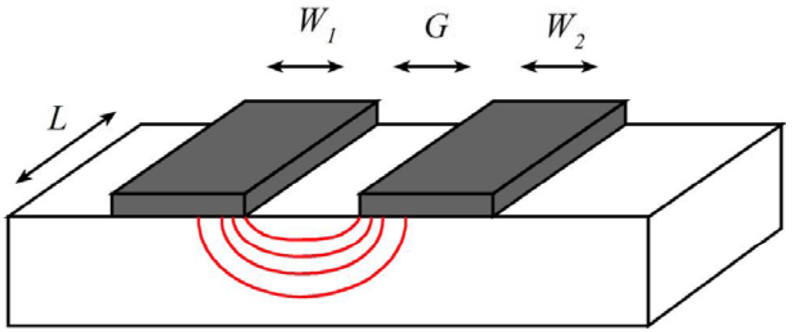
IC on heat sink

$$R_{th} \cong \underbrace{\frac{1}{4 K_{th} L}}_{\text{planar heat flow near surface}} + \underbrace{\frac{1}{\pi K_{th} L}}_{\text{spherical heat flow far from surface}}$$

Simple Device Physics: Fringing Capacitance



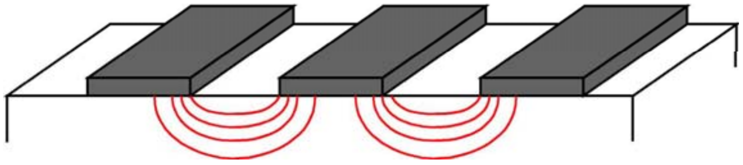
$$\frac{C}{L} \cong \underbrace{\varepsilon \cdot \frac{W}{T}}_{\text{parallel - plate}} + \underbrace{1.5 \cdot \varepsilon}_{\text{fringing}}$$



$$\frac{C}{L} \cong \varepsilon \cdot \left[\begin{array}{l} \text{slowly - varying function} \\ \text{of } \; W_1 / G \text{ and } W_2 / G \end{array} \right]$$

$$\approx (1 \text{ to } 3) \cdot \varepsilon$$

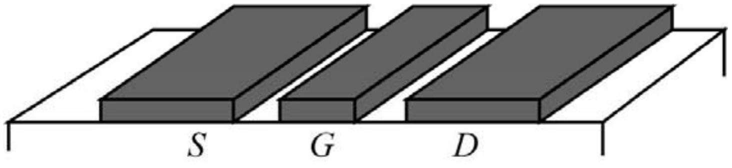
wiring capacitance



$$C / L > \varepsilon$$

VLSI power-delay limits

FET parasitic capacitances

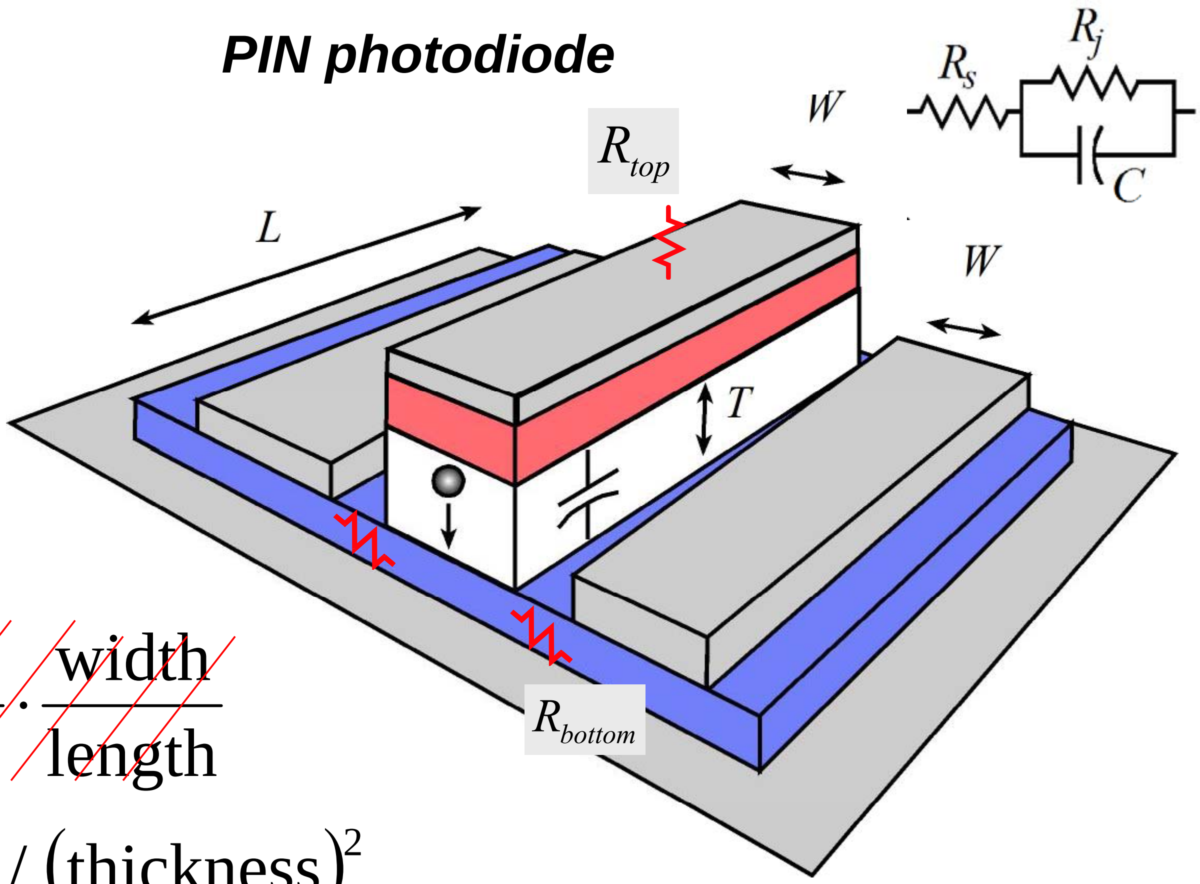


$$C_{parasitic} / L \sim \varepsilon$$

FET scaling constraints

Frequency Limits and Scaling Laws of (most) Electron Devices

PIN photodiode



$$\tau \propto \text{thickness}$$

$$C \propto \text{area} / \text{thickness}$$

$$R_{top} \propto \rho_{contact} / \text{area}$$

$$R_{bottom} \propto \frac{\rho_{contact}}{\text{area}} + \cancel{\frac{\rho_{sheet}}{4} \cdot \frac{\text{width}}{\text{length}}}$$

$$I_{\text{max, space-charge-limit}} \propto \text{area} / (\text{thickness})^2$$

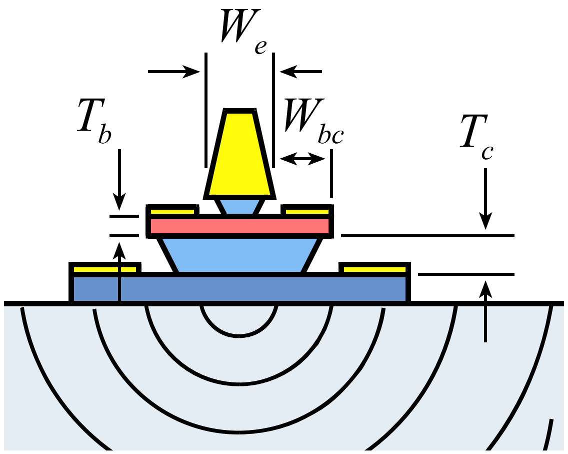
$$\Delta T \propto \frac{\text{power}}{\text{length}} \times \log\left(\frac{\text{length}}{\text{width}}\right)$$

To double bandwidth,

reduce thicknesses 2:1   Improve contacts 4:1
reduce width 4:1, keep constant length
increase current density 4:1

Bipolar Transistor Design

Bipolar Transistor Design



(emitter length L_E)

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

$$C_{cb} = \varepsilon A_c / T_c$$

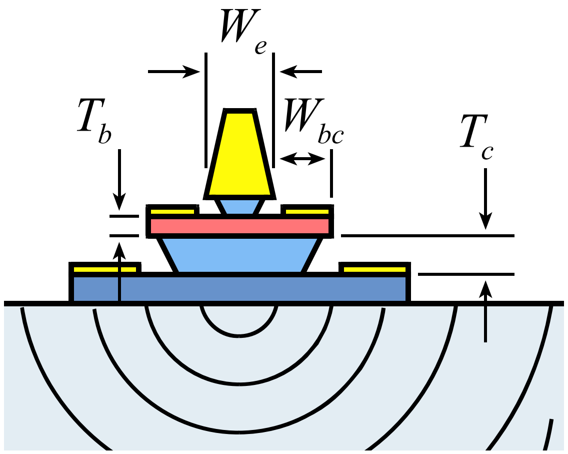
$$I_{c,\max} \propto v_{sat} A_e \left(V_{\text{ce,operating}} + V_{\text{ce,punch-through}}\right) / T_c^2$$

$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$

Bipolar Transistor Design: Scaling



(emitter length L_E)

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$$I_{c,\max} \propto v_{sat} A_e (V_{\text{ce,operating}} + V_{\text{ce,punch-through}}) / T_c^2$$

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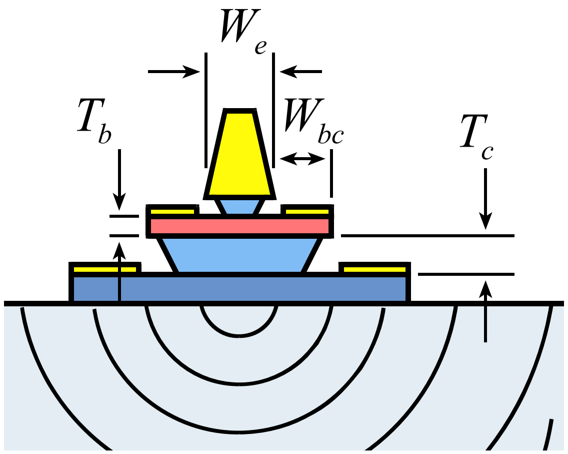
Bipolar Transistor Scaling Laws



$($emitter length $L_E)$

Changes required to double transistor bandwidth:

parameter	change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter contact resistance	decrease 4:1
current density	increase 4:1
base contact resistivity	decrease 4:1

Linewidths scale as the inverse square of bandwidth because thermal constraints dominate.

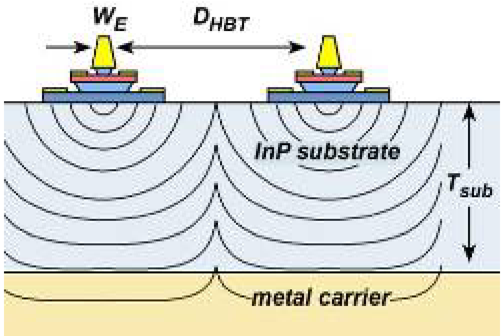
Thermal Resistance Scaling : Transistor, Substrate, Package

$$\Delta T_{\text{substrate}} \cong \overbrace{\frac{P}{\pi K_{InP} L_E}\ln\left(\frac{L_e}{W_e}\right)}^{\text{cylindrical heat flow near junction}} + \overbrace{\frac{P}{\pi K_{InP}}\left(\frac{1}{L_E}-\frac{1}{D}\right)}^{\text{spherical flow for } r > L_e} + \overbrace{\frac{P}{K_{InP}}\cdot\left(\frac{T_{sub}-D/2}{D^2}\right)}^{\text{planar flow for } r > D_{HBT}/2}$$

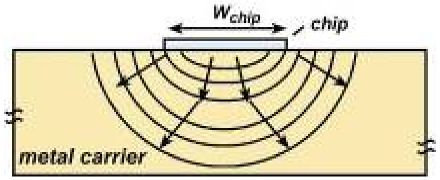
increases logarithmically

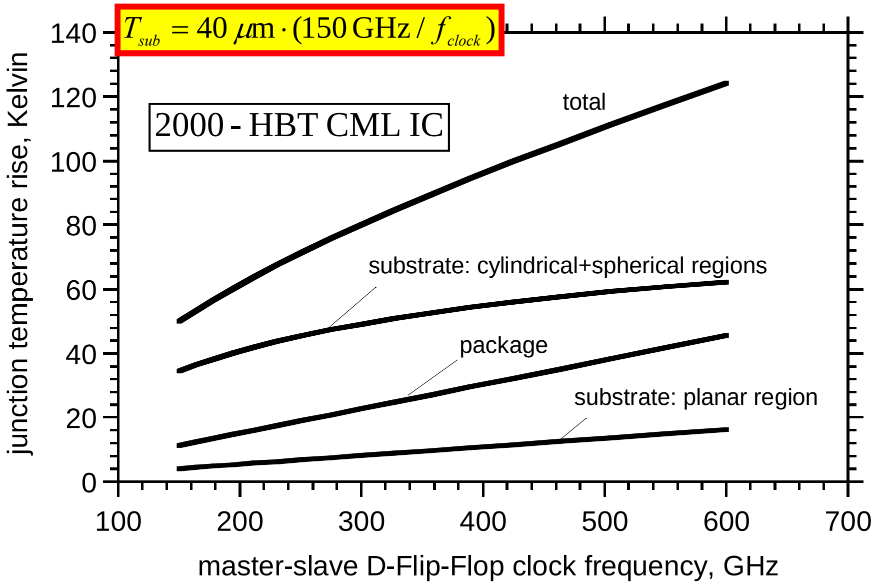
insignificant variation

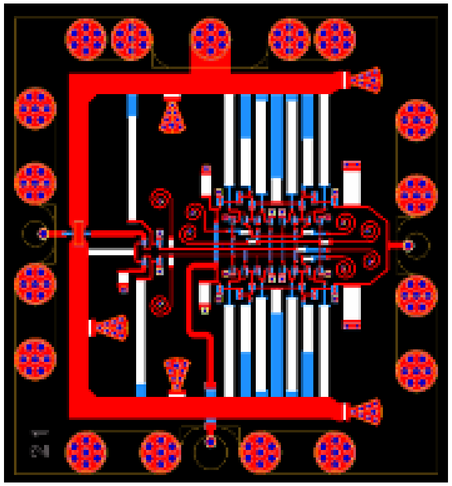
increases quadratically if T_{sub} is constant



$$\Delta T_{package} \cong \left(\frac{1}{4}+\frac{1}{\pi}\right)\frac{P_{chip}}{K_{Cu} W_{chip}}$$







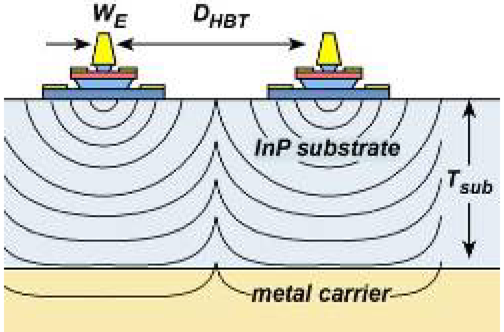
Wiring lenghts scale as 1/bandwidth. Power density, scales as $(\text{bandwidth})^2$.

Thermal Resistance Scaling : Transistor, Substrate, Package

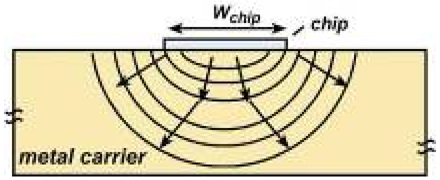
cylindrical heat flow near junction — spherical flow for $r > L_e$ — planar flow for $r > D_{HBT}/2$

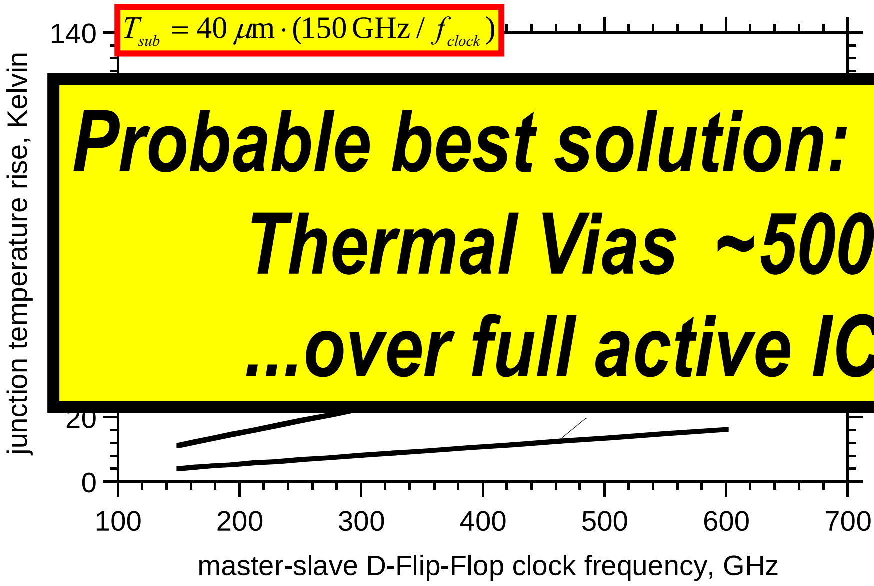
$$\Delta T_{\text{substrate}} \cong \frac{P}{\pi K_{InP} L_E}\ln\left(\frac{L_e}{W_e}\right) + \frac{P}{\pi K_{InP}}\left(\frac{1}{L_E} - \frac{1}{D}\right) + \frac{P}{K_{InP}} \cdot \left(\frac{T_{sub} - D/2}{D^2}\right)$$

increases logarithmically — insignificant variation — increases quadratically if T_{sub} is constant



$$\Delta T_{package} \cong \left(\frac{1}{4} + \frac{1}{\pi}\right)\frac{P_{chip}}{K_{Cu} W_{chip}}$$





$T_{sub} = 40\ \mu\text{m} \cdot (150\ \text{GHz} / f_{clock})$

Probable best solution:

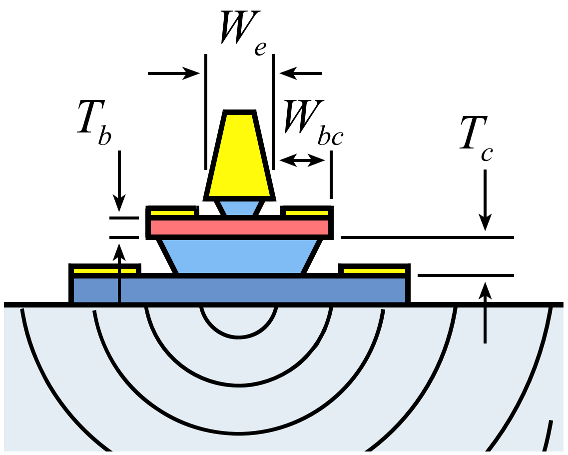
Thermal Vias ~500 nm below InP subcollector

...over full active IC area.

(bandwidth)^2.

InP Bipolar Transistor Scaling Roadmap

	industry	university →industry	university 2007-8	appears feasible	maybe
emitter	512	256	128	64	32 nm width
	16	8	4	2	$1\ \Omega\cdot\mu m^2$ access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	$1.25\ \Omega\cdot\mu m^2$ contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 $mA/\mu m^2$ current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz



Can we make a 1 THz SiGe Bipolar Transistor ?

Simple physics clearly drives scaling

transit times, C_{cb}/I_c

→ thinner layers, higher current density

high power density → narrow junctions

small junctions→ low resistance contacts

Key challenge: Breakdown

15 nm collector → very low breakdown

(also need better Ohmic contacts)

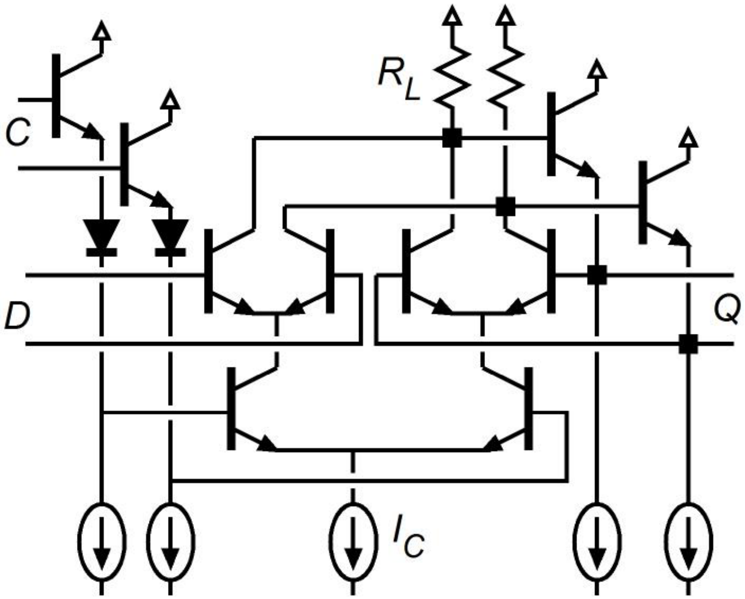
	InP	SiGe	
emitter	64	18	nm width
	2	**1.2**	$\Omega\cdot\mu m^2$ access ρ
base	64	56	nm contact width,
	2.5	**1.4**	$\Omega\cdot\mu m^2$ contact ρ
collector	53	**15**	nm thick
	36	125	$mA/\mu m^2$
	2.75	**???**	V, breakdown
f_τ	1000	1000	GHz
f_{max}	2000	2000	GHz
PAs	1000	1000	GHz
digital	480	480	GHz

(2:1 static divider metric)

Assumes collector junction 3:1 wider than emitter.

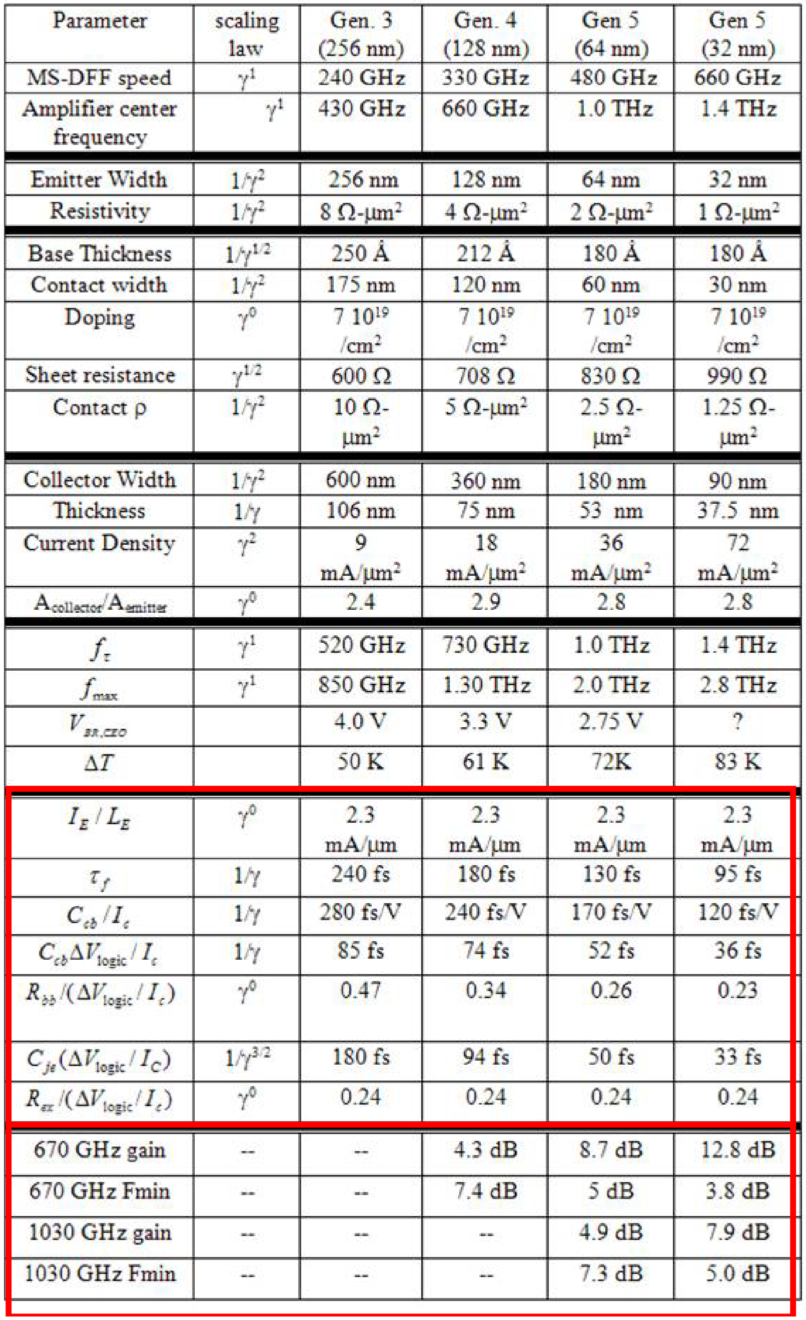
Assumes SiGe contacts 2:1 wider than junctions

HBT Design For IC Performance



from charge-control analysis:

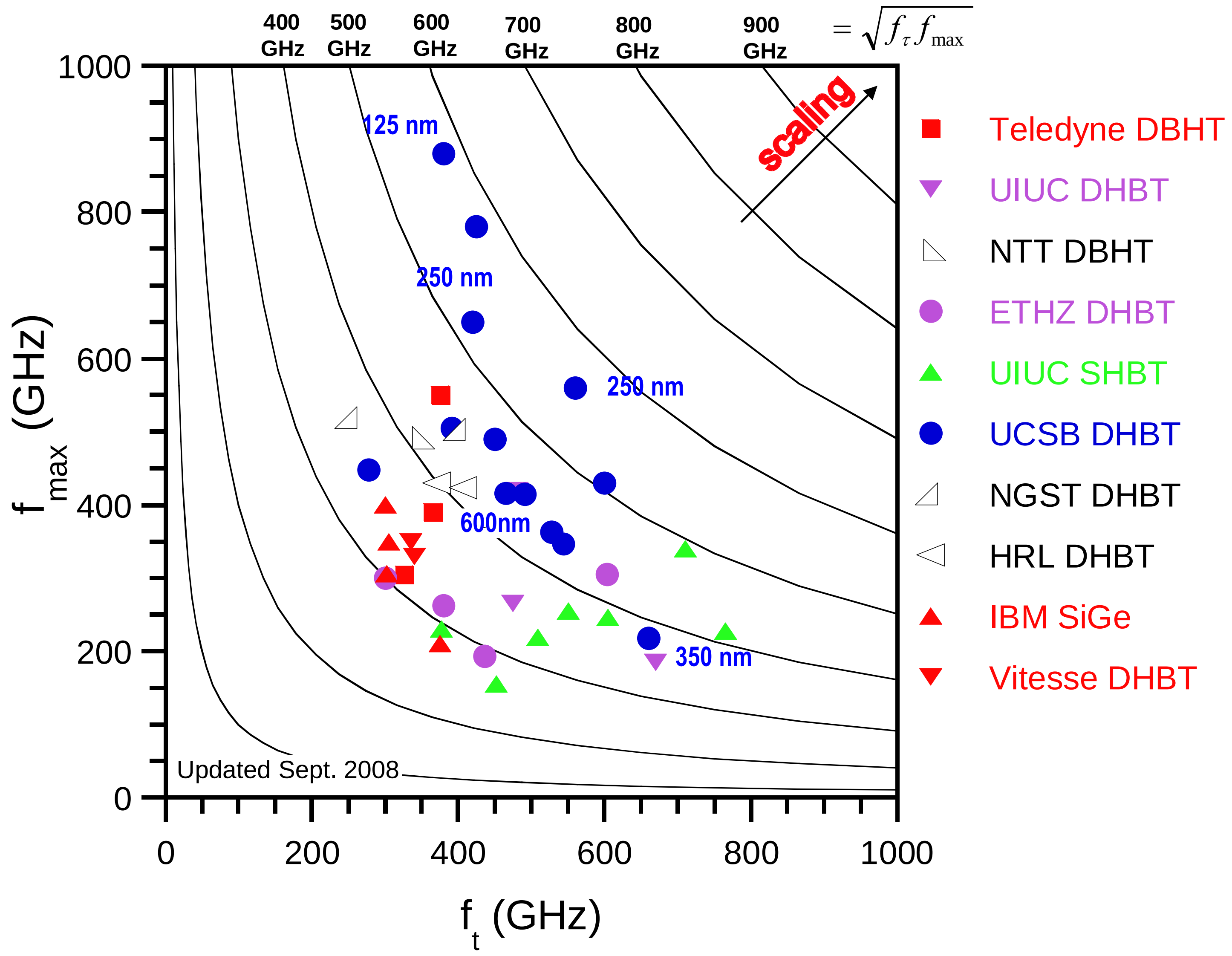
$$
\begin{aligned}
T_{gate} \approx\ & (\Delta V_L / I_C)(C_{je} + 6C_{cbx} + 6C_{cbi}) + \tau_f \\
& + (kT/qI_C)(0.5C_{je} + C_{cbx} + C_{cbi} + 0.5\tau_f I_C / \Delta V_L) \\
& + R_{ex}(0.5C_{cbx} + 0.5C_{cbi} + 0.5\tau_f I_C / \Delta V_L) \\
& + R_{bb}(0.5C_{je} + C_{cbi} + 0.5\tau_f I_C / \Delta V_L).
\end{aligned}
$$



Parameter	scaling law	Gen. 3 (256 nm)	Gen. 4 (128 nm)	Gen 5 (64 nm)	Gen 5 (32 nm)
MS-DFF speed	γ^1	240 GHz	330 GHz	480 GHz	660 GHz
Amplifier center frequency	γ^1	430 GHz	660 GHz	1.0 THz	1.4 THz
Emitter Width	$1/\gamma^2$	256 nm	128 nm	64 nm	32 nm
Resistivity	$1/\gamma^2$	8 Ω-µm²	4 Ω-µm²	2 Ω-µm²	1 Ω-µm²
Base Thickness	$1/\gamma^{1/2}$	250 Å	212 Å	180 Å	180 Å
Contact width	$1/\gamma^2$	175 nm	120 nm	60 nm	30 nm
Doping	γ^0	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²
Sheet resistance	$\gamma^{1/2}$	600 Ω	708 Ω	830 Ω	990 Ω
Contact ρ	$1/\gamma^2$	10 Ω-µm²	5 Ω-µm²	2.5 Ω-µm²	1.25 Ω-µm²
Collector Width	$1/\gamma^2$	600 nm	360 nm	180 nm	90 nm
Thickness	$1/\gamma$	106 nm	75 nm	53 nm	37.5 nm
Current Density	γ^2	9 mA/µm²	18 mA/µm²	36 mA/µm²	72 mA/µm²
$A_{collector}/A_{emitter}$	γ^0	2.4	2.9	2.8	2.8
f_τ	γ^1	520 GHz	730 GHz	1.0 THz	1.4 THz
f_{max}	γ^1	850 GHz	1.30 THz	2.0 THz	2.8 THz
$V_{BR,CEO}$		4.0 V	3.3 V	2.75 V	?
ΔT		50 K	61 K	72K	83 K
I_E / L_E	γ^0	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm
τ_f	$1/\gamma$	240 fs	180 fs	130 fs	95 fs
C_{cb} / I_c	$1/\gamma$	280 fs/V	240 fs/V	170 fs/V	120 fs/V
$C_{cb}\Delta V_{logic} / I_c$	$1/\gamma$	85 fs	74 fs	52 fs	36 fs
$R_{bb}/(\Delta V_{logic} / I_c)$	γ^0	0.47	0.34	0.26	0.23
$C_{je}(\Delta V_{logic} / I_C)$	$1/\gamma^{3/2}$	180 fs	94 fs	50 fs	33 fs
$R_{ex}/(\Delta V_{logic} / I_c)$	γ^0	0.24	0.24	0.24	0.24
670 GHz gain	--	--	4.3 dB	8.7 dB	12.8 dB
670 GHz Fmin	--	--	7.4 dB	5 dB	3.8 dB
1030 GHz gain	--	--	--	4.9 dB	7.9 dB
1030 GHz Fmin	--	--	--	7.3 dB	5.0 dB

InP HBT: Status

InP DHBTs: September 2008



popular metrics :

f_τ or $f_{\max}$ alone

$(f_\tau + f_{\max})/2$

$\sqrt{f_\tau f_{\max}}$

$(1/f_\tau + 1/f_{\max})^{-1}$

much better metrics :

power amplifiers:

PAE, associated gain,

mW/μm

low noise amplifiers:

$F_{\min}$, associated gain,

digital:

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

$(R_{ex}I_c / \Delta V)$,

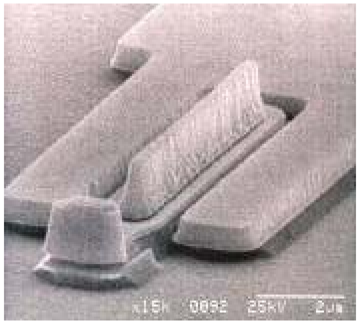
$(R_{bb}I_c / \Delta V)$,

$(\tau_b + \tau_c)$

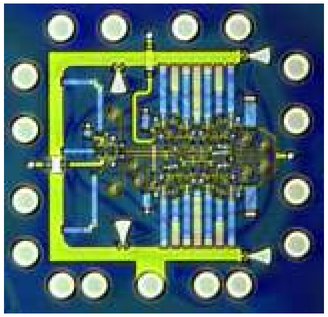
512 nm InP DHBT

Laboratory Technology

500 nm mesa HBT

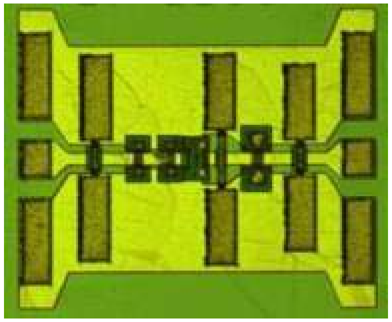


150 GHz M/S latches



UCSB / Teledyne / GCS

175 GHz amplifiers

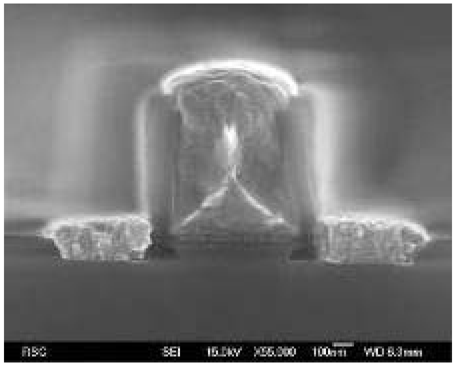


UCSB

Production

(Teledyne)

500 nm sidewall HBT



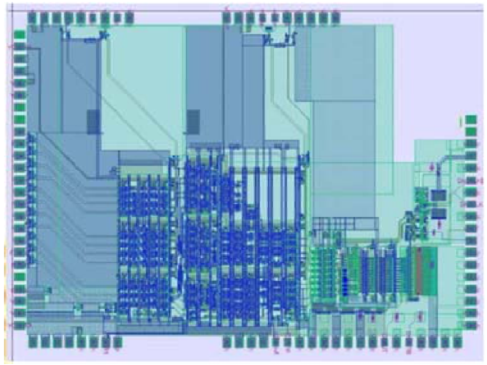
Teledyne

f_τ = 405 GHz

f_{max} = 392 GHz

$V_{br,\,ceo}$ = 4 V

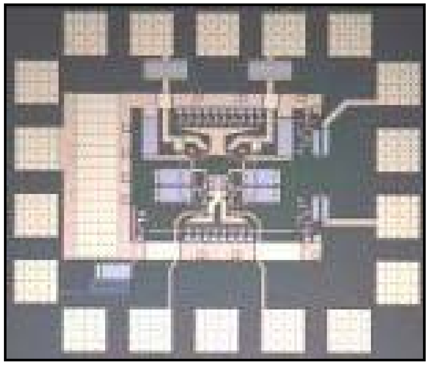
DDS IC: 4500 HBTs



Teledyne / BAE

20 GHz clock

20-40 GHz op-amps

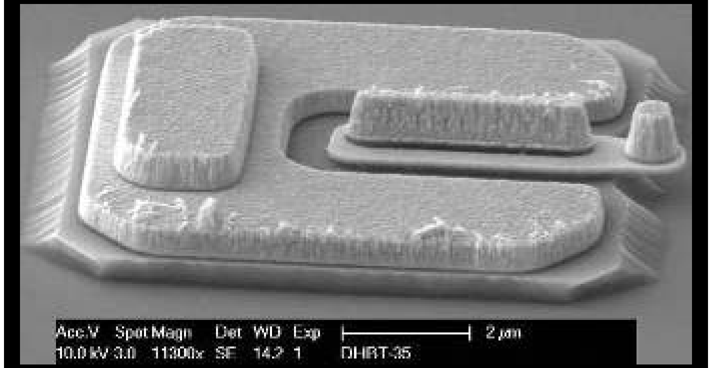


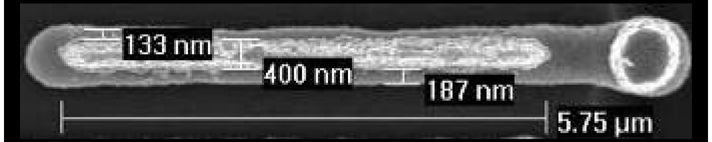
Teledyne / UCSB

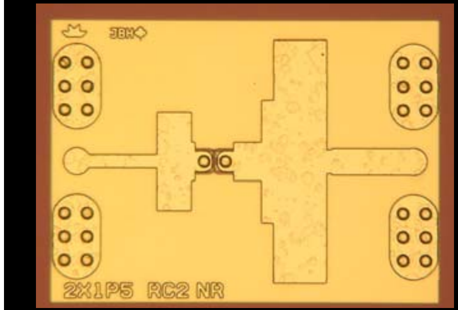
53-56 dBm OIP3 @ 2 GHz with 1 W dissipation

Z. Griffith
M. Urteaga
P. Rowell
D. Pierson
B. Brar
V. Paidi

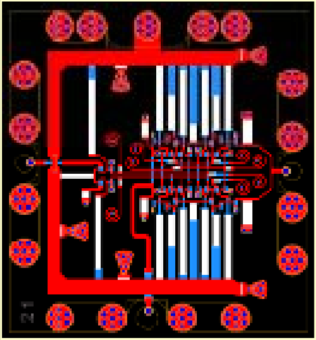
256 nm Generation InP DHBT







324 GHz Amplifier

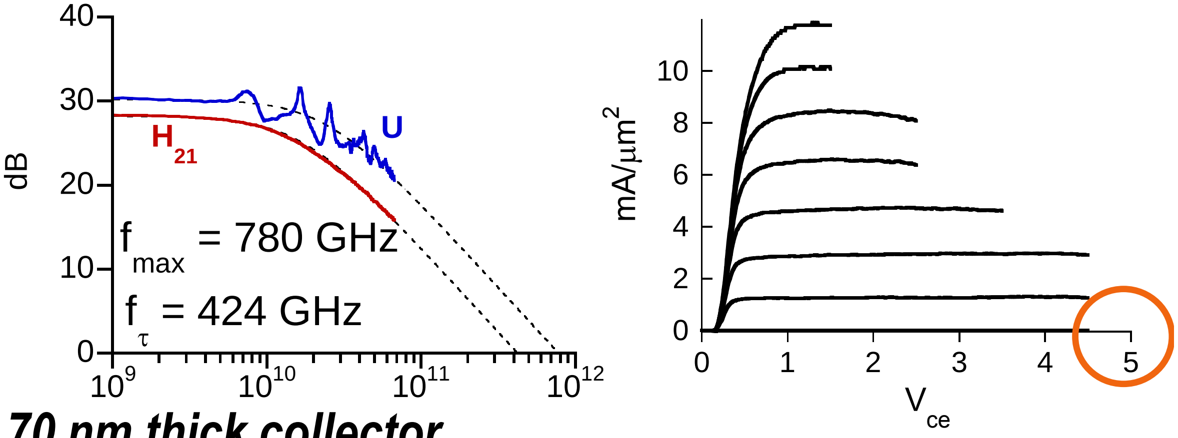


200 GHz master-slave latch design

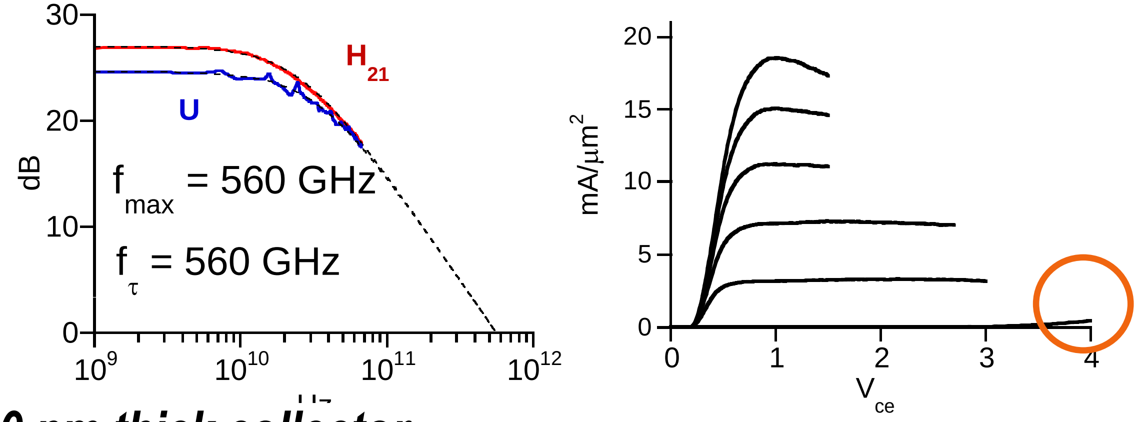
Z. Griffith, E. Lind

J. Hacker, M. Jones

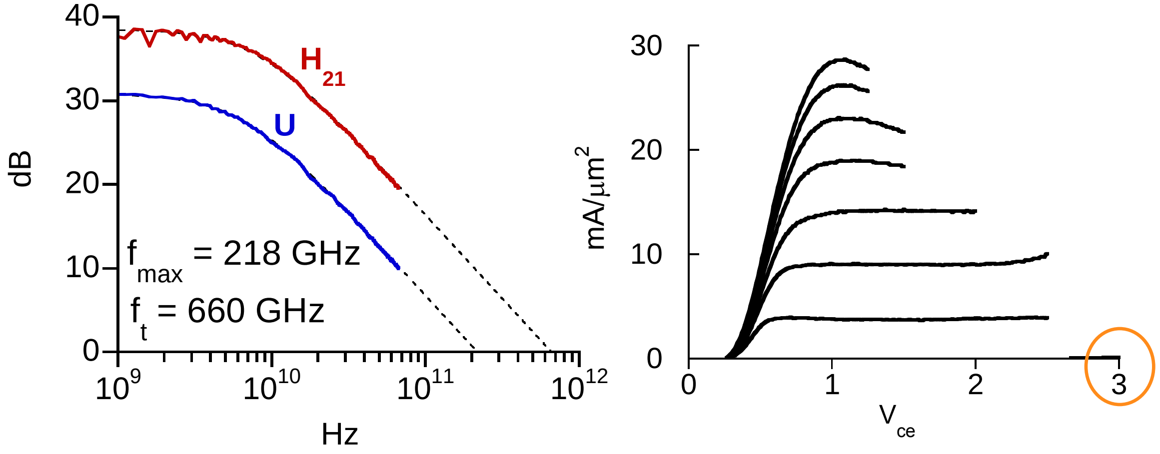
150 nm thick collector



70 nm thick collector



60 nm thick collector



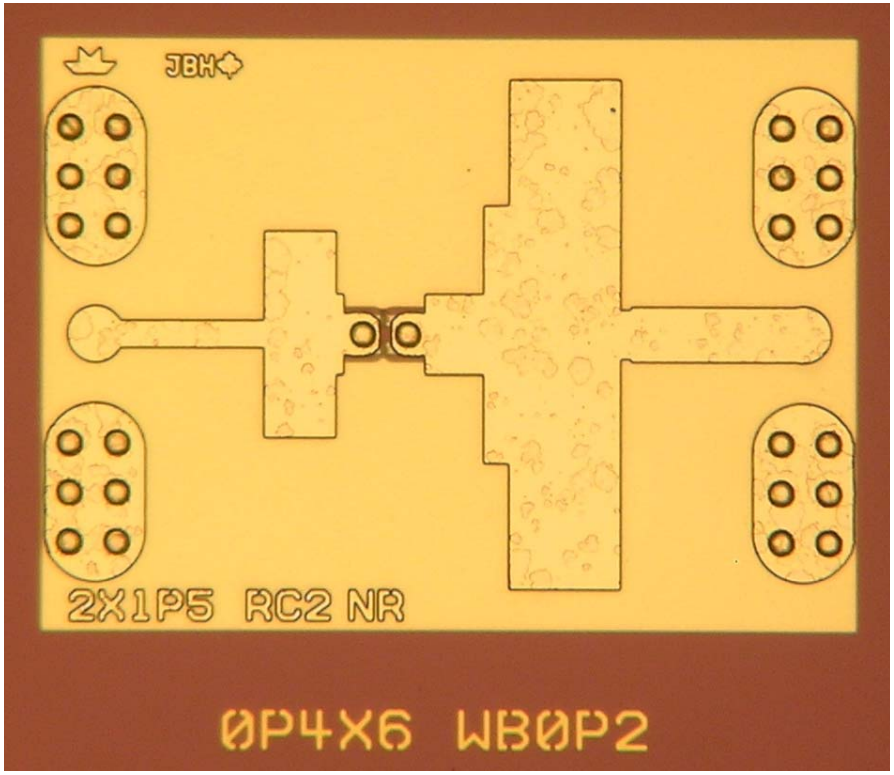
324 GHz Medium Power Amplifiers in 256 nm HBT

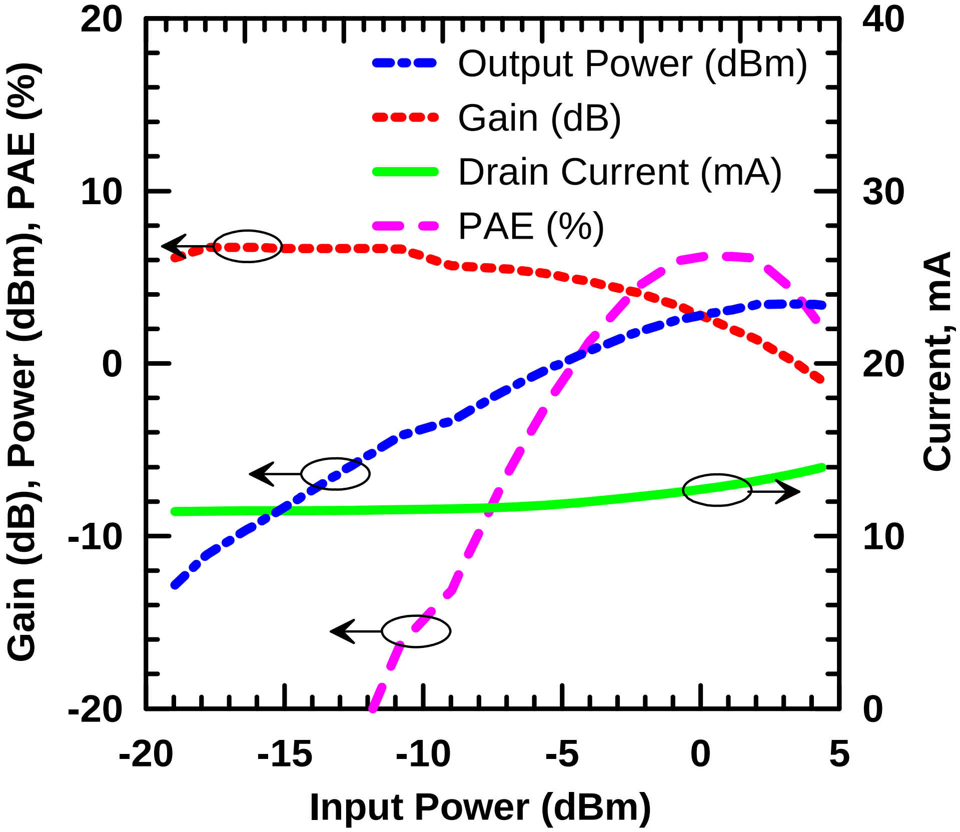
ICs designed by Jon Hacker / Teledyne

Teledyne 256 nm process flow-

Hacker et al, 2008 IEEE MTT-S

~2 mW saturated output power



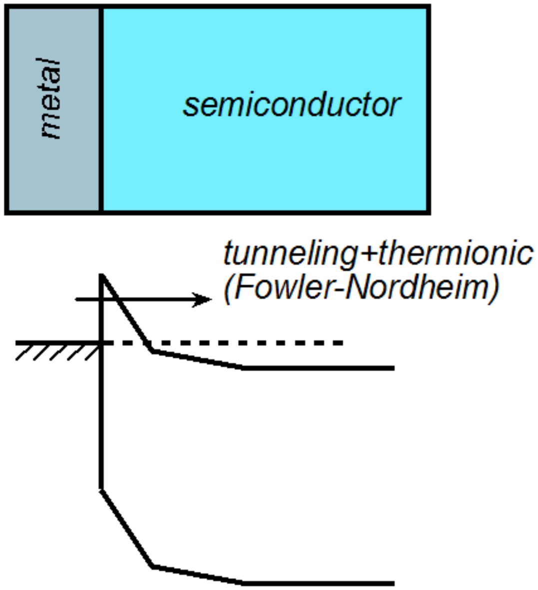


128 / 64 / 32 nm
HBT Technologies

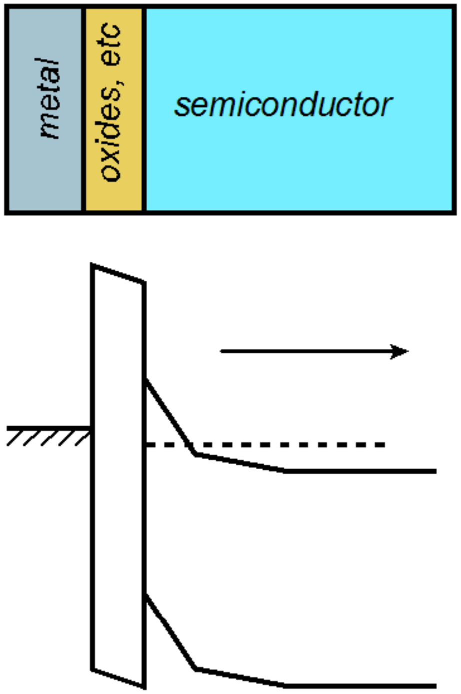
Conventional ex-situ contacts are a mess

THz transistor bandwidths: very low-resistivity contacts are required

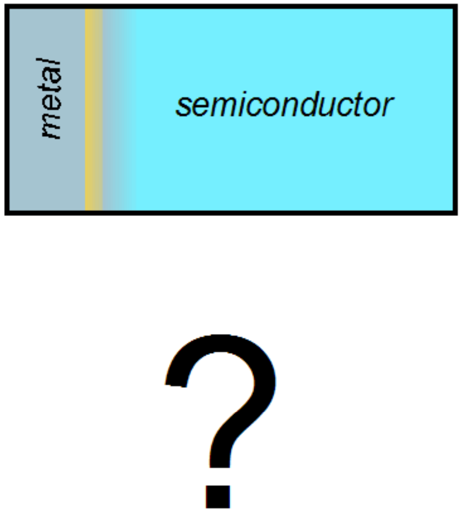
textbook contact



with surface oxide



with metal penetration



Interface barrier → resistance

Further intermixing during high-current operation → degradation

Improvements in Ohmic Contacts

128 nm generation requires ~ 4 $\Omega - \mu m^2$ emitter & base resistivities

64 nm generation requires ~ 2 $\Omega - \mu m^2$

Contacts to N-InGaAs*:

Mo	*MBE in-situ*	*0.3 (+/- 0.7) $\Omega - \mu m^2$*
TiW	*ex-situ / NH4 pre-clean* *variable between process runs*	*~1 to 2 $\Omega - \mu m^2$*

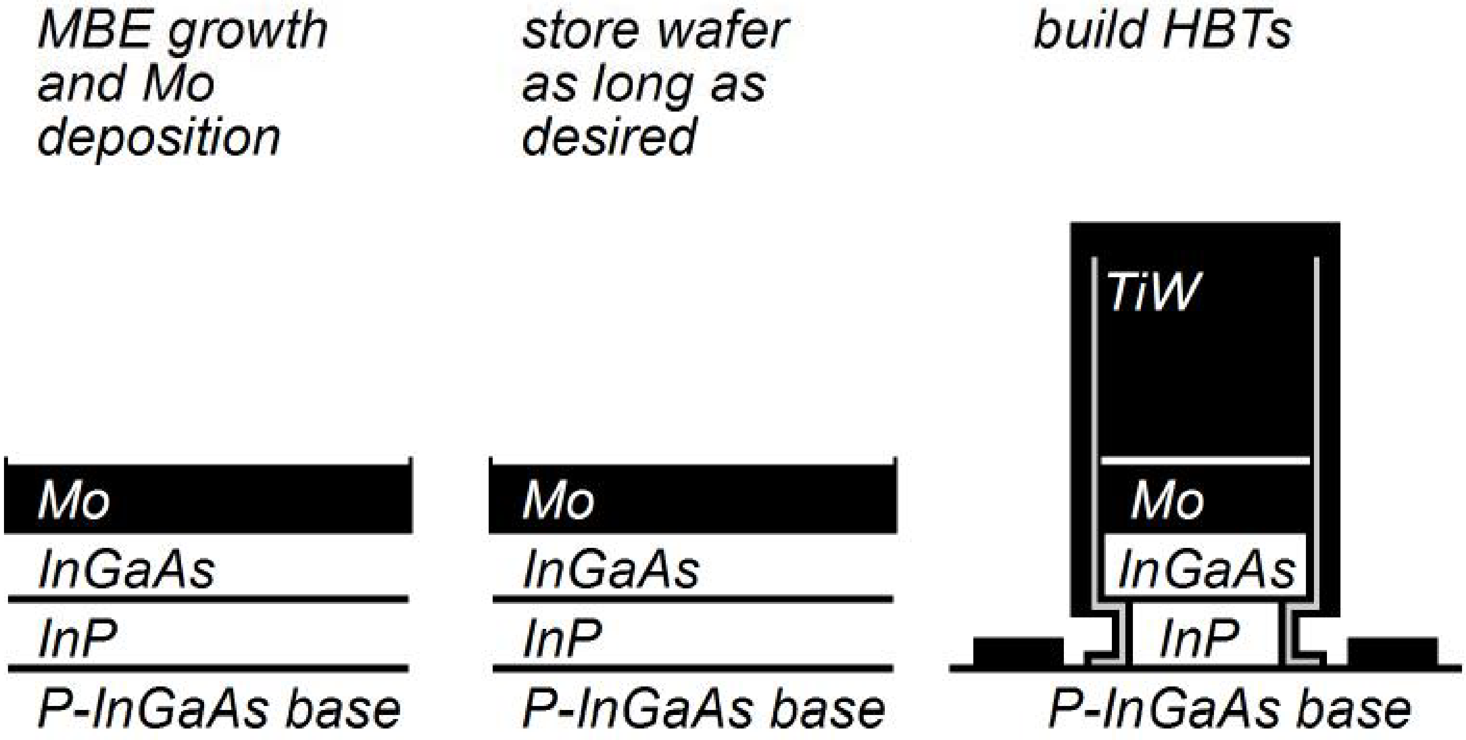
Contacts to P-InGaAs:

Mo	*MBE in-situ*	*below 2.5 $\Omega - \mu m^2$*
Pd/Ti...	*ex-situ*	*~4 $\Omega - \mu m^2$*

**measured emitter resistance remains higher than that of contacts.*

Mo Emitter Contacts: Robust Integration into Process Flow

Proposed Process Integration:



MBE growth and Mo deposition

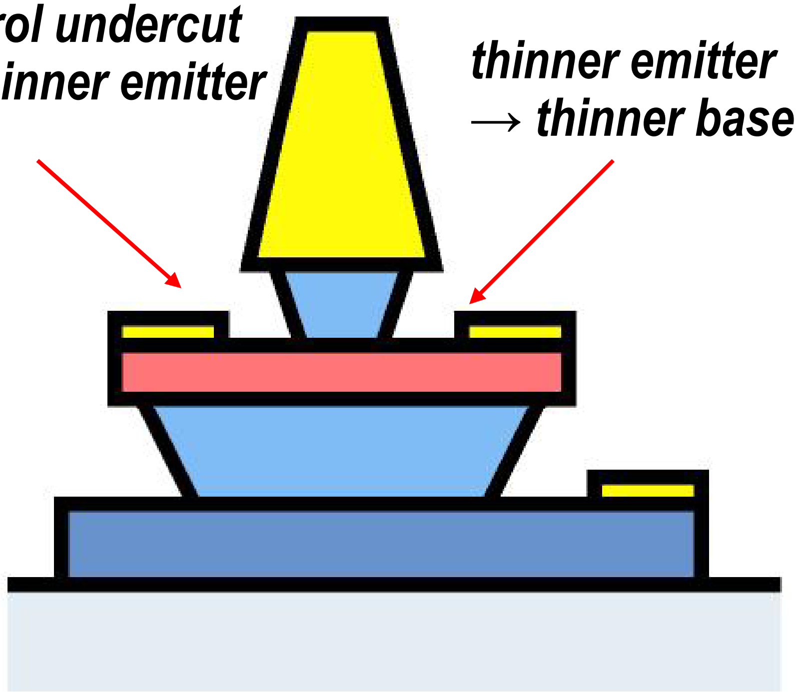
store wafer as long as desired

build HBTs

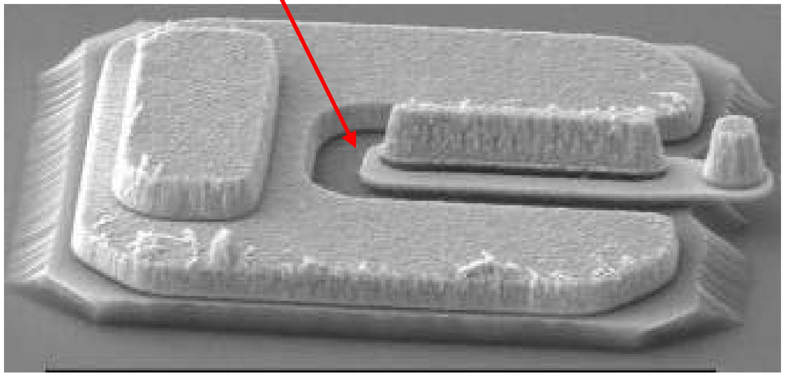
Process Must Change Greatly for 128 / 64 / 32 nm Nodes

control undercut
→ thinner emitter

thinner emitter
→ thinner base metal

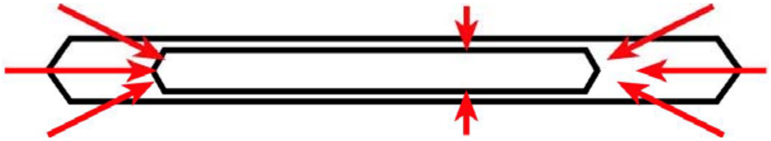


thinner base metal
→ excess base metal resistance

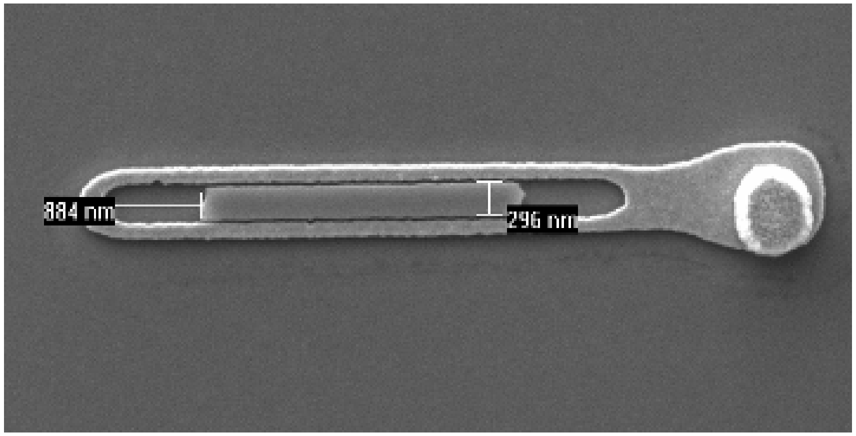


Undercutting of emitter ends

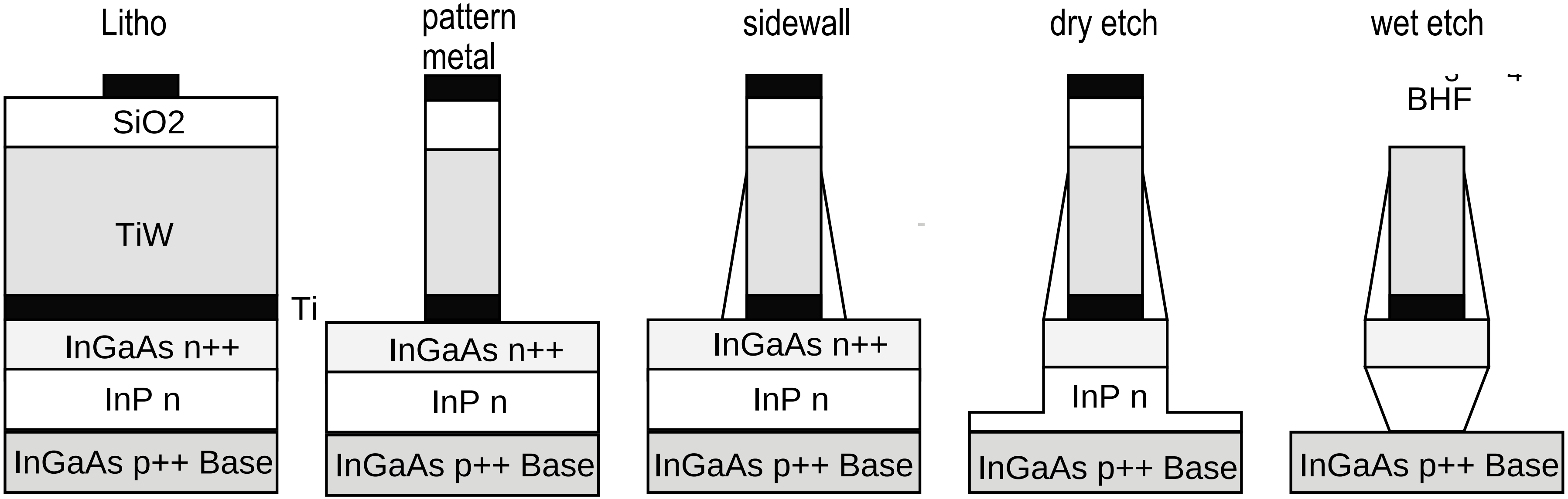
{101}A planes: fast



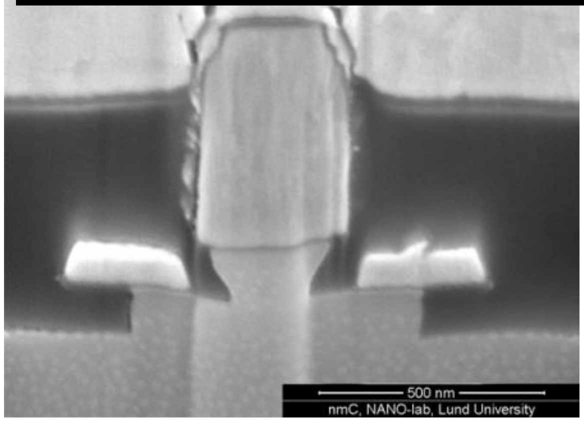
{111}A planes: slow

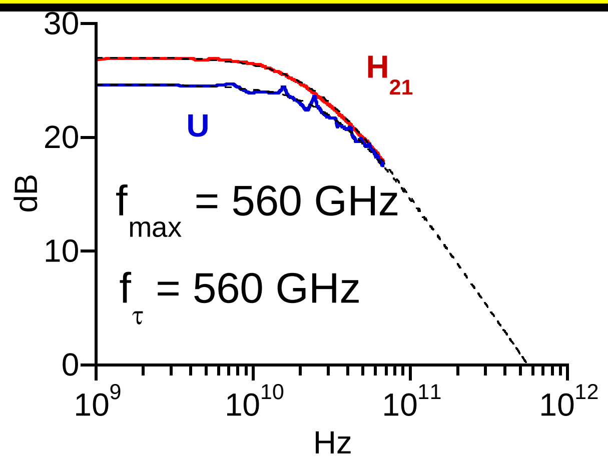


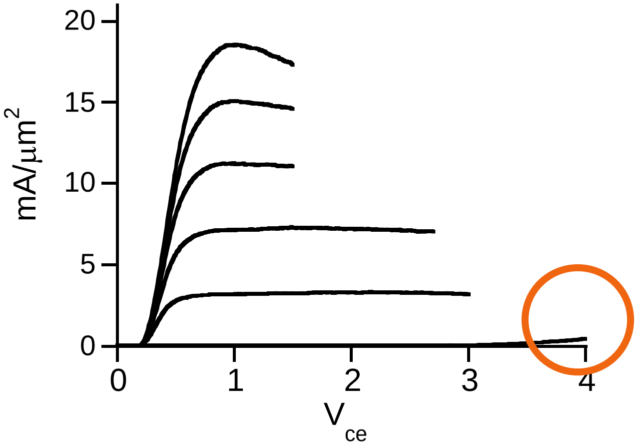
128 nm Emitter Process: Dry Etched Metal & Semiconductor



Recent Results @ 128 nm emitter width to be submitted

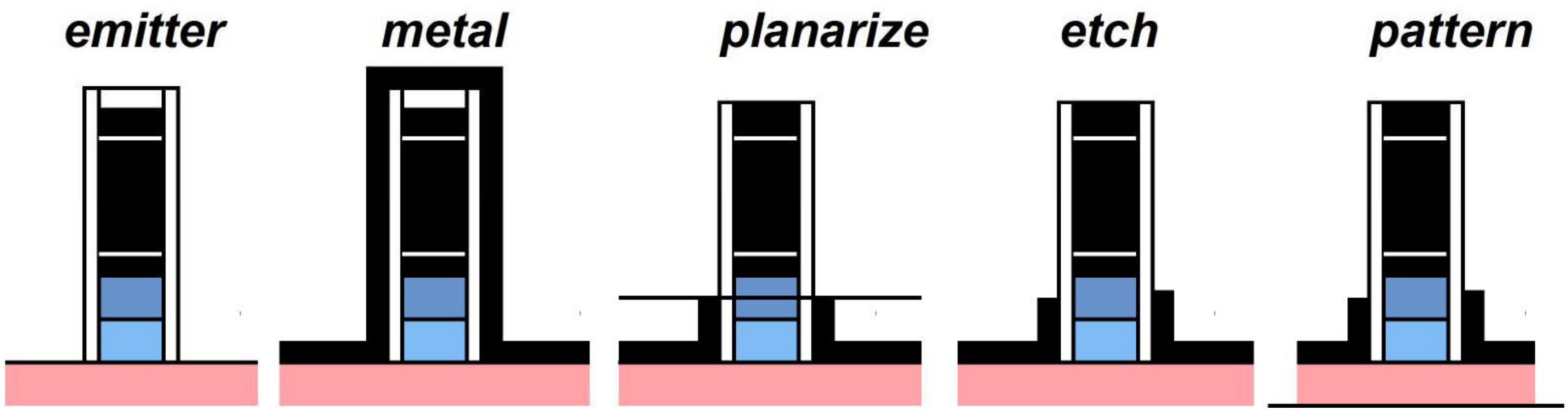


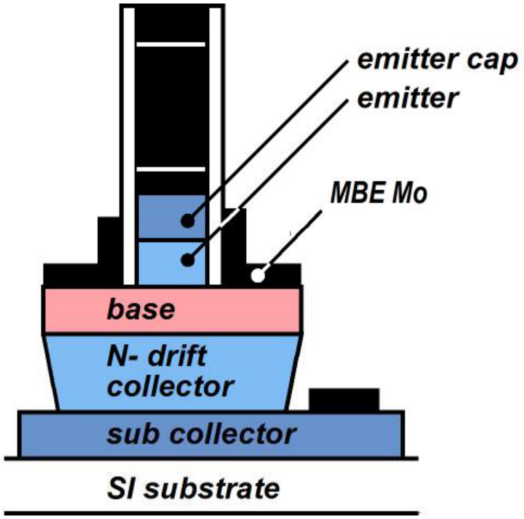


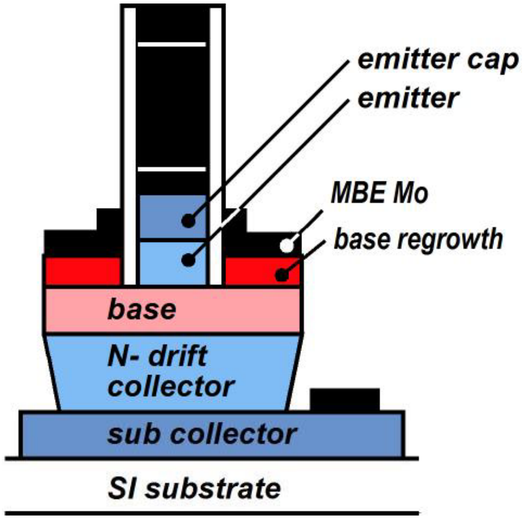


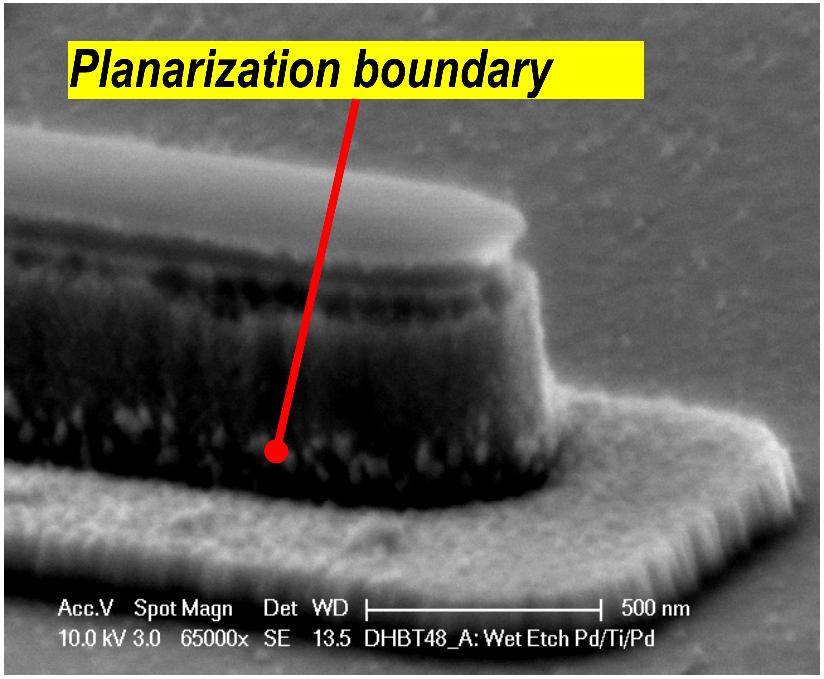
results @ c.a. 200 nm emitter metal width

Planarization E/B Processes for 64 & 32 nm





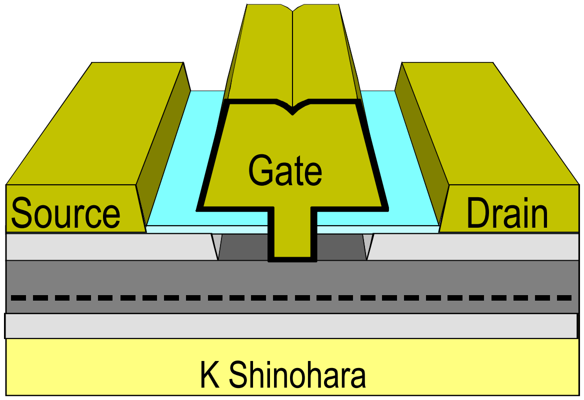


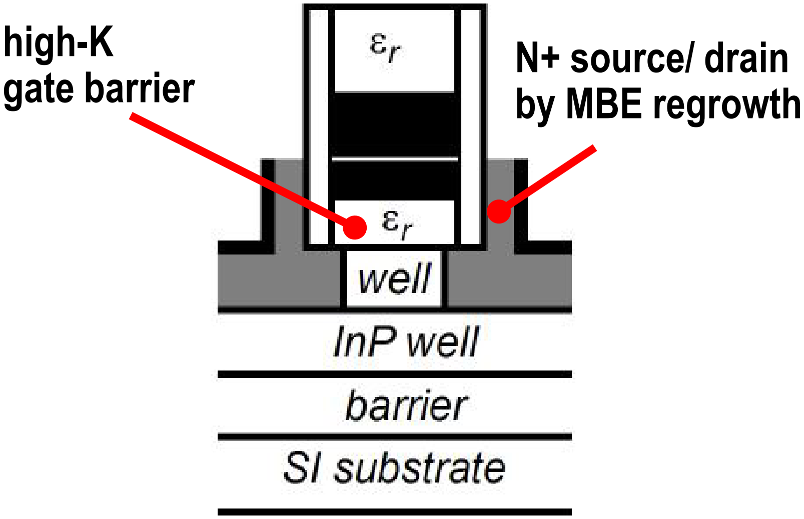


What about InGaAs HEMTs ?

...& InGaAs MOSFETS ?

InGaAs HEMTs and InGaAs MOSFETs





sub-22-nm InGaAs MOSFETs being developed for potential use in VLSI

Efforts may: improve understanding HEMT & MOSFET scaling limits
produce process modules which aid THz HEMTs

Key III-V MOSFET scaling limits:
low density of states→limits g_m→ $C_{fringing}/g_m$ does not scale
low m → high well energy → minimum well thickness*

Additional HEMT scaling limits:
high access resistance: barriers, recess regions, contacts
limits to sheet concentration from small hetero-barrier energy

HBT Applications

Applications of THz InP HBTs

Mixed-Signal ICs (ADCs, DACs, DDS)

benefit in high-clock-rate ICs with 1k-3k devices
lack of CMOS integration a major limitation
→ Mark Rosker's talk

Precision GHz analog ICs using THz transistors

→ Sanjay Raman's talk , Zach Griffith's talks

mm-Wave Power: 60 GHz & up

GaN threatens, but f_{max} *→ gain → PAE*

600-1000 GHz transceiver ICs

for low-volume military / scientific applications

Few-THz Bipolar Transistors

THz InP Bipolar Transistors: can it be done ?

Scaling limits: contact resistivities, device and IC thermal resistances.

62 nm (1 THz f_τ, 1.5 THz f_{max}) scaling generation is feasible.

700 GHz amplifiers, 450 GHz digital logic

Is the 32 nm (1 THz amplifiers) generation feasible ?

THz InP Bipolar Transistors: what would we do with it ?

Mixed-Signal IC Power density & CMOS integration are serious challenges

Precision GHz analog systems

mm-wave power

Sub-mm-wave electronics