InGaAs channel MOSFET with self-aligned source/drain MBE regrowth technology

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InGaAs is a promising alternative channel material to Si for sub-22 nm node technology because of its low electron effective mass (m^*) hence high electron velocities. We report a gate-first MOSFET process with self-aligned source/drain formation using non-selective MBE re-growth, suitable for realizing high performance scaled III-V MOSFETs.

A W/Cr/SiO_2 gate stack was defined on thin (4 nm/ 2.5 nm) InGaAs/InP channel by an alternating selective dry etch technique. A 5 nm Al_2O_3 layer was used as gate dielectric. An InAlAs bottom barrier provided vertical confinement of the channel. An *in-situ* H cleaning of the wafer leaves an epi-ready surface suitable for MBE or MOCVD regrowth.

Source/Drain region were defined by non-selective MBE regrowth and *in situ* molybdenum contacts. First generation of devices fabricated using this process showed extremely low drive current of 2 µA/µm.

The drive current was limited by an extremely high source resistance. A regrowth gap between source/drain and gate was the cause for high source resistance. The gap in the regrowth was because of low growth temperature (400 ºC). A modified high temperature growth technique resolved the problem.

Si is expected to reach the scaling limit beyond 22 nm gate node mainly due to the inability to achieve low leakage sub-0.5 nm equivalent oxide thickness (EOT) gate dielectrics. Also, sub-22 nm gate length and sub-1 nm EOT Si devices cannot realize complete ballistic transport, hence not achieving the full potential drive currents [1]. High electron velocity III-V materials are investigated as an alternative channel to Si in N-MOSFETs. $In_xGa_{1-x}As$ ($x \geq 0.53$) is a leading candidate as a channel material because

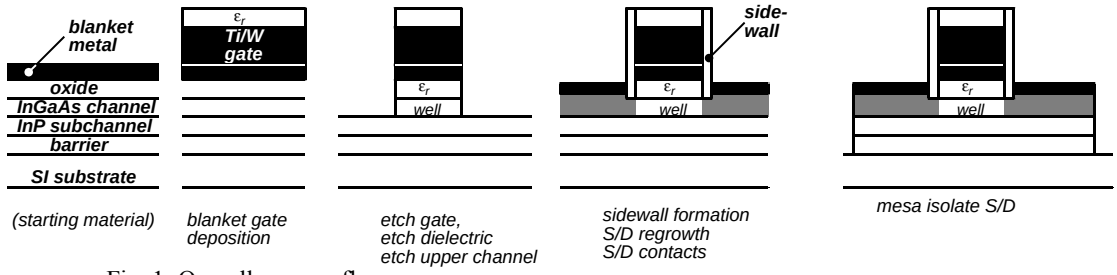


Fig. 1: Overall process flow

of its low electron effective mass (m^*) and high saturation velocities (v). Also the large inter-valley separation in $In_{0.53}Ga_{0.47}As$ (InGaAs) reduces inter-valley scattering, so electron velocities remain high even at high electric fields. The main obstacle of unpinned interfaces to high-k dielectric on InGaAs have been addressed by several groups with various high-k dielectrics [2, 3, 4]. However these devices either have long gate lengths or were not scaled vertically. The full potential of InGaAs channel devices can only be realized in MOSFETs which are scaled both horizontally and vertically.

We report the design and process flow development of a self-aligned InGaAs MOSFET using MBE regrown source/drain (S/D) regions. Detailed MOSFET scaling laws and sub-22 nm III-V FET design are discussed in references [1, 5, 6]. Lateral scaling of the gate length to 22 nm dictates a vertical scaling of the device. At sub-22 nm gate lengths, a maximum of 1 nm EOT dielectric and 5 nm thick channel with strong vertical confinement are required for maximum transconductance (g_m) and acceptably low drain induced barrier lowering (DIBL). We use $In_{0.52}Al_{0.48}As$ (InAlAs) heterojunction barrier to achieve this confinement. An alternative approach using electrostatic confinement would need high p^+ doping in the In GaAs channel, which would reduce the channel mobility because of impurity scattering and will also degrade the short channel effects due to discrete dopant fluctuations. In sub-22 nm devices, the device parasitic capacitances dominate and limit the circuit delay [1, 5]. The IC delay (τ) can be reduced only through high drive current (I_d) and high g_m. InGaAs MOSFETs are expected to achieve very high drive currents (5 mA/μm) and transconductances (7 mS/μm) because of high thermal velocities ($J=qnv$) [1, 5, 6]. These current levels are achieved at a sheet concentration of ~ 10^{13} cm^{-2}. Large intervalley separation ($E_{\Gamma-L}$, $E_{\Gamma-X}$ = 0.5 eV) in InGaAs makes it possible to achieve these densities without populating the slower satellite valleys.

Furthermore, source access resistance plays an important role in scaled devices because it degrades the available I_d and g_m from the device. Even a very low source access resistance of 15 Ω–μm would degrade I_d by 10% [5]. This value is an order of magnitude smaller than the ITRS roadmap listed source access resistance of 180 Ω–μm [7]. IC layout density requirement would constrain $L_c = L_g = 22$ nm, which means a specific contact resistivity ρ_c=0.25 Ω–μm^2 corresponding to 10 Ω–μm resistance. A 4 Ω–μm S/D extension access resistance translates into a high 5×10^{19} cm^{-3} active doping in these regions. Besides source resistance, high doping concentrations is required in S/D to avoid "source starvation" [6]. Unlike Si, ion implantation is not a viable technique for InGaAs due to various difficulties. There is no data showing the capability of implantation realizing these high active concentrations and contact resistance values. Instead we are using MBE to regrow S/D regions after gate formation. Active Si doping ~ 4×10^{-19} cm^{-3} and low contact resistance of 0.5 Ω–μm^2 have been demonstrated by MBE and in-situ molybdenum (Mo) contacts [8]. Scaled sub 50 nm Schottky barrier FETs (HEMTs) with 1 nm EOT have been reported but have not been able to achieve the high simulated drive currents [9]. HEMTs have non-scalable source resistance because of the high bandgap barrier under the S/D contacts [10]. The Schottky gate barrier also has a higher gate leakage current than dielectrics do, making it unsuitable for VLSI applications.

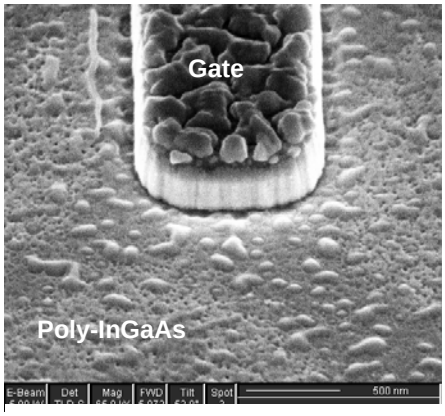


Fig. 2: SEM of Poly-InGaAs regrowth

The details of the process flow are provided below, but the general flow is as follows. As shown in Fig. 1, the gate was defined first by a scalable dry etch process rather than by traditional III-V lifoff techniques. The high-k dielectric was wet etched and gate was encapsulated in a SiN sidewall, followed by InGaAs source/drain regrowth by molecular beam epitaxy (MBE). Self-aligned contacts were defined by a blanket metal deposition and a height-selective etch, then the devices were mesa isolated. We shall now discuss these steps in greater detail.

First, a composite InGaAs (4 nm)/InP (2.5 nm) channel and 100 nm of InAlAs back barrier was grown by MBE on semi-insulating InP. Then the wafer was cooled to 50 ºC and capped with 100 nm of As. The wafer was unloaded and transferred to an Atomic Layer Deposition (ALD) chamber, then the As cap was desorbed, and 5 nm of Al_2O_3 dielectric was grown immediately. Next, the blanket gate stack W(50nm)/Cr(50nm)/SiO_2(300nm)/Cr(50nm) was deposited. For these devices, the gate dielectric is directly on top of the thin channel, without any intentional intermediate layers. This imparts a considerable processing challenge as thin layers are prone to damage during dry etches. A damaged channel layer would result in imperfect S/D regrowth, which leads to high source resistances. Also, any pinhole introduced in the channel because of the dry etch would expose and oxidize the underlying InAlAs layer. This would again cause defect ridden S/D regrowth and high resistances. Fig. 2 shows the faceted and resistive poly-InGaAs which results from regrowth on a damaged channel.

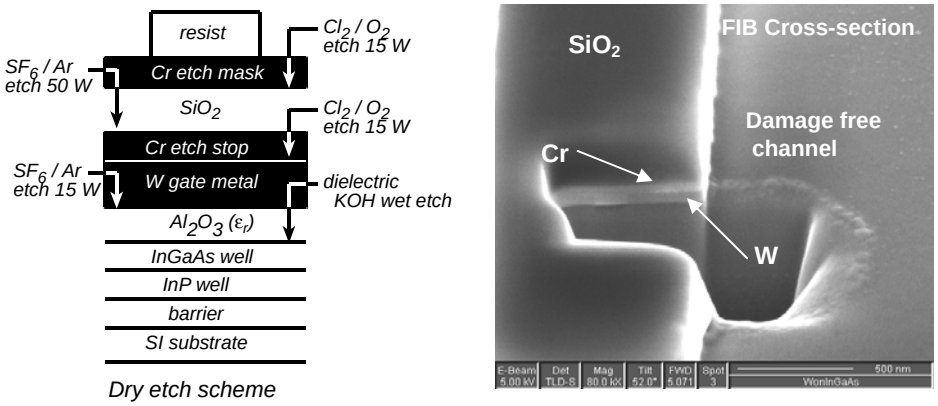


Fig. 3: Dry etch scheme and FIB crosssection SEM image of a gate

Therefore a multiple layer gate stack and alternating selective dry etch scheme was developed (Fig. 3). The top Cr layer was used as a dry etch mask after patterning it with photoresist and i-line photolithography, followed by a Cl_2/O_2 dry etch. The Cr was removed before the channel was exposed. Next, before the SiO_2 was etched, the photo-resist was stripped and O_2 plasma etched; the SiO_2 protected the channel from damage, and the aggressive O_2 etch prevented organic contamination of the MBE chamber. The alternating selective dry etch scheme (Fig. 3) allows a final low power dry etch of the W layer without damaging the channel. The Al_2O_3 dielectric was wet etched in dilute KOH solution. As a result, 300 nm long and 400 nm thick gate stacks were fabricated on 4 nm InGaAs channel. The process can be easily used to fabricate sub-50 nm features by using electron beam lithography.

A 45 nm, conformal layer of SiN_x was deposited over the gates by PECVD, and a low power anisotropic etch was performed to remove the SiN_x from the far field, leaving well defined sidewalls. The final SiO_2/W/Cr structure with SiN_x sidewalls leaves the metals unexposed in the MBE chamber during regrowth avoiding any possible metal contamination. The InGaAs channel was selectively wet etched, stopping on the InP sub-channel, and an over-etch was done to etch a small amount InGaAs under the SiN_x sidewall. Next the wafer was treated with 30 minute UV-Ozone forming a 1 nm sacrificial oxide. It was followed by 1 minute 1:10 HCl:DI treatment to remove the oxide, 1 minute DI rinse, and blown dry in N_2. Then it was immediately loaded into MBE chamber and baked overnight at 200 ºC. The wafer was atomic hydrogen cleaned at 400 ºC for 30 minutes. A c(2×4) surface reconstruction was seen in reflection high energy electron diffraction (RHEED) before regrowth, indicating an epi-ready surface. Using this cleaning procedure, defect free epitaxial InGaAs films were regrown on InGaAs and showed low sheet and contact resistances [11]. A 25 nm/ 5 nm InGaAs/ InAs with 3.6×10^{19} cm^{-3} active Si doping was grown non-selectively at 400 °C. Then the wafer was then transferred to an electron beam evaporator attached to the MBE under ultra high vacuum, and 20 nm of Mo was deposited.

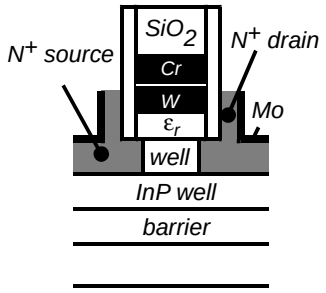


Fig. 4: Cross-section schematic of final device

Both the InGaAs regrowth and Mo are deposited over the top of the gate, shorting the source to the drain. To remove the undesired material, the wafer was planarized by spinning photo-resist and ashed back in an inductively coupled O_2 plasma (ICP) until the tops of the gates were exposed. Then the Mo was dry etched in a SF_6/Ar plasma, and the InGaAs layers were wet etched [11, 12]. The PR was stripped to give a self-aligned S/D MOSFET. Next S/D pads were lifted-off, and devices were mesa isolated and measured by needle probe. A schematic of the scaled InGaAs MOSFET is given in Fig. 4. The self-aligned S/D regrowth ensures the source resistance does not degrade from surface state induced depletion. [13].

The RHEED was spotty during the regrowth on the MOSFET wafer, which indicated a rough surface. We attribute this to InP to InAs conversion during the initial stage of regrowth. [14] The highly strained InAs layer relaxed, and the subsequent InGaAs growth became rough. This phenomenon was confirmed by the failure of the selective Arsenide wet etch to stop on the InP layer after regrowth. Spotty RHEED and rough InGaAs regrowth were

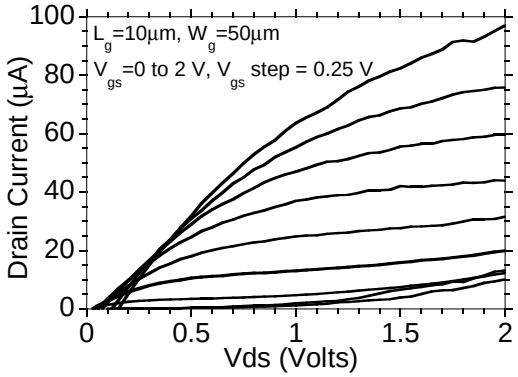
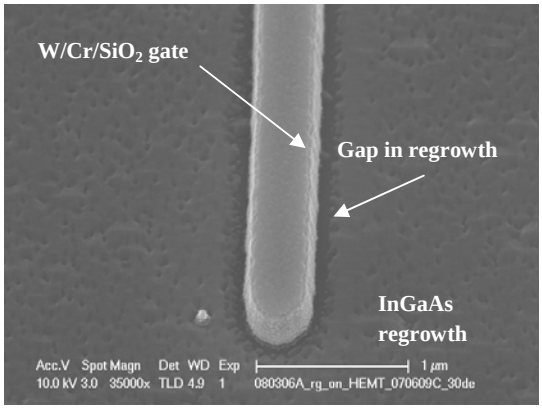


Fig. 5: Measured I_d-V_d of the MOSFET

also observed on unprocessed wafers with thin InP but with no gates. A similar rough surface was observed even in chemical beam epitaxy (CBE) growth. This confirmed that the problem was a growth related issue, rather than process related contamination. Transmission line measurements (TLM) on the regrowth layer gave a high sheet resistance of 310 Ω–µm and a contact resistance of 130 Ω–µm^2. A source resistance of 300 Ω–µm was expected from the TLM data. A low sheet resistance of 28 Ω–µm and contact resistance of 9 Ω–µm^2 were measured on a co-processed wafer with no high-k and no InP, confirming the possibility of high quality regrowth on a processed wafer. We attribute the higher resistance observed in the MOSFET wafer to relaxation and rough growth on the thin InP layer.

Fig. 5 shows the output characteristics of a 10 µm gate length device. The maximum drive current is ~ 2 µA/µm at V_{gs}=2.0 V and V_{ds}=2.0 V. Similar low drive currents were observed for the shorter gate length devices. The I_d-V_g characterstics showed an extremely high source resistance limited linear behavior with R_s~10-100 kΩ. The on resistance is orders of magnitude higher than the value calculated from the TLM structures.

A scanning electron microscope (SEM) image of the device showed a 150-200 nm gap between the n^+ regrowth regions and the gate. Similar gaps in regrowth were observed on co-processed wafers with gates but without high-k (Fig. 6). The gap is most likely due to shadowing by the gate during MBE regrowth and/or by a thin (nm) layer of SiN_x remaining on the surface near the gate even after the sidewall etch. The gap was also observed in process monitor wafers on which no sidewall was deposited. We attribute this to shadowing by the tall gate features as well as reduced surface mobility of group III adatoms at the growth temperature (400 ºC). As a result, the channel surface next to gate is starved of group III elements, resulting in a gap. Without the high doping from regrowth, the channel in the gap region is depleted of all electrons because of the pinning of Fermi-level well below the conduction band edge due to surface states. Furthermore a large undercut in Al_2O_3 dielectric can introduce an additional depleted region between the channel and the source. Fig. 7 shows Id-Vds of a device where the InGaAs channel was not etched. The breakdown voltage is 8 V consistent with an InGaAs breakdown of 20 V/µm [15] for total S/D to gate gap of 400 nm as seen in SEM. Thus we believe the low drive currents resulted from the undoped gaps in regrowth.



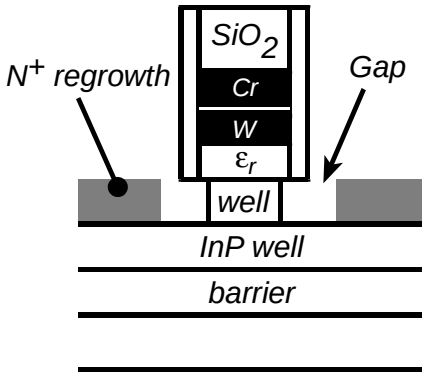


Fig. 6: SEM and schematic image showing a gap in regowth

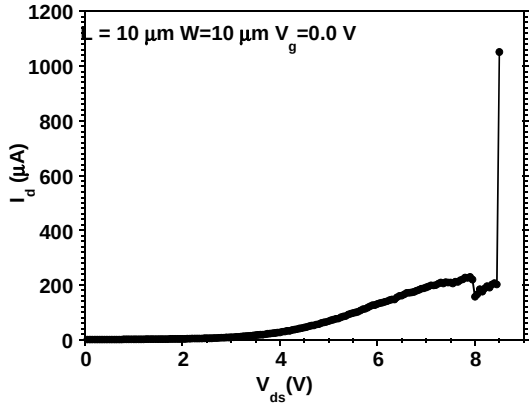


Fig. 7: Break down charcterstics of the MOSFET

The two main reasons for the high source resistance are the inability to re-grow low resistance epitaxial InGaAs on thin InP sub-channel, and a gap region with no regrowth next to the gate. Instead of the thin InP layer, introducing a 2 nm strained $In_{0.88}Ga_{0.12}P$ (InGaP) sub-channel etch stop layer allowed successful regrowth of low resistance InGaAs [11]. A high temperature migration enhanced epitaxy (MEE) regrowth technique showed no gaps next to the gate [16]. Furthermore, a 5-10 nm thick SiN_x sidewall technology is being developed. This would mean a 5-10 nm lateral extension under sidewall, so the MBE regrowth would only need to fill in a horizontal void with a 1:1 or 1:2 aspect ratio.

In summary, we developed a scalable, self-aligned, III-V MOSFET process with MBE S/D regrowth. The gate process and H cleaning leave a 5 nm thick, clean, undamaged, epi-ready channel surface suitable for MBE or MOCVD regrowth. Working devices were fabricated with this process. The devices show low drive current because of undoped gaps between the S/D and the gate in the early devices. Improved high temperature S/D growth techniques have been developed and will be used in the next generation of devices.

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