InGaAs MOSFET with self-aligned Source/Drain by MBE regrowth

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Outline

- **Motivation: III-V MOSFETs**
- **Approach: Self-aligned source/drain by MBE regrowth**
- **FET and Contacts Results**
- **Conclusion**

Why III-V MOSFETs

Silicon MOSFETs:

- Scaling limit beyond sub-22 nm L_g
- Non-feasibility of sub-0.5 nm equivalent oxide thickness (EOT)

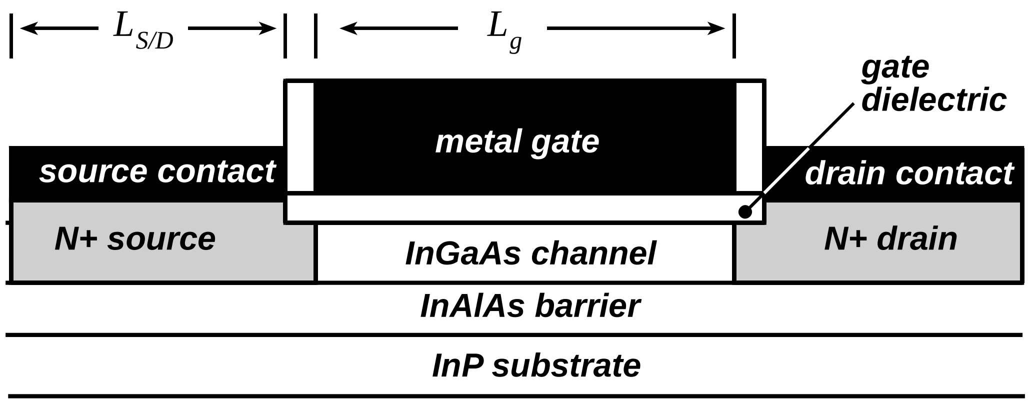
Alternative III-V channel materials

III-V materials$\rightarrow$ lower m*$\rightarrow$ higher velocities (v_{eff})

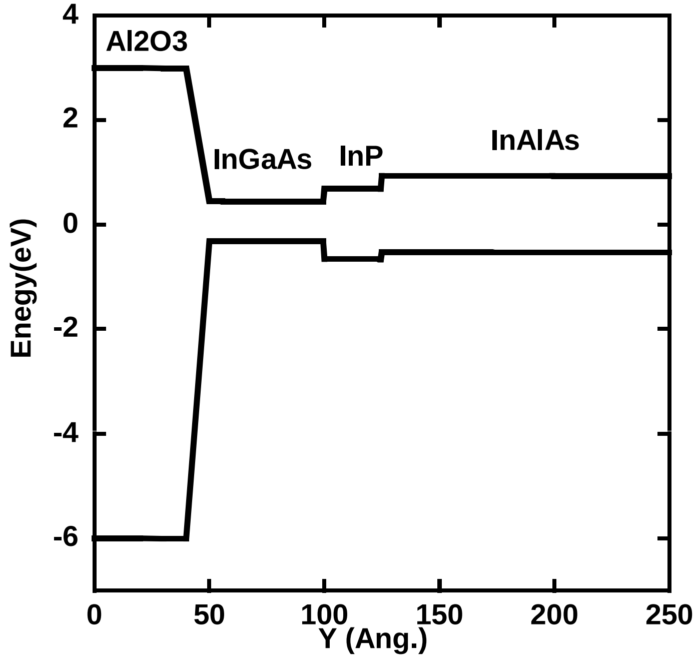
$$I_d / W_g = q n_s v_{eff} \qquad I_d / Q_{transit} = v_{eff} / L_g$$

$$In_{0.53}Ga_{0.47}As : m^* = 0.041 \cdot m, v_{eff} \sim v_{th} = 3.5 \cdot 10^7 \, cm/s$$

22 nm InGaAs MOSFET



Predicted drive current: ~5 mA/μm[1,2]



Key Challenges

- 1 nm EOT gate dielectric
- 5 nm channel with back barrier
- 15 Ω–μm source resistance
- 5×10^{19} cm^{-3} source active doping[2]

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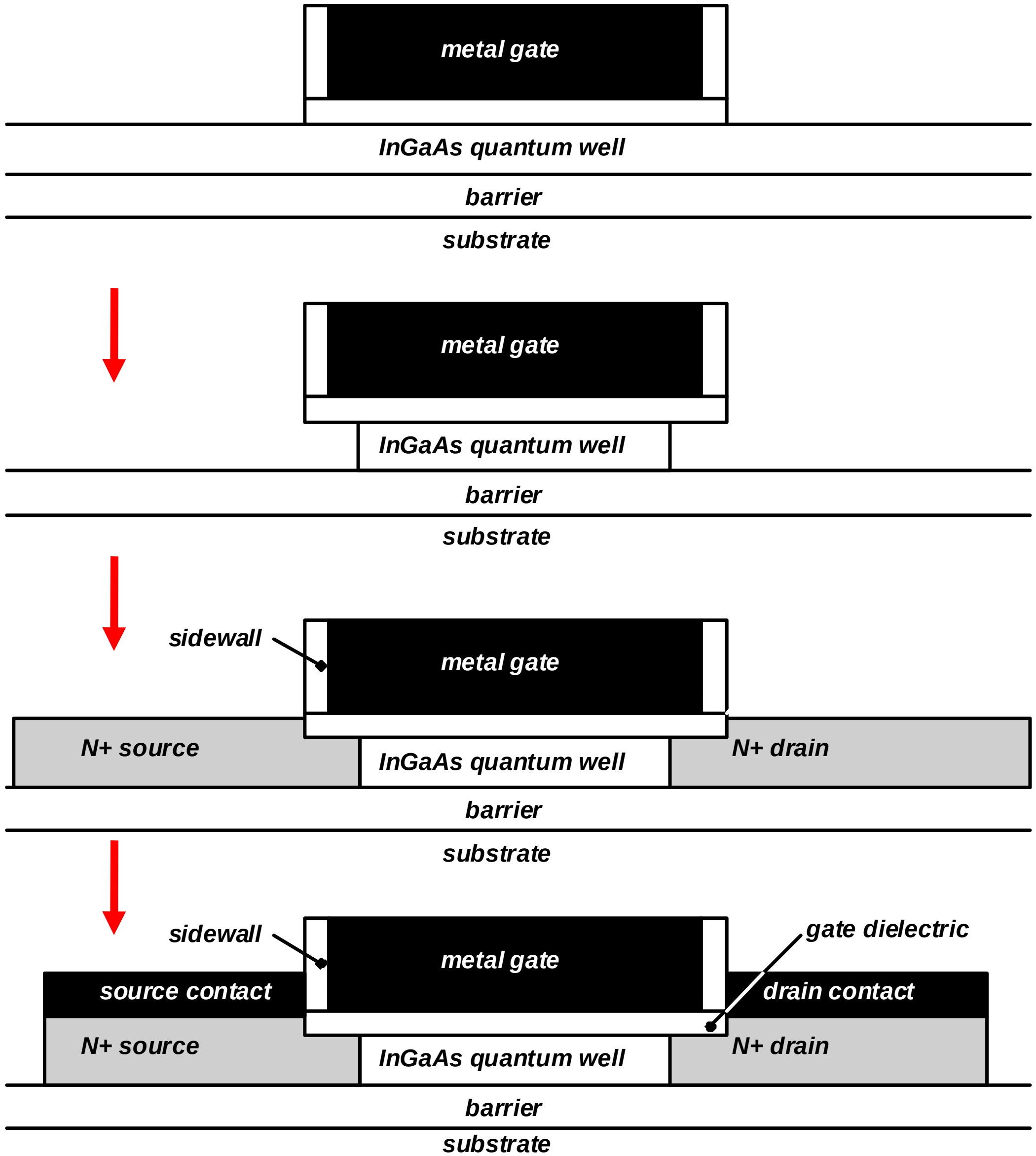
[1] Rodwell. IPRM 2008
[2] Fischetti. IEDM 2007

InGaAs MOSFET with Source/Drain regrowth



Process scalable to 22 nm

Source/Drain defined by MBE regrowth

Regrowth InGaAs, in situ Mo contact Resistance:

*$0.5\ \Omega\text{–}\mu m^2$ ($2.5\ \Omega\text{–}\mu m$)**

* Wistey, EMC 2008

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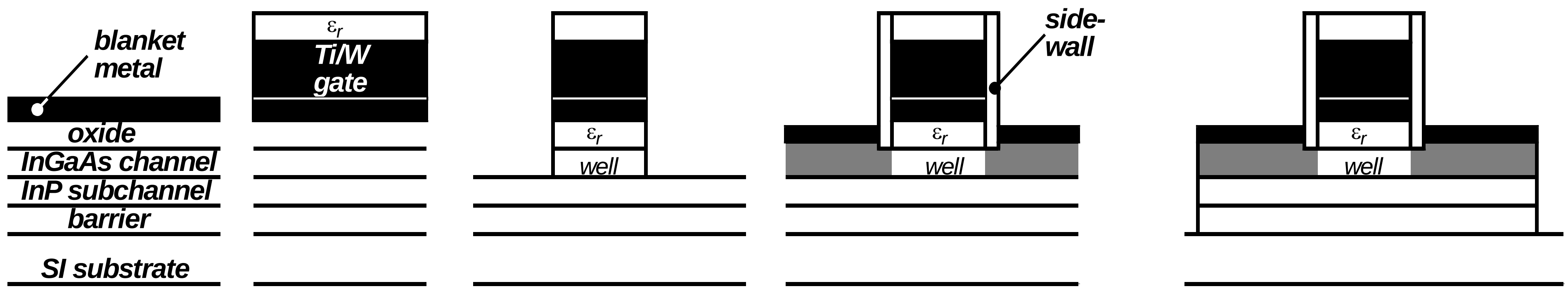
Process flow

Gate definition

Sidewall, Source/Drain



(starting material)

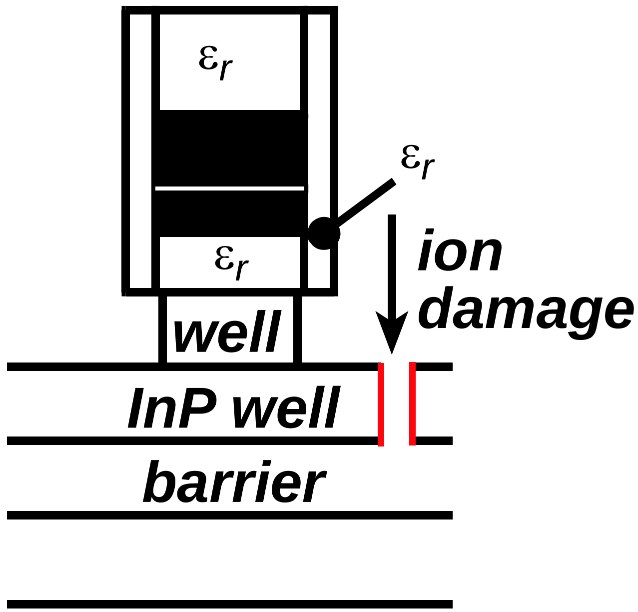
blanket gate deposition

etch gate, etch dielectric etch upper channel

sidewall formation S/D regrowth S/D contacts

mesa isolate S/D

Gate Definition: Challenges

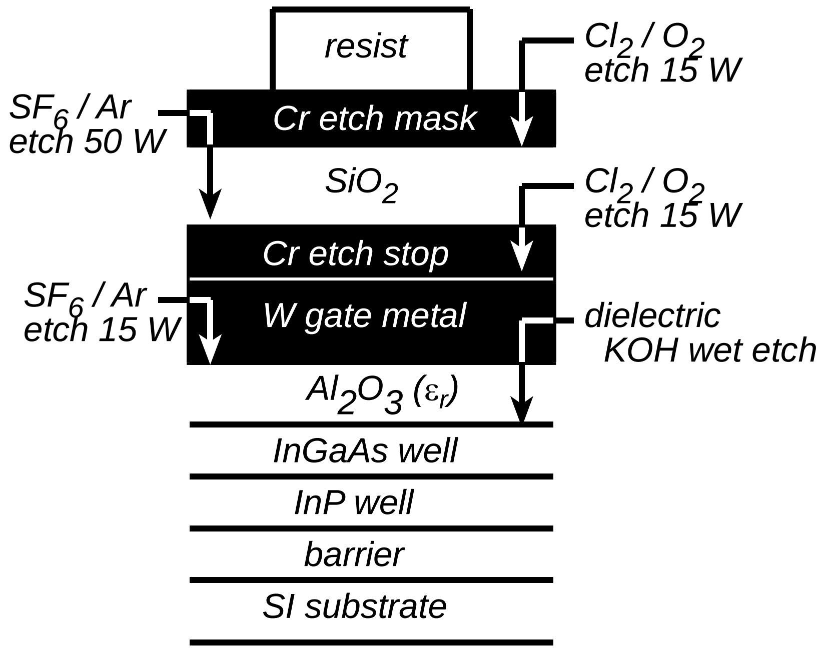


- *Must scale to 22 nm*
- *Dielectric cap surrounding the gate for source/drain regrowth*
- *Metal & Dielectric etch must stop in 5 nm channel*
- *Dry etch must not damage thin channel*

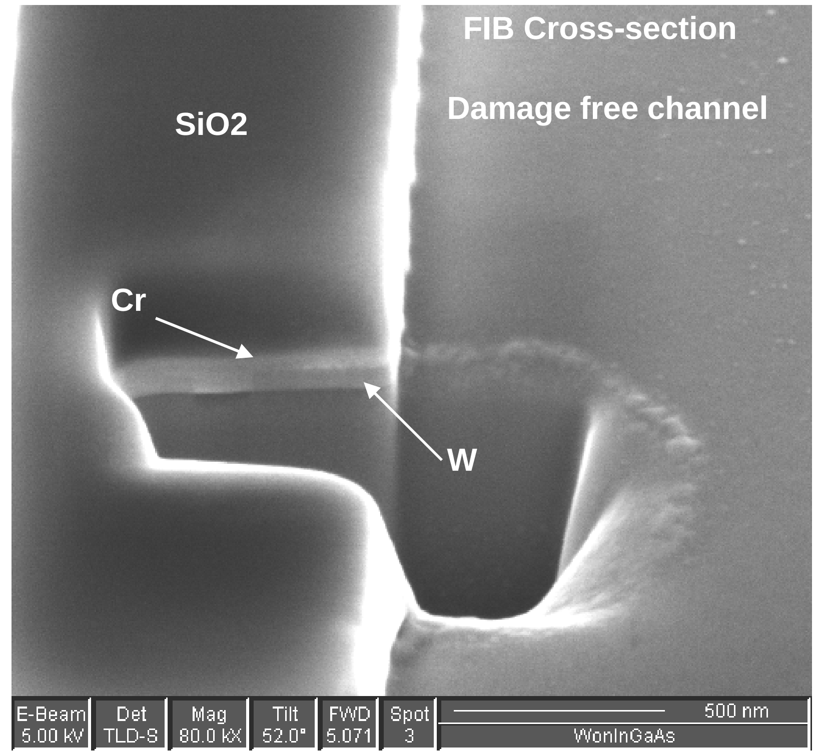
Process must leave surfaces ready for S/D regrowth

Gate Stack: Multiple Layers & Selective Etches

Key: stop etch before reaching dielectric, then gentle low-power etch to stop on dielectric

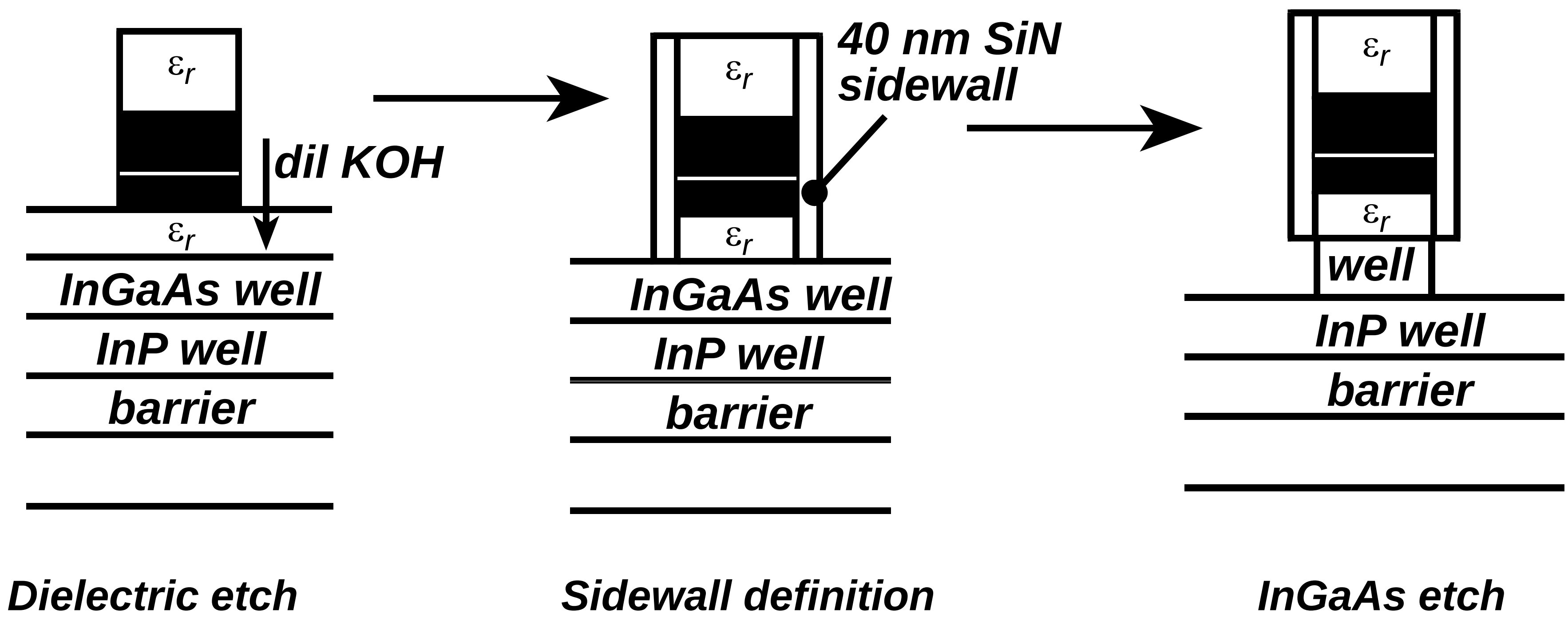


Dry etch scheme



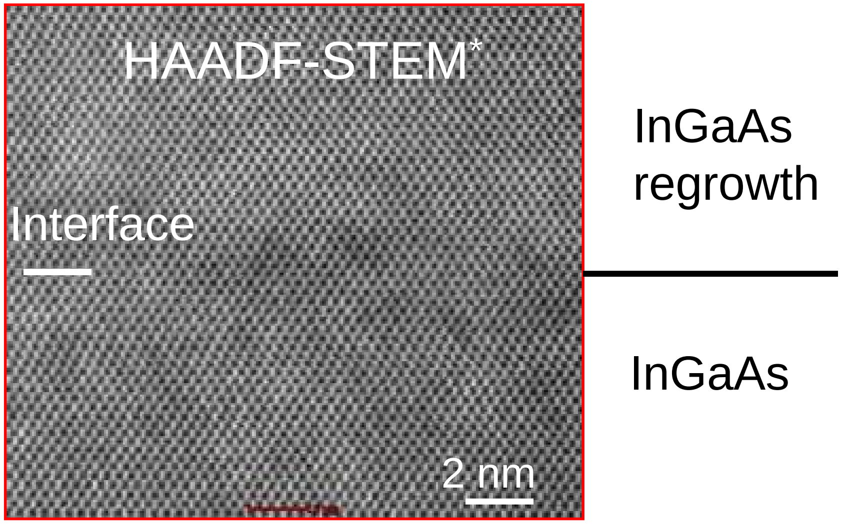
Process scalable to sub-100 nm gate lengths

Dielectric etch and sidewall formation



Surface cleaning before regrowth

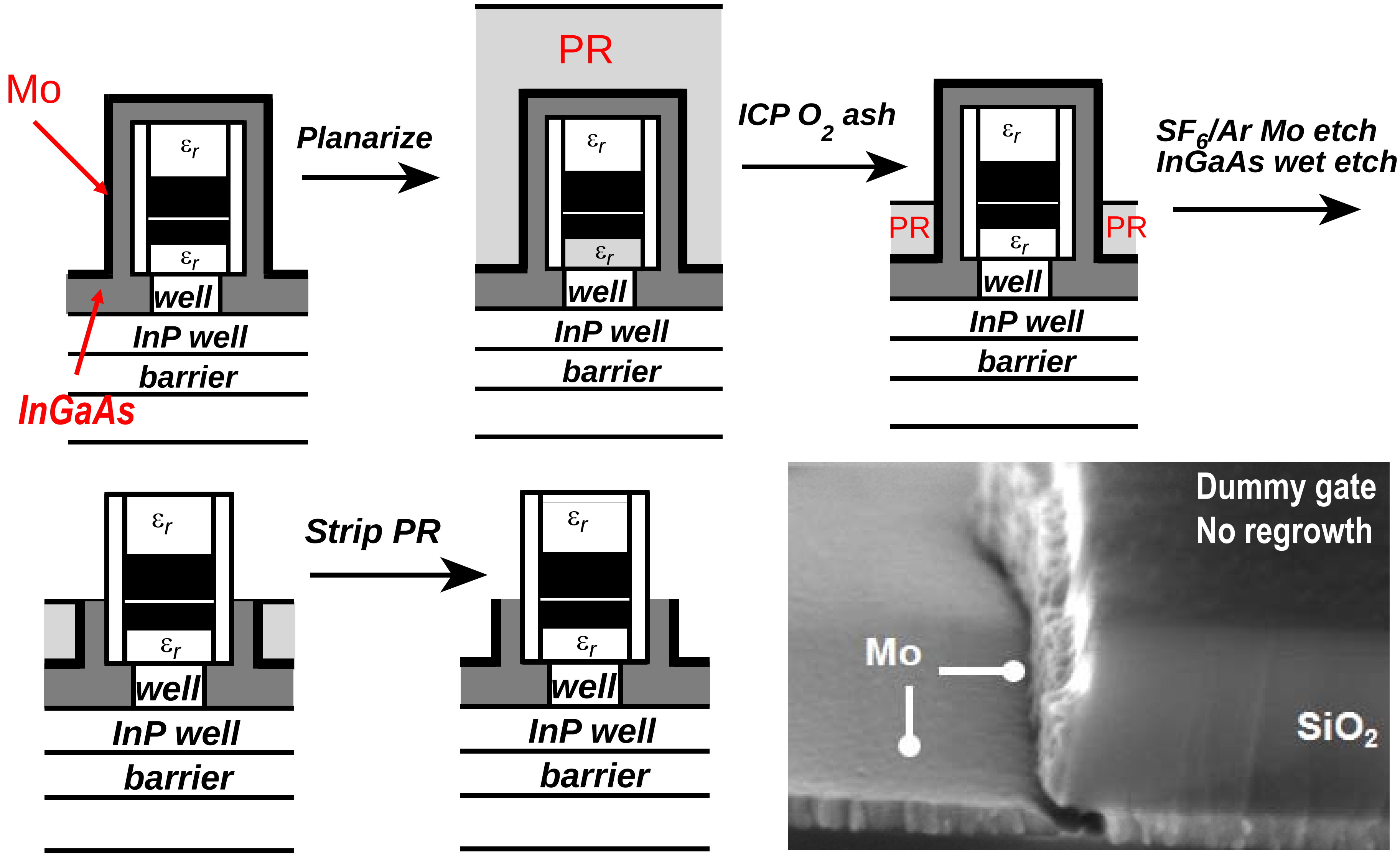
- Clean organics by 30 min UV   Ozone
- Ex-situ HCl:H_2O clean
- In-situ 30 min H clean
- c(4×2) reconstruction before regrowth
- Defect free regrowth



Epi-ready surface before regrowth, defect free regrowth on processed wafer

* Wistey, EMC 2008

Height selective Etching*



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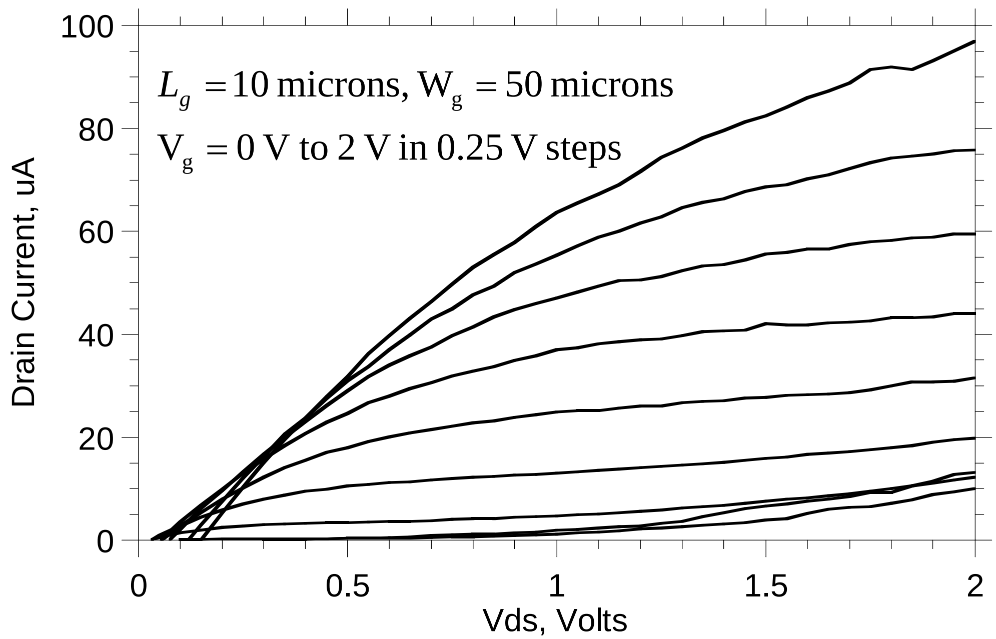
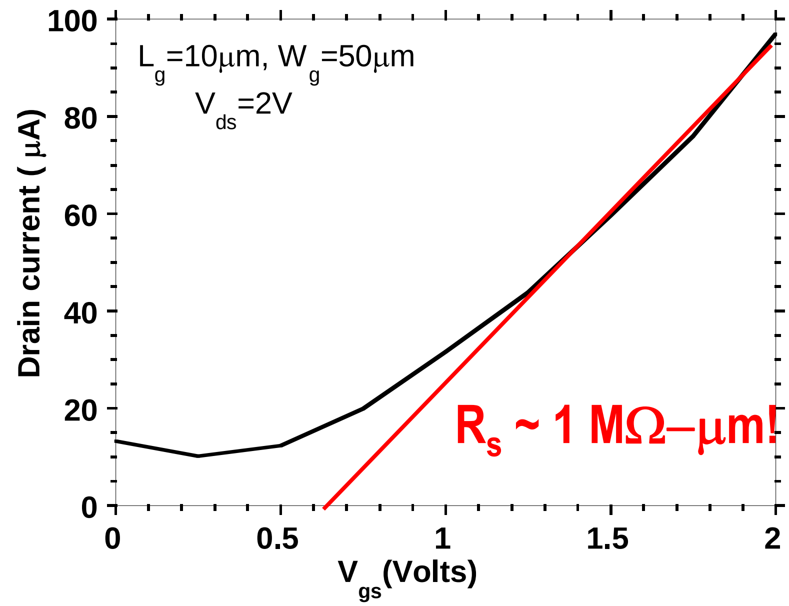
* Burek, J.Cryst.Growth, submitted for publication

MOSFET characterstics

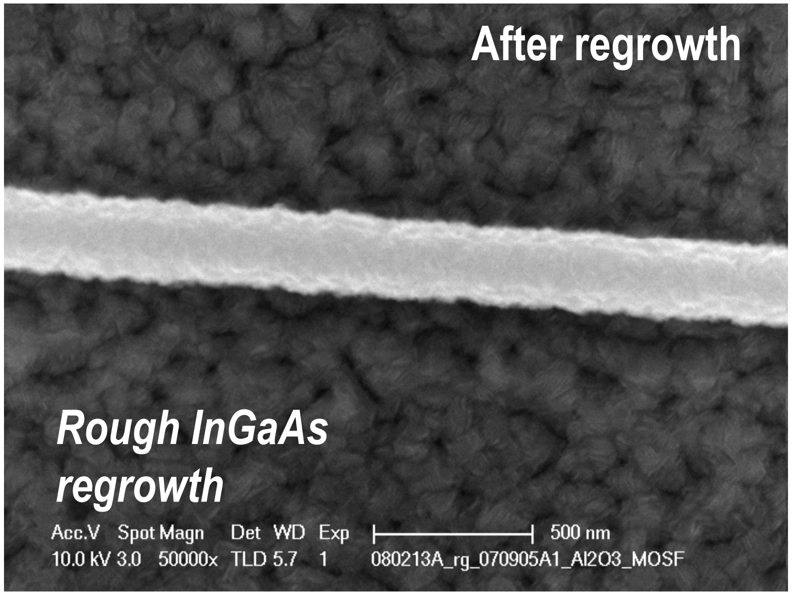


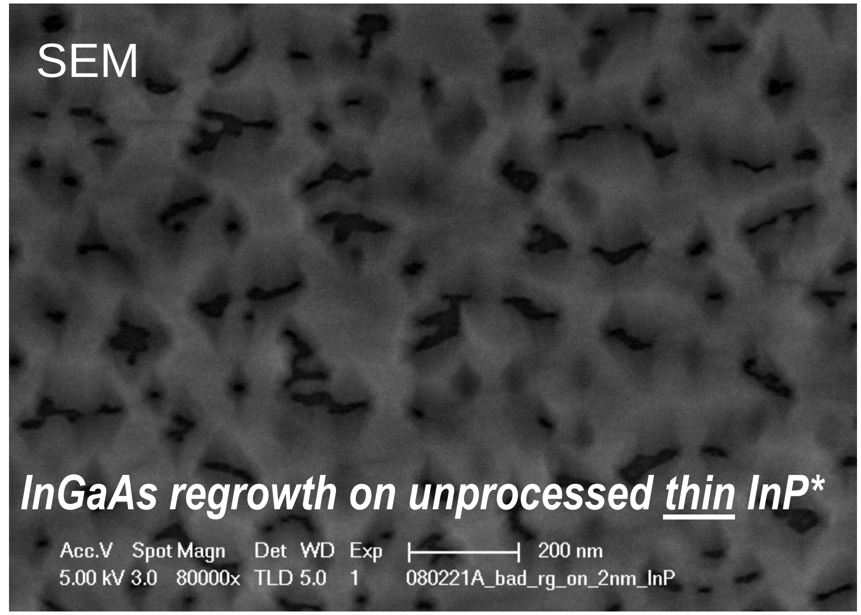


- **Extremely low drive current: 2 µA/µm**
- **Extremely high R_{on}= 10-100 kΩ**

- **Why is R_s so high?**

Source Resistance 1: Poly Growth on InP





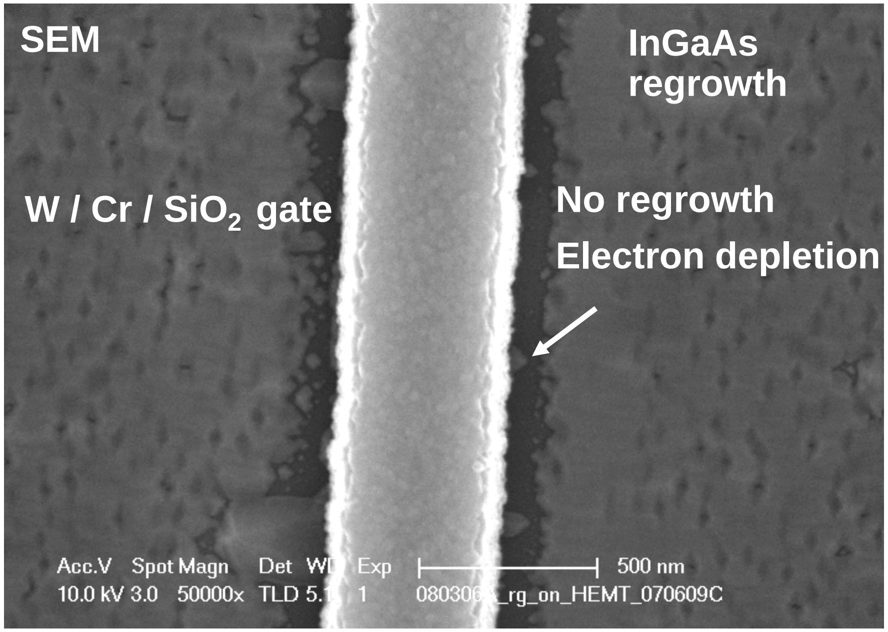
- **Spotty RHEED during regrowth: faceted growth**
- **InP desorbs P during hydrogen clean or regrowth: InP converts to highly-strained InAs***

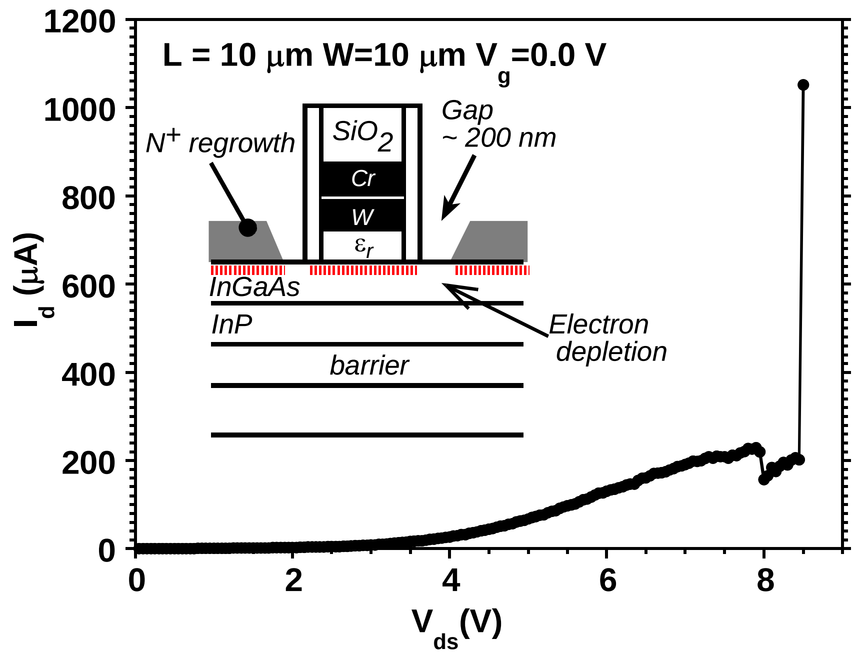
- **From TLM measurement, R_{sh}= 310 $\Omega/\square$, ρ_c=130 $\Omega-\mu m^2$ and R_s= 300 $\Omega-\mu m$**

Sheet resistance doesn't explain 1 MΩ-µm source resistance.

* Wistey (in preparation)

Source Resistance 2: Gap in Regrowth





- No regrowth within 200 nm of gate because of shadowing by gate
- Gap region is depleted of electrons
- Breakdown at Vg=0V, ~ 8V, consistent with 400 nm gap and InGaAs breakdown field of 20V/μm*

High source resistance because of electron depletion in the gap

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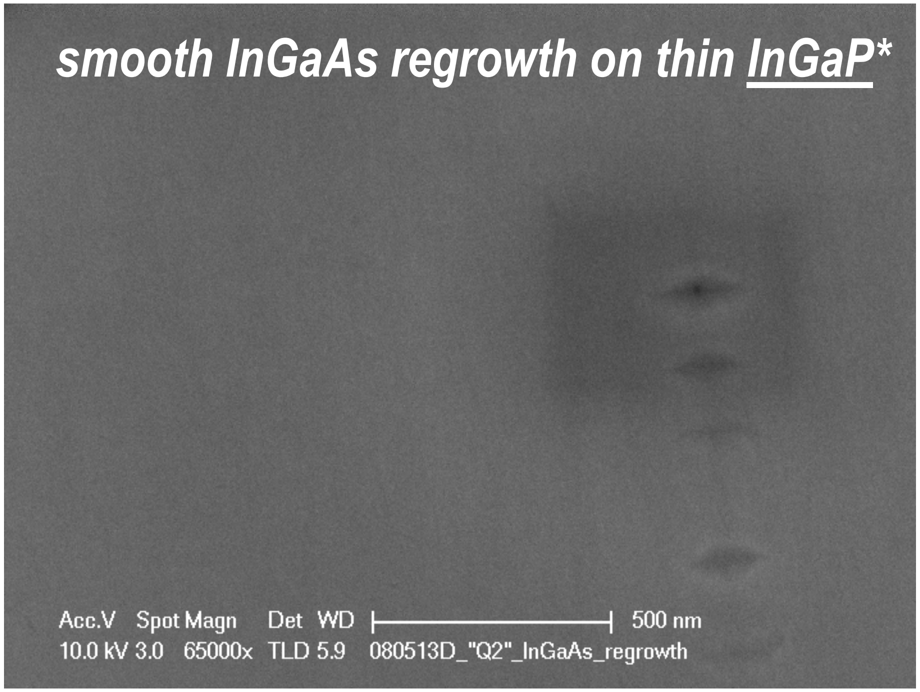
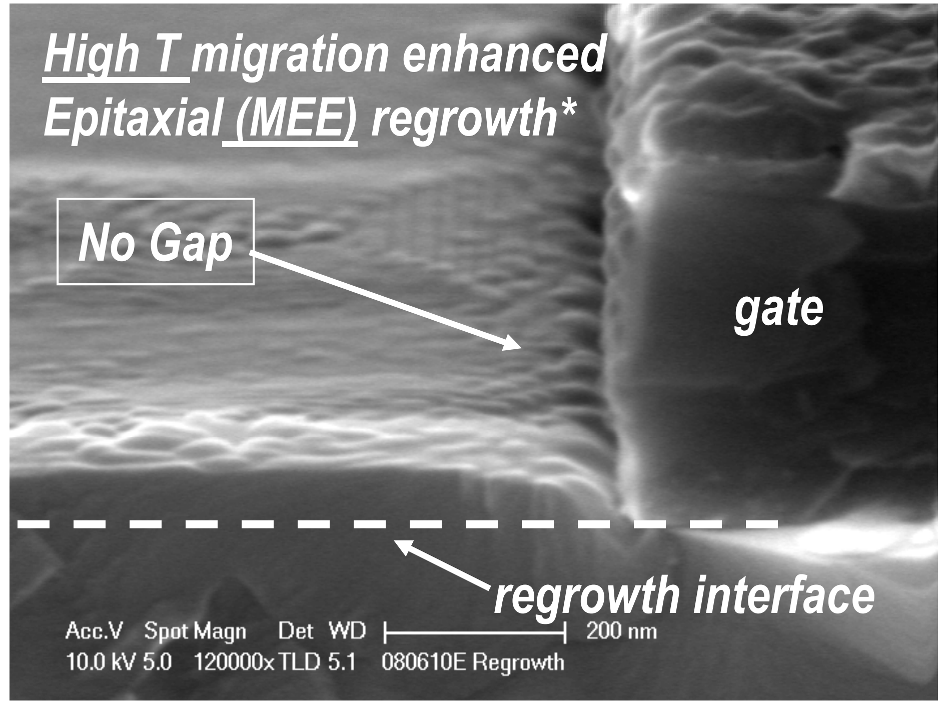
*http://www.ioffe.rssi.ru/SVA/NSM/Semicond/

Regrowth: Solutions





*Wistey, EMC 2008
Wistey, ICMBE 2008

Conclusion

- Scalable III-V MOSFET process with self-aligned source/drain with MBE regrowth
- Gate proces and H clean leave a epi-ready 5 nm channel
- Low drive current in initial devices because of break in regrowth
- Improved regrowth techniques in next generation of devices

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