A High-Linearity, LC-Tuned, 24-GHz T/R Switch in 90-nm CMOS

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ABSTRACT — **This paper presents an LC-tuned, 24-GHz single-pole double-throw (SPDT) transmit/receive (T/R) switch implemented in 90-nm CMOS. The design focuses on the techniques to increase the power handling capability in the transmit (Tx) mode under 1.2-V operation. The switch achieves a measured P_{-1dB} of 28.7 dBm, which represents the highest linearity, reported to date, for CMOS millimeter-wave T/R switches. The transmit and receive (Rx) branches employ different switch topologies to minimize the power leakage into the Rx path during Tx mode, and hence improve the linearity. To accommodate large signal swing, AC floating bias is applied using large bias resistors to all terminals of the switch devices. Triple-well devices are utilized to effectively float the substrate terminals. The switch uses a single 1.2-V digital control signal for T/R mode selection and for source/drain bias. The measured insertion loss is 3.5 dB and return loss is better than –10 dB at 24 GHz.**

***Index Terms* — CMOS transmit/receive (T/R) switch, triple-well, 1-dB compression point, floating substrate.**

I. INTRODUCTION

Recently, a fully integrated 24-GHz multi-channel phased-array transceiver has been reported using 0.13-μm CMOS [1]. The 4-channel, 8-antenna system showcases the high-frequency performance and integration capability offered by advanced CMOS processes. At millimeter-wave (mm-wave) frequencies, multi-input-multi-output (MIMO) system architectures are often adopted to achieve directivity gain to boost transmission range. While the transceiver size can be reduced through integration, the overall system form factor is still dominated by the antenna array size. This limitation is especially problematic at the lower mm-wave frequency band. For the 24-GHz ISM band, the antenna size and spacing between array elements are typically on the order of 1 cm. Therefore, it is advantageous to integrate the T/R switches and as much as feasible the matching networks on chip to reduce the board-level complexity for interfacing to the antennas and hence reduce the overall system size.

Most CMOS T/R switches reported in literature are limited to operations below 20 GHz [2]–[5]. Switch designs at 24 and 60 GHz have been reported but their linearities (P_{-1dB}) are limited to less than 5 dBm [6][7]. In this paper, we present a 24-GHz T/R switch design with a combination of linearity enhancement techniques. The prototype is implemented in IBM's 90nm CMOS process, which offers 1.2-V NMOS with 120-GHz f_T and 250-GHz f_{max} [8].

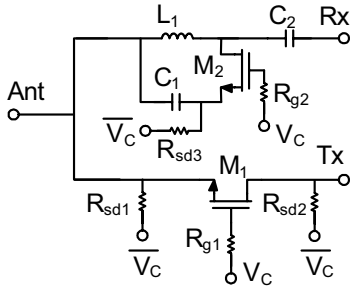

Figure 1. Schematic of the LC-tuned, SPDT T/R switch.

Triple-well (TW) NMOS is a standard feature in this technology and is employed to reduce signal loss to the substrate [5][6]. This paper is organized as follows. First, the design and operation of the asymmetric switch topology between Tx and Rx branch will be described. Trade-off between linearity, switching speed, insertion loss (IL), and isolation will then be analyzed. Finally, measurement results versus simulation prediction along with performance benchmark against published results will be presented.

II. T/R SWITCH DESIGN

Achieving high linearity is more critical for Tx mode than for Rx because the outgoing transmitted power level can be as high as 20–30 dBm, while the incoming received signal from the antenna is typically less than –40 dBm. Since transmit and receive power handling requirement are quite different, an asymmetric switch design is exploited. Figure 1 shows the schematic of the T/R switch. In the Tx path, a series switch (M_1) is used whereas a shunt switch (M_2) is employed in the Rx path. A 1.2-V digital control signal, V_C, is applied to the gate of the switches to select Tx or Rx mode operation.

Series gate bias resistors, R_{g1} and R_{g2}, are used, so the gate potential is bootstrapped to the source and drain. This essentially floats the gate at AC which is a common practice in T/R switch design to prevent power loss into the gate terminal [2]–[5]. To determine the proper value of R_g, the trade-off between P_{-1dB} and the 10%-to-90% turn-on switching time (T_{sw}) is examined for M_1, as shown in Figure 2(a). The W/L of M_1 is 160μm/80nm, which presents a gate capacitance of 180 fF. For R_g less than 5 kΩ, P_{-1dB} starts to decrease with R_g. In this T/R switch design, R_g of 30 kΩ is chosen to minimize power loss to the

gate terminal while keeping T_{sw} less than 10 ns. The proper sizing of M_1 is determined based on the trade-off of the on-resistance (R_{on}) in the triode region, which affects insertion loss, and C_{sd} in cut-off region, which affects isolation, as illustrated in Figure 2(b). With the chosen width of 160 μm for M_1, the R_{on} is 2.4 Ω and the C_{sd} is 75 fF according to simulations. The measured insertion loss and isolation will be presented in the next section.

The source and drain voltages ($V_{S/D}$) of M_1 and M_2 are biased using the inverted V_C ($\overline{V_C}$ in Figure 1) through large bias resistors (R_{sd1}–R_{sd3}). In Tx mode, V_C is set at 1.2 V, so $V_{S/D}$ of M_1 and M_2 is at 0 V. The Rx path presents a parallel resonant tank with L_1 and C_1 shorted through M_2. The large bias resistor R_{sd3} causes the source terminal of M_2 to be floating. This keeps the impedance between M_2's source and drain small even under large signal swings at the antenna node. As a result, the Q of the L_1C_1-tank remains sufficiently high to effectively block out leakage power from the Tx branch. The L_1C_1-tank impedance at 24 GHz is about 700 Ω. Based on simulation, a 2-dB improvement in the Tx P_{-1dB} is observed with the insertion of R_{sd3}. If a series switch topology is used symmetrically in both Tx and Rx branch [3]–[5], the impedance looking into the Rx branch will be limited by the source-to-drain capacitance (75 fF) which is much lower than the L_1C_1-tank impedance in our design. Also, large signal swings at the antenna port in Tx mode can potentially turn on the series Rx switch which further limits the power handling capability of the symmetric topology.

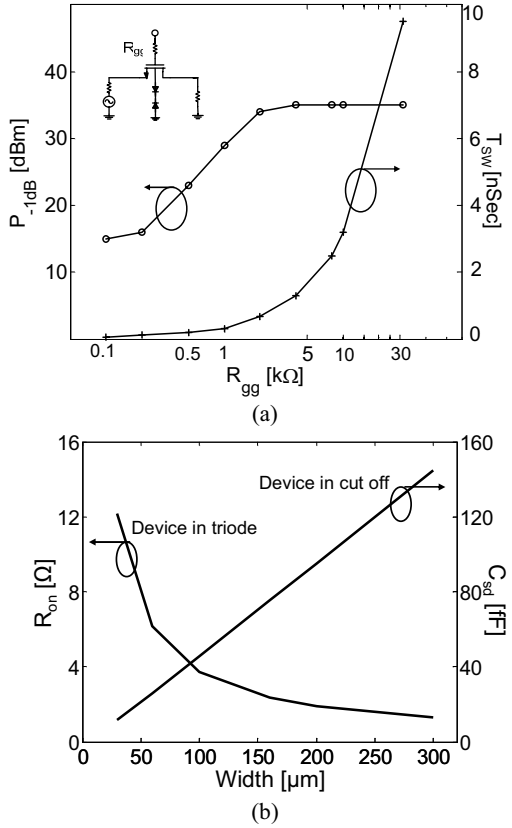

Figure 2. (a) Trade-off between P_{-1dB} and the 10%-to-90% turn-on switching time in Tx mode as a function of series gate bias resistance for M_1 (160μm/80nm). (b) Trade-off between on-resistance (insertion loss) and source-to-drain capacitance (isolation) as a function of switch device width.

In Rx mode, both M_1 and M_2 are turned off with V_C set to 0 V, so $V_{S/D}$ of M_1 and M_2 is at 1.2 V. As M_2 is shut off, L_1 and C_2 form a series LC-resonant matching network to the receiver input. With the source terminal of M_2 floating due to R_{sd3}, the source-to-drain capacitance of M_2 is bootstrapped. Simulation result confirms that R_{sd3} improves the IL in Rx mode by 0.3 dB. The drain-to-body junction capacitance of M_2 is also bootstrapped with the floating body terminal.

While the gate, source, and drain terminals of the switch transistor can be floated at AC using large bias resistors, floating the body terminal is more difficult. Directly floating the P-substrate node can lead to a latch-up hazard. An LC-tuned substrate bias network was proposed to alleviate this problem at the cost of larger chip area due to an additional space separation to substrate contacts and an extra inductor [2]. As TW becomes a standard feature in scaled CMOS processes, using TW NMOS for T/R switch is a more effective implementation choice. Figure 3 shows the cross section of TW NMOS with AC floating bias resistors, R_{b1} and R_{b2}, for P-well and D-nwell, respectively. It is important to float both the P-well and the D-nwell in order to bootstrap both the source/drain/P-well junction and the P-well/D-nwell junction [5]. While the D-nwell/P-sub junction is not bootstrapped (since P-sub is tied to ground direclty), the necessary voltage swing to turn on this junction is very high. The substrate impedance of a TW device (Z_{TW}) should be high enough to provide proper substrate isolation, thus less power leakage to the substrate. The Z_{TW} is capacitive because at least one of junctions between the P-well/D-nwell and D-nwell/P-sub is reverse-biased even in the presence of large signal swings. The size of the TW switch devices dictates the P-well area which directly affects the Z_{TW}. By limiting the P-well area, the $|Z_{TW}|$ at 24GHz is kept at 650 Ω, which is more than 10 times greater than the 50-Ω termination.

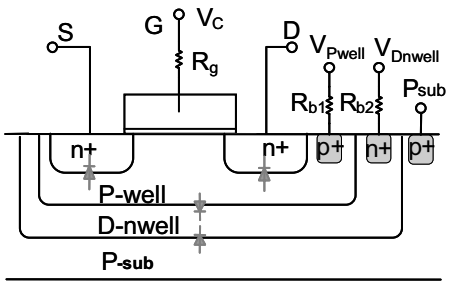

Figure 3. Cross section of triple-well NMOS (M_1 and M_2) with bias resistors to float the gate, P-well and D-nwell at AC.

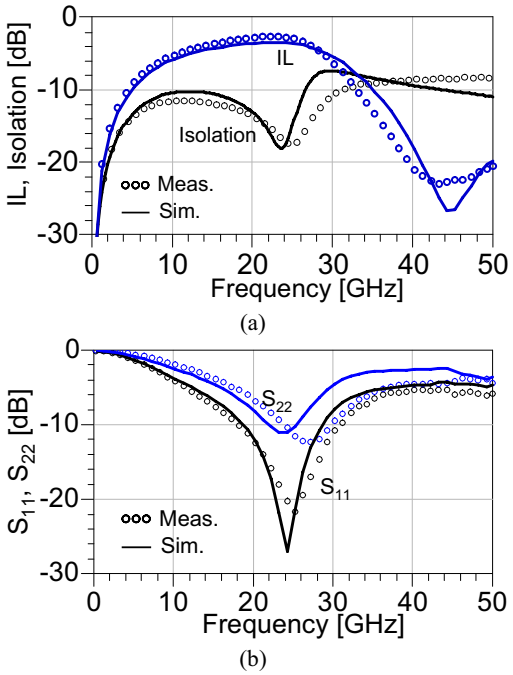

Figure 4. Measured vs. simulated results in Rx mode. (a) Insertion loss and isolation. (b) Matching at the Ant port (S_{11}) and Rx port (S_{22}).

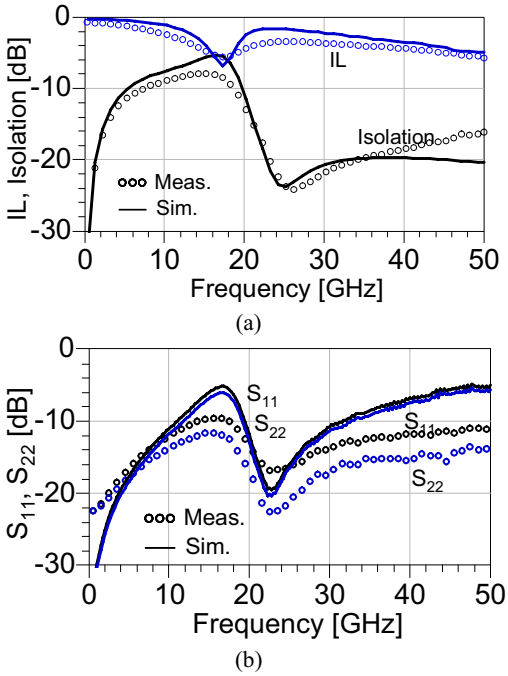

Figure 5. Measured vs. simulated results in Tx mode. (a) Insertion loss and isolation. (b) Matching at the Tx port (S_{11}) and Ant port (S_{22}).

III. Measurement Results

In Figure 4(a), the Rx mode IL and isolation of measurement and simulation are plotted up to 50 GHz. The measured IL between Rx and Ant port is 3.5 dB at 24 GHz which is within 0.5 dB of the simulated value. The isolation between Rx and Tx port is 16 dB at 25 GHz. The measured and simulated return loss at the Ant and Rx port, S_{11} and S_{22}, respectively, are plotted in Figure 4(b). Despite the slight mistuning of the L_1-C_2 series resonant frequency, the return loss is still better than –10 dB at 24 GHz.

Figure 5(a) shows the comparison for IL and isolation in Tx mode. The measured Tx IL at 24 GHz is 3.4 dB. This is 2 dB worse than the simulated value and can be attributed to the additional loss in the source/drain junction capacitance of M_1 and in the series routing interconnect which need to be better modeled. The measured return losses at both the Tx and Ant ports are better than –15 dB at 24 GHz as shown in Figure 5(b). The measured P_{out} vs. P_{in} in Tx mode is plotted in Figure 6 from which the P_{-1dB} of 28.7 dBm is extracted. The two main losses in the Tx mode are the on-resistance of M_1 (R_{on} ~ 2.4 Ω) and the power leakage into the Rx path. In the Tx mode, M_2 in the Rx path should remain in a low-impedance state (R_{on} ~3.7Ω) to make the L_1C_1-tank high impedance. This prevents Tx signal from leaking into the Rx path. However, as the transmit power approaches P_{-1dB}, the instantaneous V_{gs} and V_{gd} fluctuations in M_2 increase its effective R_{on}. This lowers the L_1C_1-tank impedance and consequently, power leaks into the Rx path.

Table 1 compares the performance of this work with that of other RF and mm-wave CMOS switches. This work achieves the highest linearity and the smallest chip area among the reported switches to date operating at above 20 GHz. Figure 7 illustrates the layout and chip photo of the switch presented. The switch occupies merely 110x160 μm^2 of chip area. The TW NMOS devices, M_1 (160µm/80nm) and M_2 (100µm/80nm), are laid out as multi-finger devices with a 10-µm finger width since the device gate resistance is absorbed as part of R_g. A

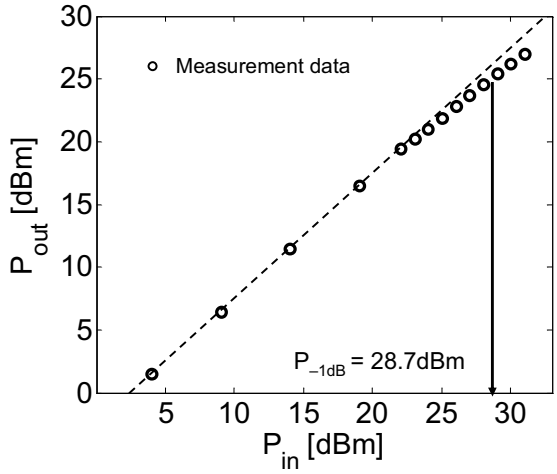

Figure 6. Measured P_{out} vs. P_{in} in Tx mode.

symmetric inductor, L_1 (350 pH), with a measured Q of 8.5 at 24 GHz is used. The capacitors, C_1 (105 fF) and C_2 (100 fF), are inter-layer metal-oxide-metal capacitors that utilize Metal1 through Metal8. Non-silicided p+ polysilicon resistors (30 kΩ) are used for the bias resistors R_{g1-2}, R_{b1-2}, and R_{sd1-3}.

IV. Conclusion

In summary, we have presented the design of a 24-GHz SPDT T/R switch that achieves the highest linearity (28.7dBm of P_{-1dB}) among CMOS switches for mm-wave applications. The switch utilizes a single 1.2-V digital control signal to select Rx/Tx mode and to set the source/drain bias of the switch devices. The design is well suited for integration with multi-channel transceiver to reduce the overall system size and cost.

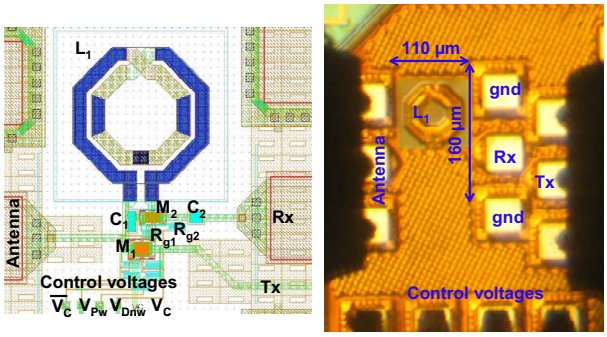

Figure 7. Layout and die photo of the T/R switch.

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Table 1. Summary of this work and comparison with reported T/R switch designs.

Frequency	Key Performance			Technique, Chip area, Control voltage	Technology	Ref.
	P_{-1dB}	IL	Tx-Rx Isolation			
5.2 GHz	28 dBm	1.52 dB (Tx) 1.42 dB (Rx)	30 dB (Tx) 15 dB (Rx)	LC tuned bias, 0.56 mm^2, V_{cont} 1.8V	0.18-µm CMOS	[2] ISSCC03
15 GHz	21.5 dBm	1.8 dB (Tx)	17.8 dB	Impedance transform, 0.20 mm^2, V_{cont} 1.2V 3V	0.13-µm CMOS	[3] JSSC05
DC ~ 20GHz	22.6 dBm	2.5 dB (20GHz) 7.5 dB (24GHz)	25 dB	Floating well, 0.058 mm^2, V_{cont} 1.8V, 3.6V	0.18-µm Triple-well CMOS	[4] MTT07
DC ~ 20GHz	27 dBm single-ended	2.0 dB (20GHz)	22 dB	Floating well,0.03 mm^2, V_{cont} 0V, 2V	0.13-µm Triple-well CMOS	[5] JSSC07
24 GHz	0.5 dBm	Gain 1.9 dB NF 11.3dB	42 dB	Active switch, 0.55 mm^2, V_{DD} 5V, P_{diss} 120mW	0.5-µm SiGe BiCMOS	[6] RFIC04
57~66 GHz	4.1 dBm	4.5~5.8 dB	24~26 dB	Impedance transform, 0.22 mm^2, V_{cont} 0V, 1.2V	0.13-µm CMOS	[7] RFIC07
24 GHz	**28.7 dBm**	**3.4 dB (Tx) 3.5 dB (Rx)**	**22 dB (Tx) 16 dB (Rx)**	**Floating well, 0.018 mm^2, V_{cont} 0V, 1.2V**	**90-nm Triple-well CMOS**	**This work**