Planarization and Regrowth of Self-Aligned Ohmic Contacts on InGaAs

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Outline

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- Motivation: Can InGaAs MOSFETs beat Si?
  - Contact resistance is key: $R_c \sim 1 / f^2$
- Planarization & Etchback — Self-aligned
- Regrown Low Resistance Contacts and MEE
- InGaP Etch Stop Layer
- Conclusions

In Order to Beat Silicon...

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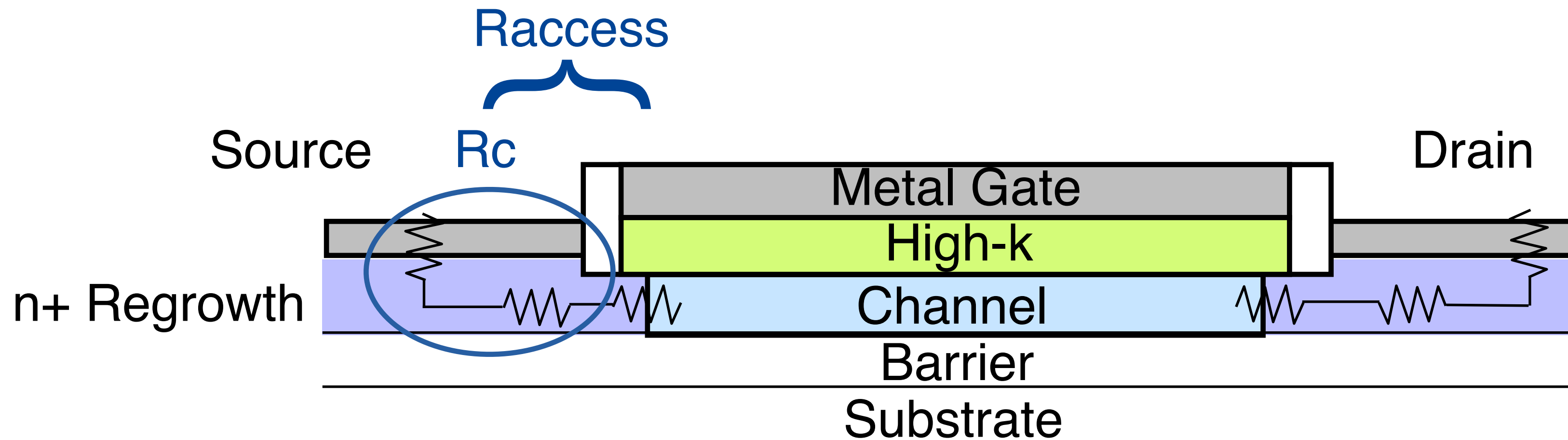

Target...		Strategy...
R_{sd} = 180 Ω-μm		$In_xGa_{1-x}As$ channel
I_{ds} = 6 mA/μm & low gate leakage		High gate barrier: MOSFET
L_g = 22 nm, low SD leakage		High back barrier: AlGaAs
R_c = 1 Ω-μm² (10^{-8} Ω-cm²)	**Rc ~ 1 / f²**	Regrow S/D epitaxially.*
R_{access} = 10 Ω-μm		Backfill channel recess etch.*

***Major challenges for MBE.**

Source: Rodwell IPRM 2008

Surface Cleaning for Regrowth

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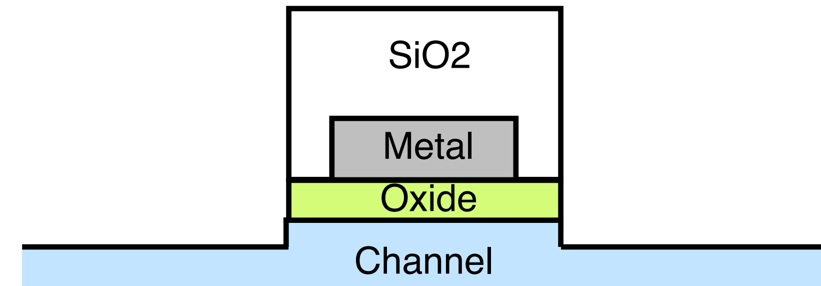
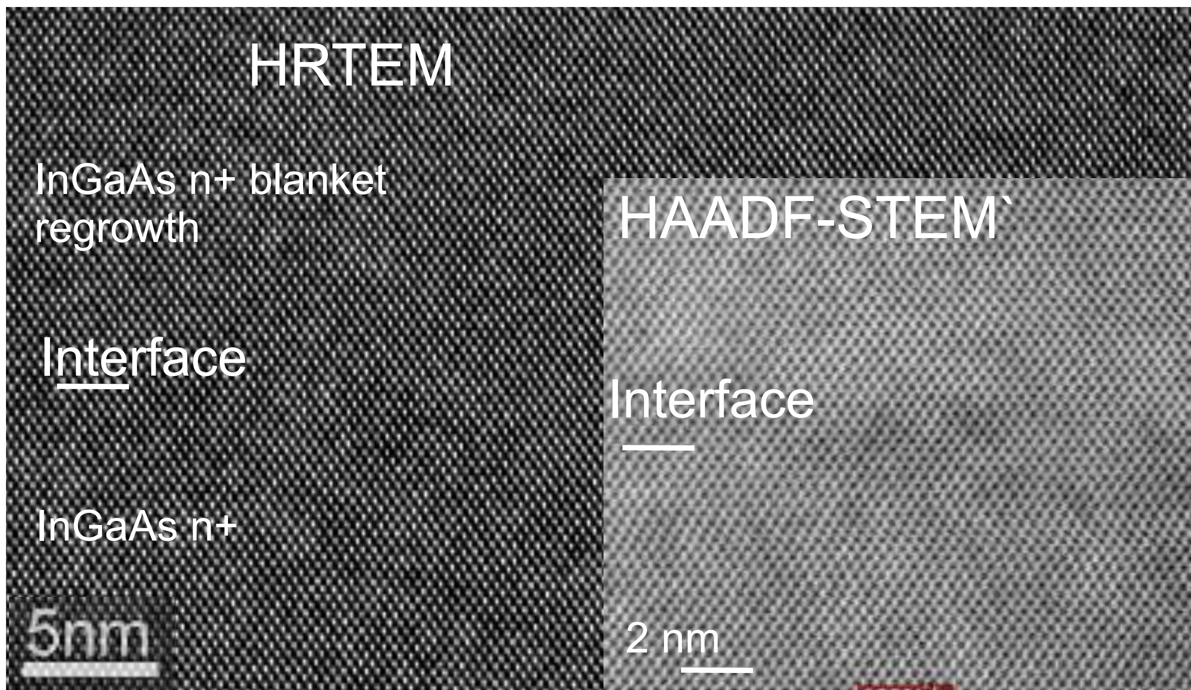
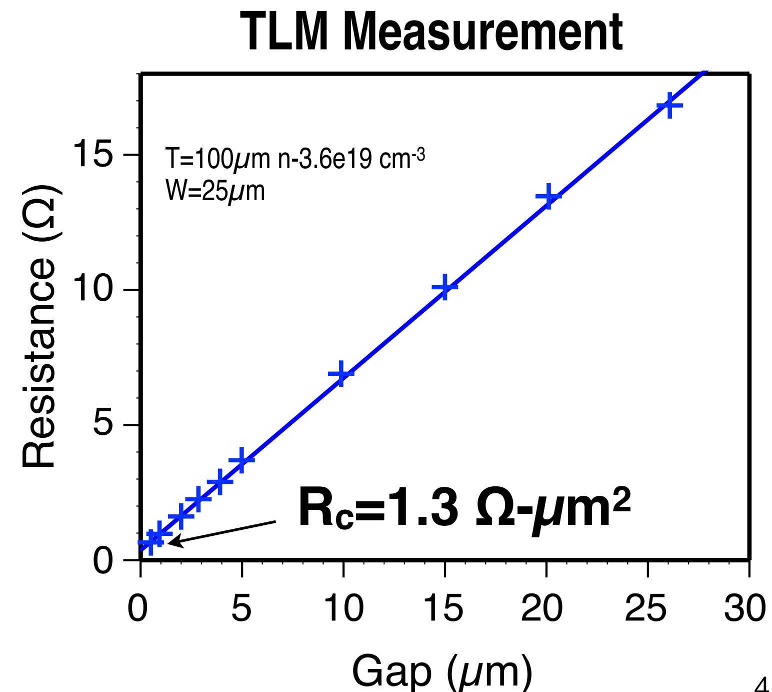
- **Encapsulate all gate metals**
- **Surface clean:**
  - Recess etch
  - UV ozone 30min
  - 1:10 HCl:H_2O for 1 min, DI rinse
  - UHV bake 200°C
  - H clean or thermally desorb oxide
- **No extended defects, low contact resistance: 1.3 Ω-μm^2**

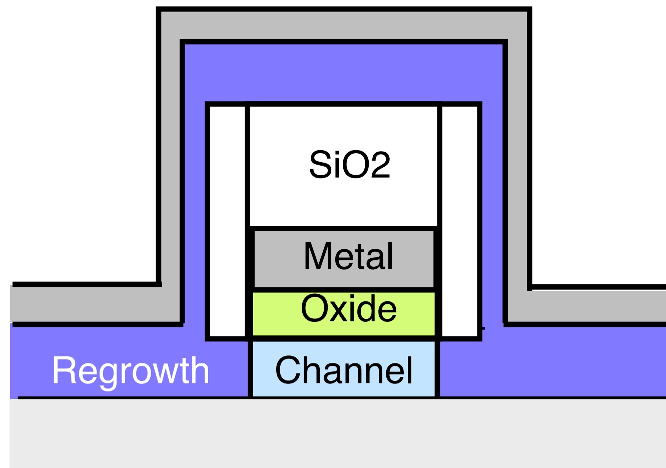


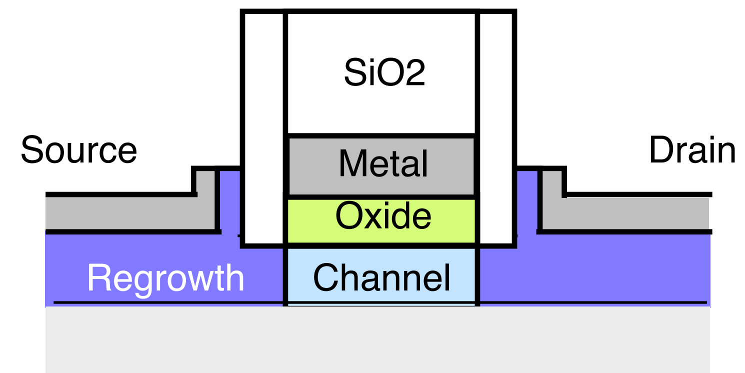




Planarization & Etchback

- **Goal: self-aligned, selective area contacts**





Planarization & Etchback

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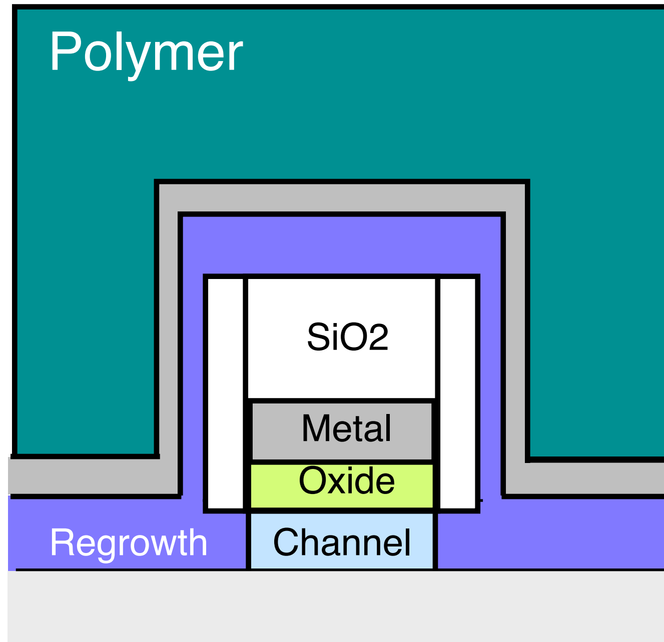
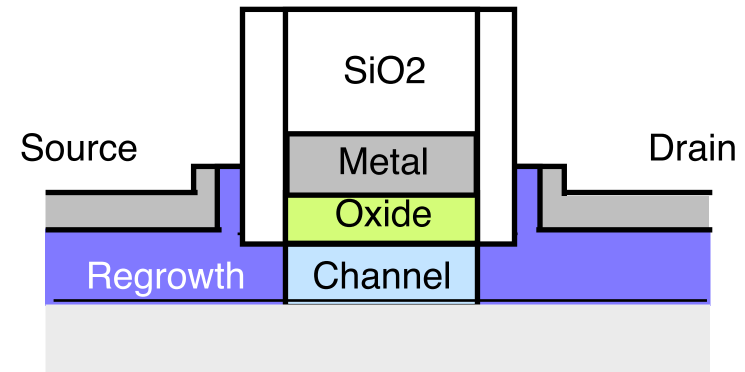
- **Goal: self-aligned, selective area contacts**

1. Spin on thick polymer





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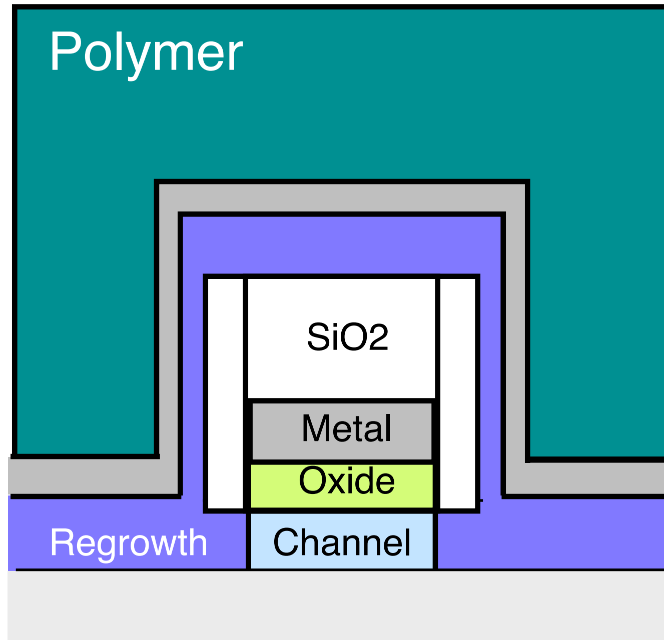
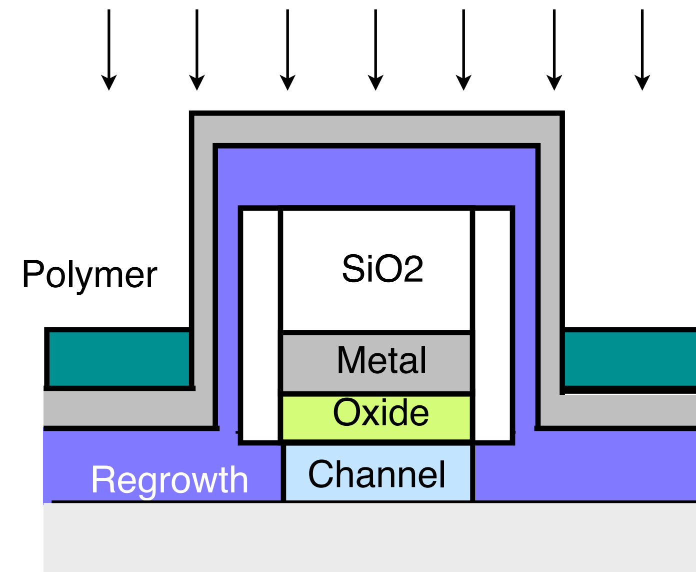
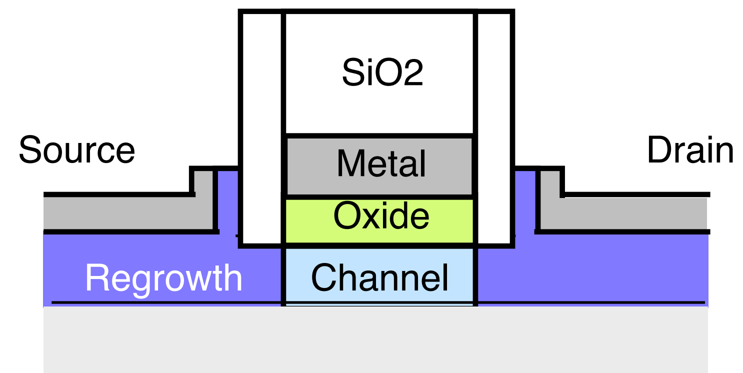


2. O2 Ash or Developer



4. Strip resist



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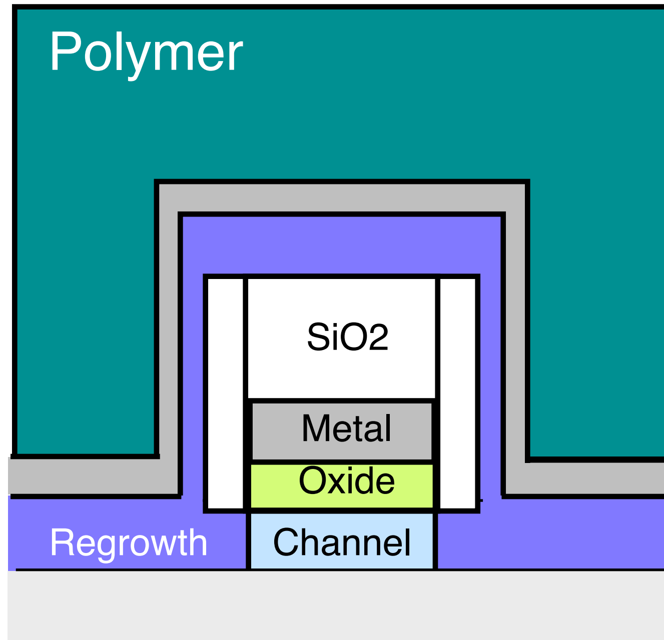

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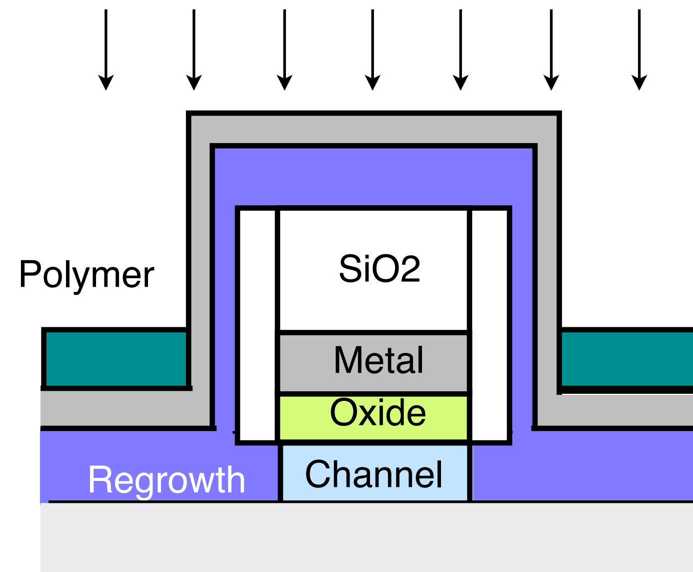
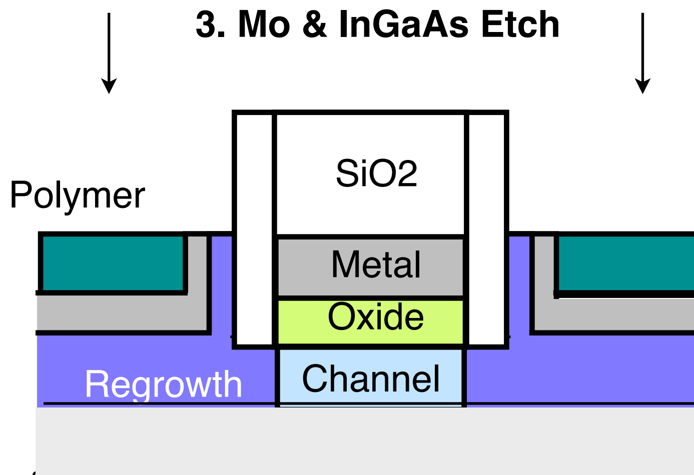


3. Mo & InGaAs Etch



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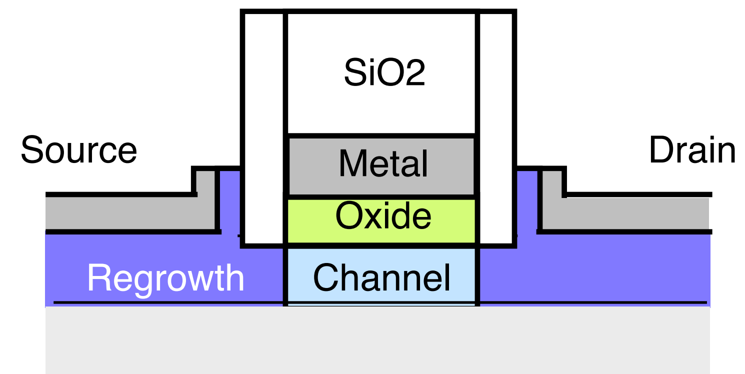

Choice of Polymers

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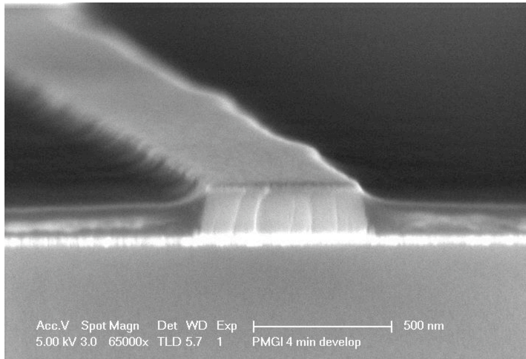
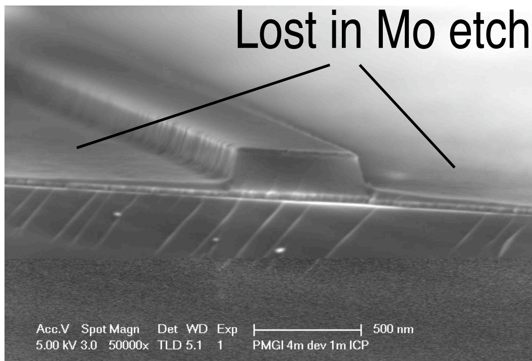
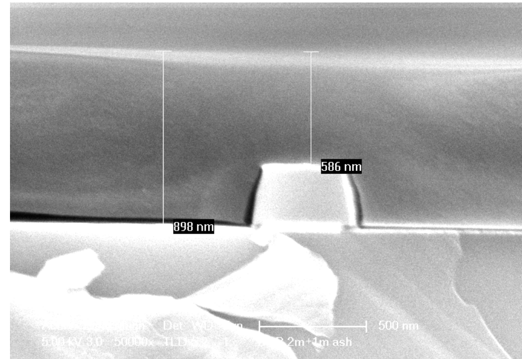
PMGI / MIF developer

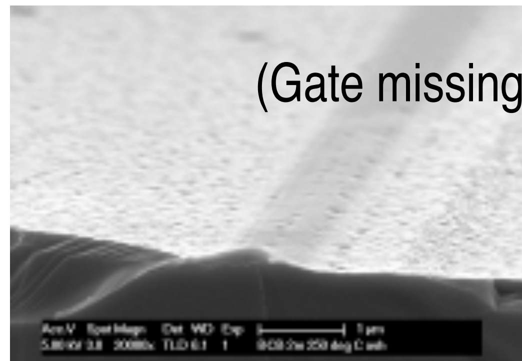




Lost in Mo etch

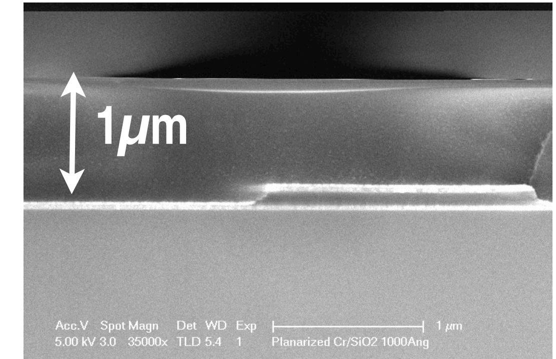
BCB / CF4+O2

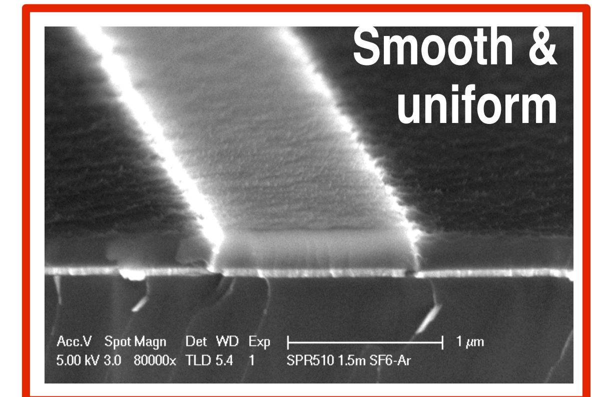




Difficult to process

SPR510 / O2 plasma





Spin: 4kRPM 30s. Bake: 90°C 1min, 110°C 1min.

- **Photoresist (SPR-510):**
  - **Easy to process**
  - **Withstands wet & dry etches**
  - **Smooth & uniform...**

Low Power Plasma Gives Smooth Etchback

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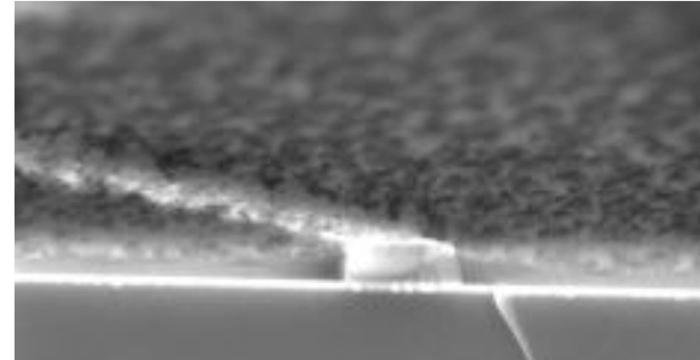
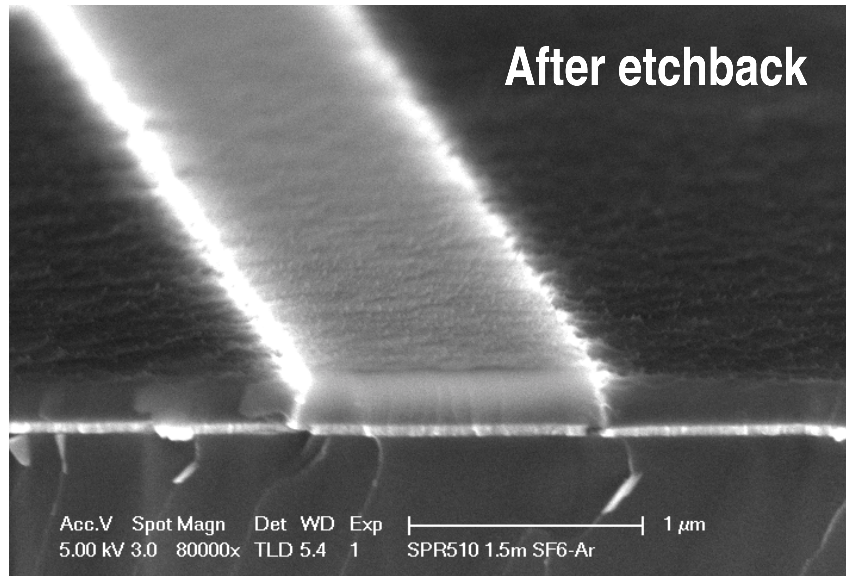
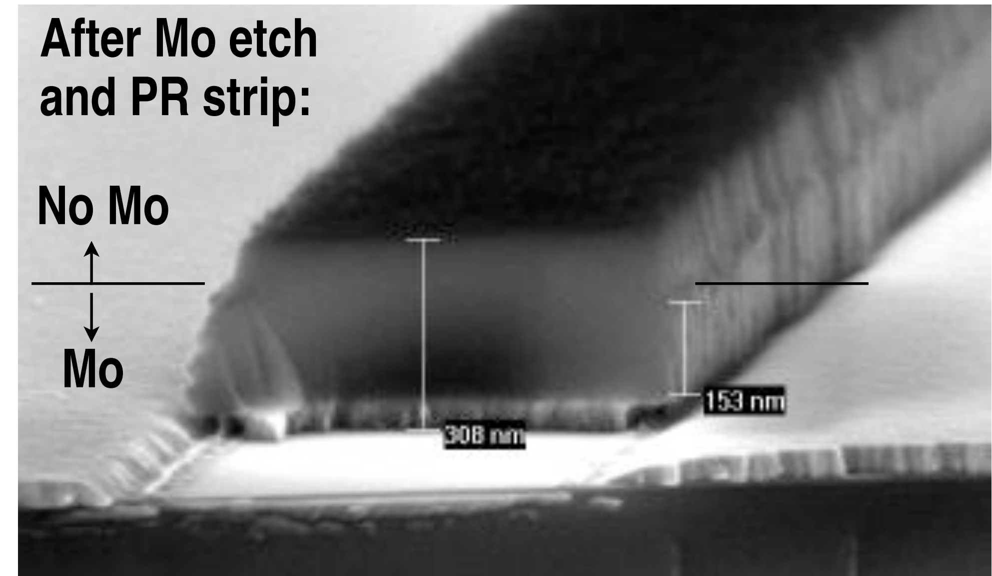
- Etchback in high energy O_2 plasma:
  - Extreme roughness (micromasking)
  - Scum



- Etchback in low energy O_2 plasma (ICP) or UV ozone:
  - Clean, smooth surfaces, no scum





Planarization: Repeatable and Easy

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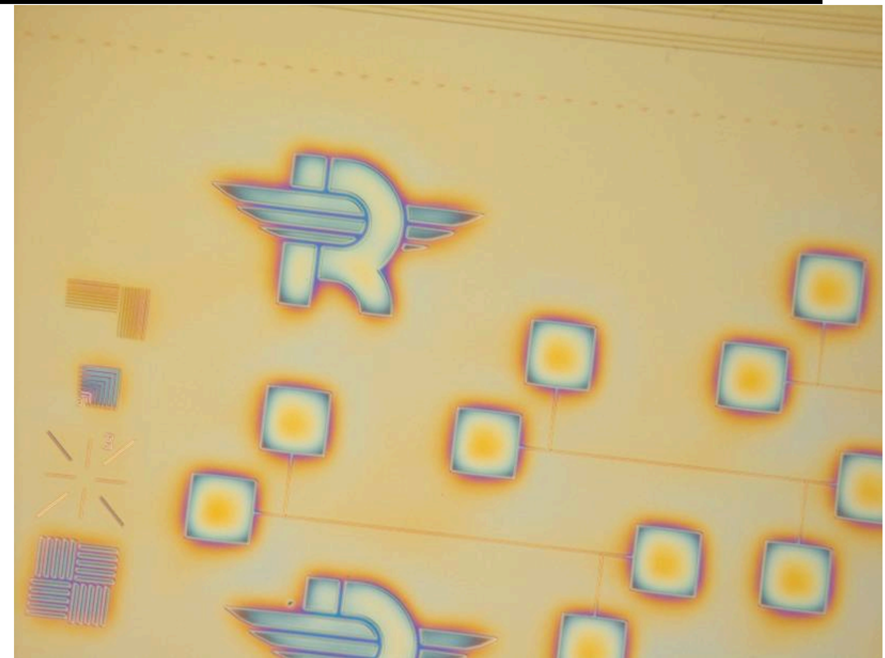
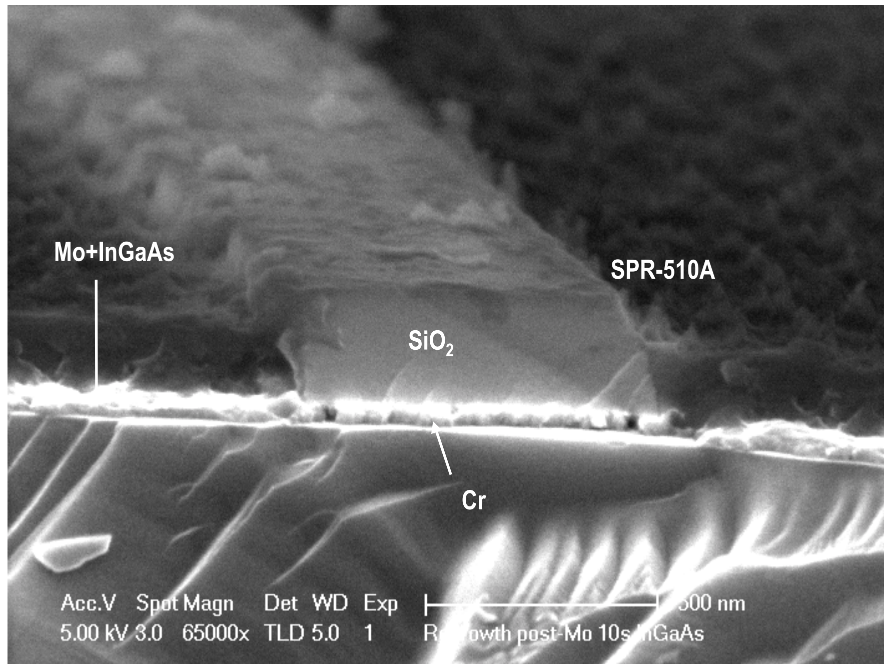
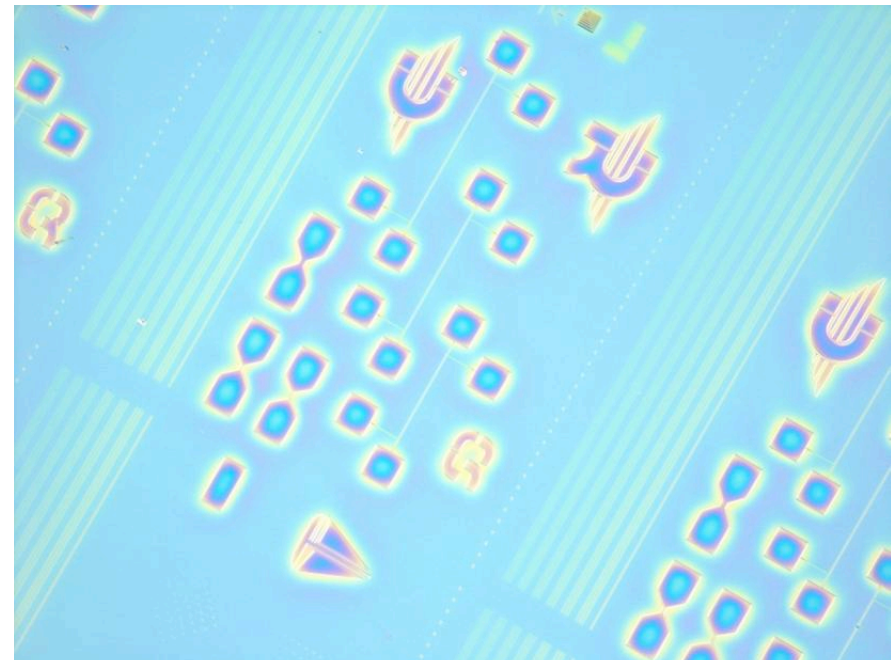
- Thickness by naked eye
  - Purple/Blue – 300nm
  - Yellow – 200nm
  - Light Blue – 100nm
  - Burnt/Black – <70nm
- High yield esp. for <1μm







MBE Regrowth: Bad at any Temperature?

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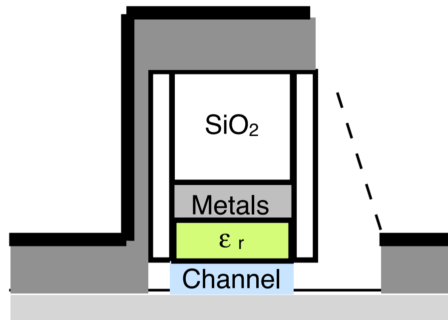
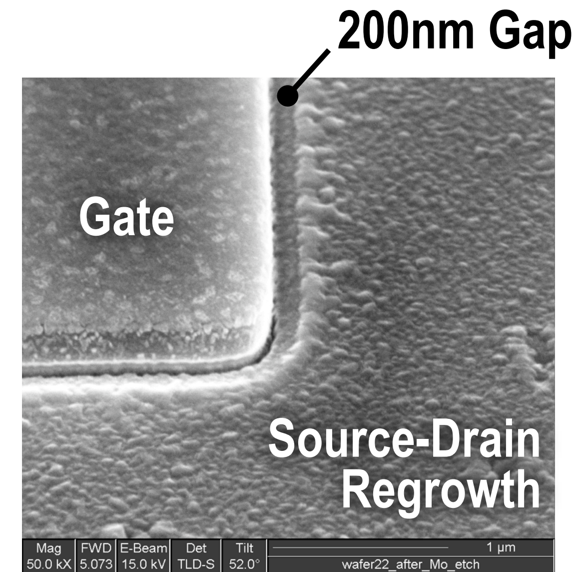
- Conditions: 0.5 μm/hr, V/III=35
- Low growth temperature (<400°C):
  - Smooth in far field
  - Gap near gate (shadowing)
  - No contact to channel!





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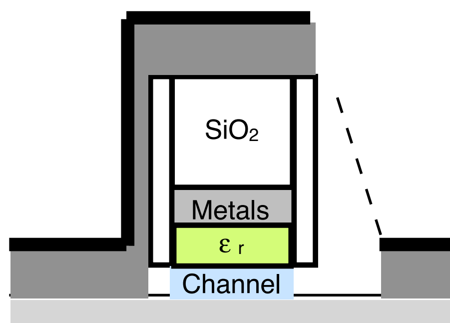
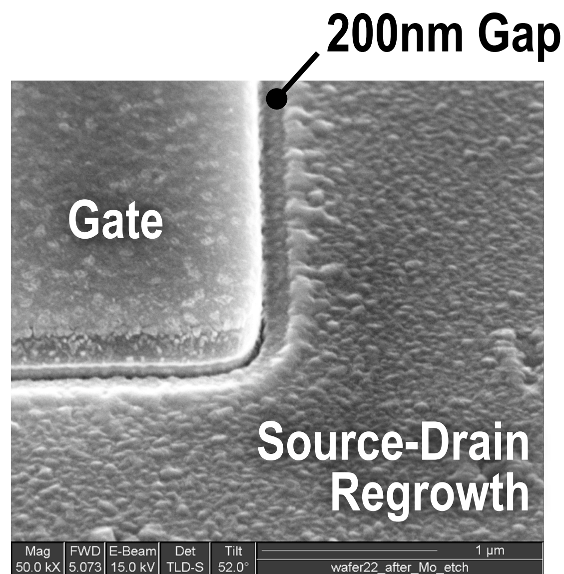
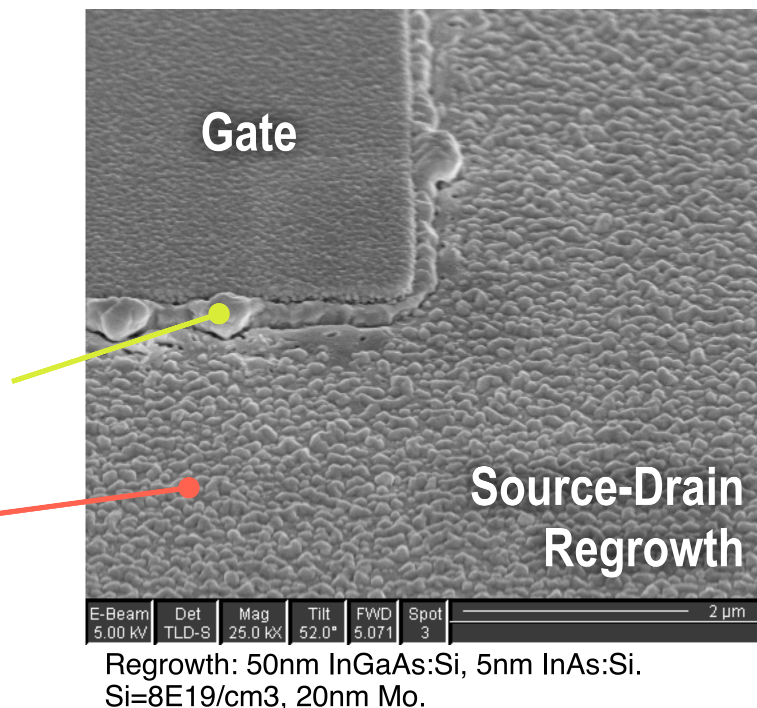




- High growth temperature (>490°C):
  - Selective/preferential epi on InGaAs
    - No gaps near gate
  - Rough far field
    - High resistance



Regrowth: 50nm InGaAs:Si, 5nm InAs:Si. Si=8E19/cm3, 20nm Mo.

Gap-free Regrowth by MEE

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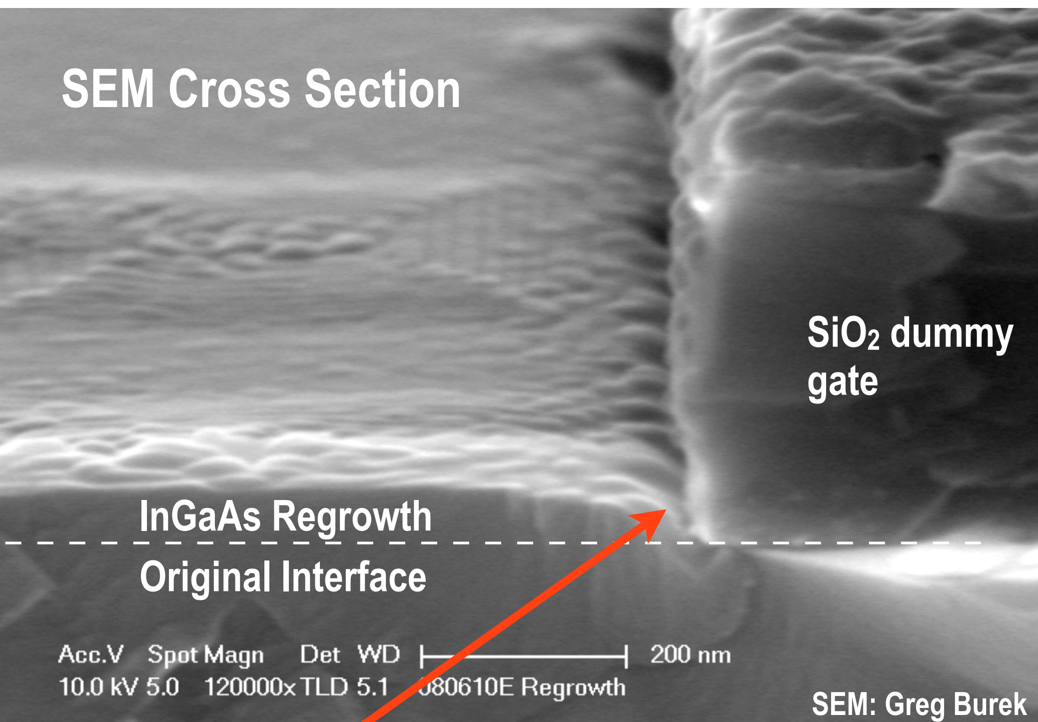
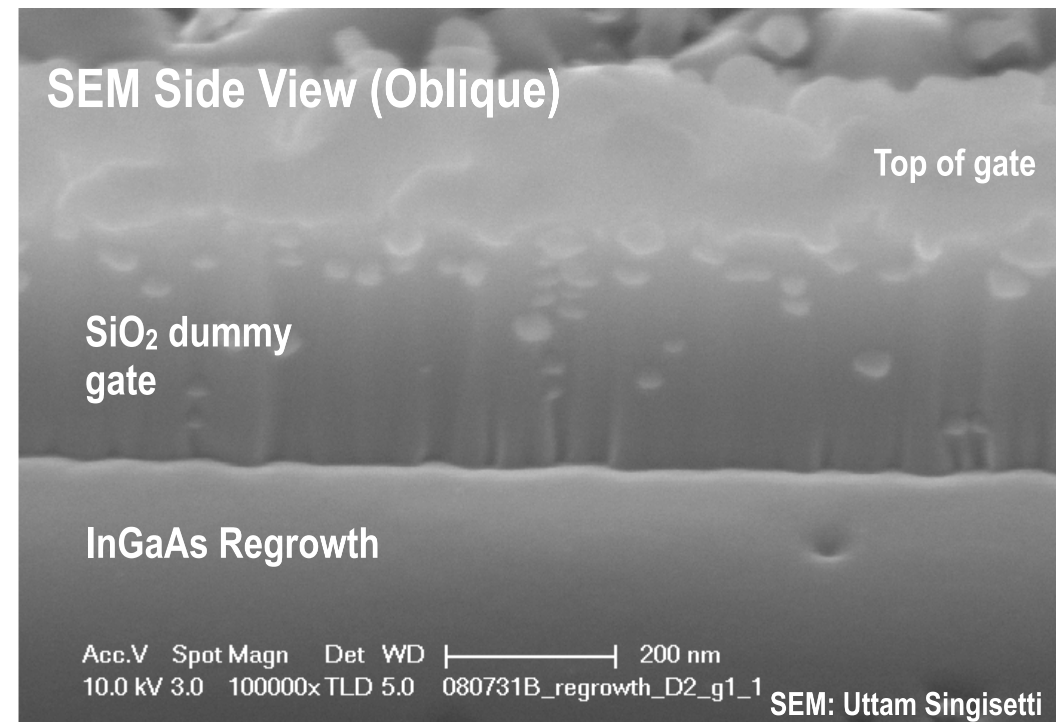
Migration-Enhanced Epitaxy (MEE) conditions:

490-550°C (pyrometer)
As flux constant ~ $1x10^{-6}$ Torr: V/III~3, not interrupted.
0.5nm InGaAs:Si pulses (3.7 sec), 10-15 sec As soak
RHEED: 4x2 ==> 1x2 ==> 4x2 with each pulse.





- No gaps
- Smooth surfaces.

- High Si activation ($4x10^{19}$ cm^{-3}).
- Quasi-selective: no growth on sidewalls

Rough Regrowth on Thin InP Etch Stop Layer

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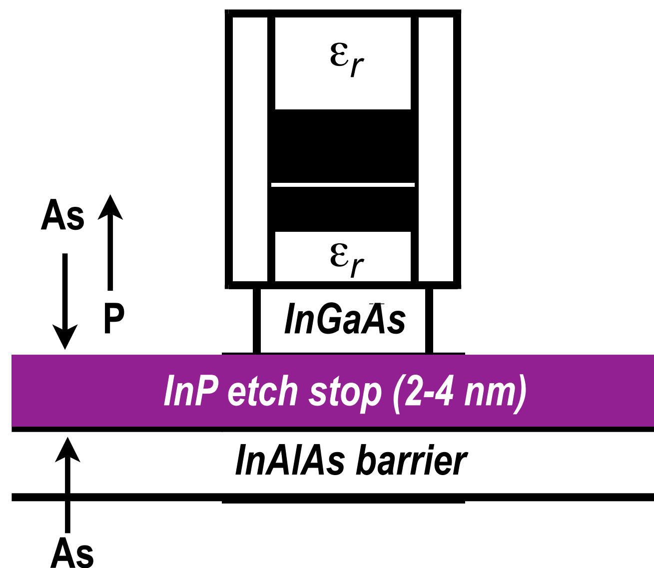
- Conversion of 2-4nm InP to InAs
- Strain relaxation



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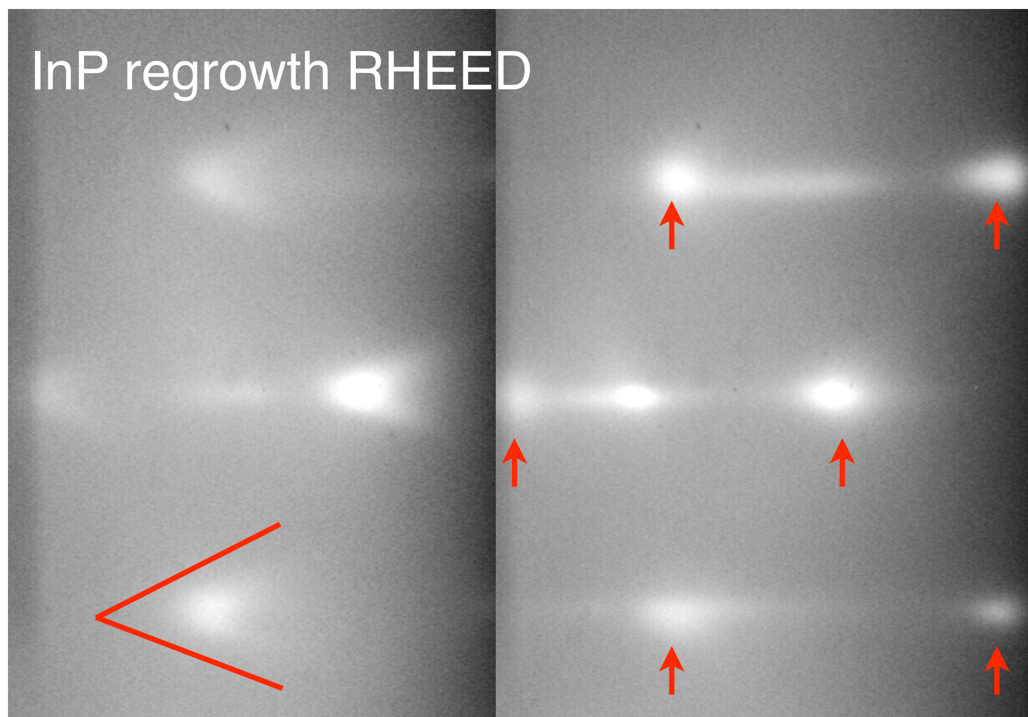

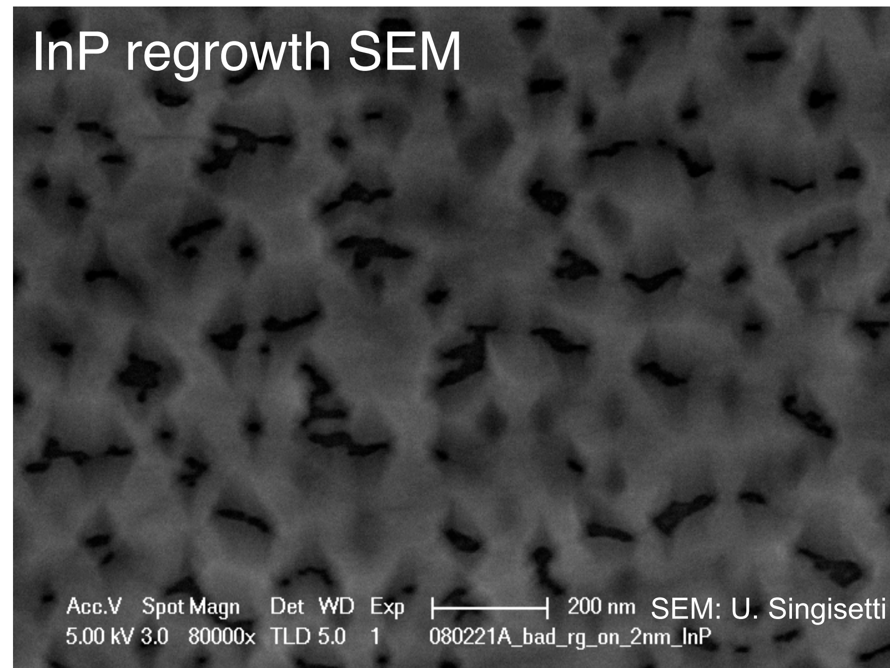

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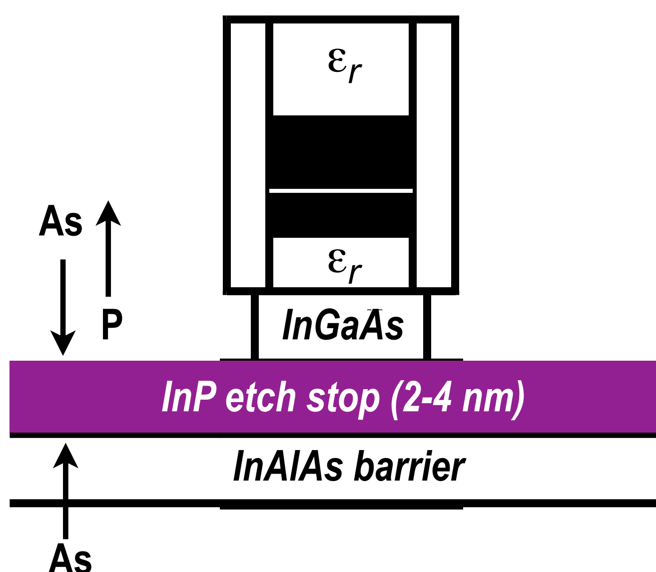

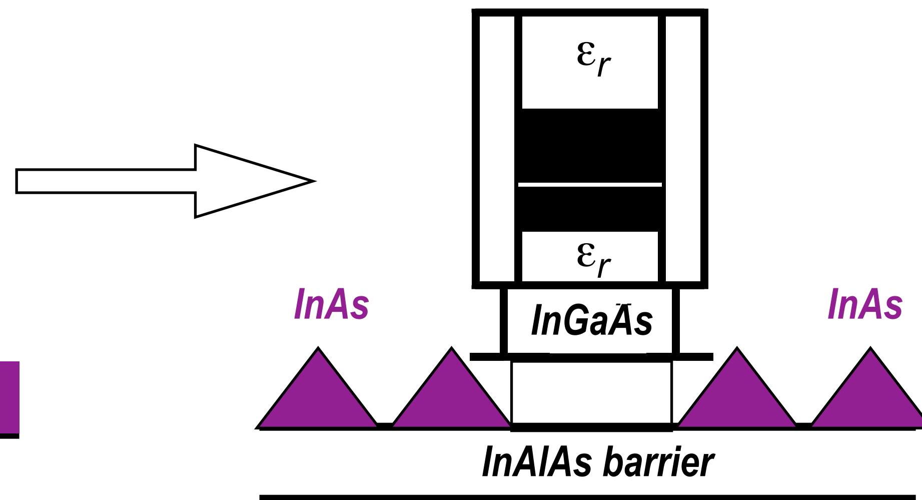

Regrowth on InGaP

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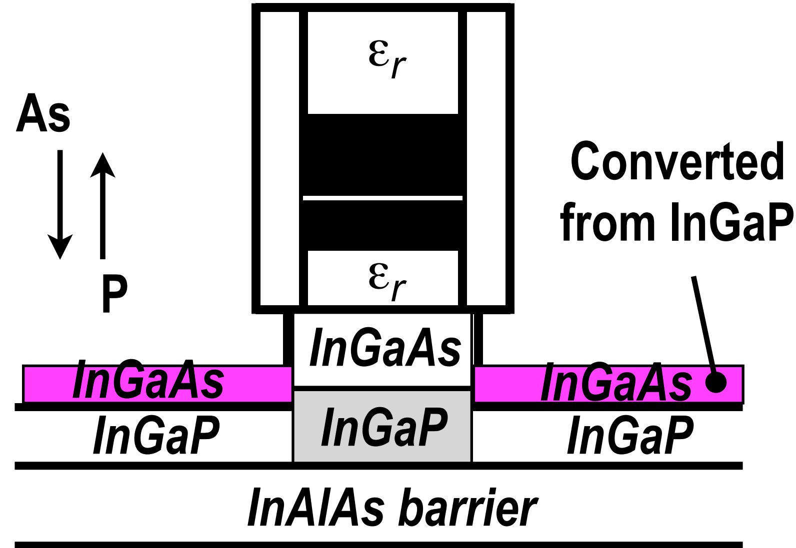
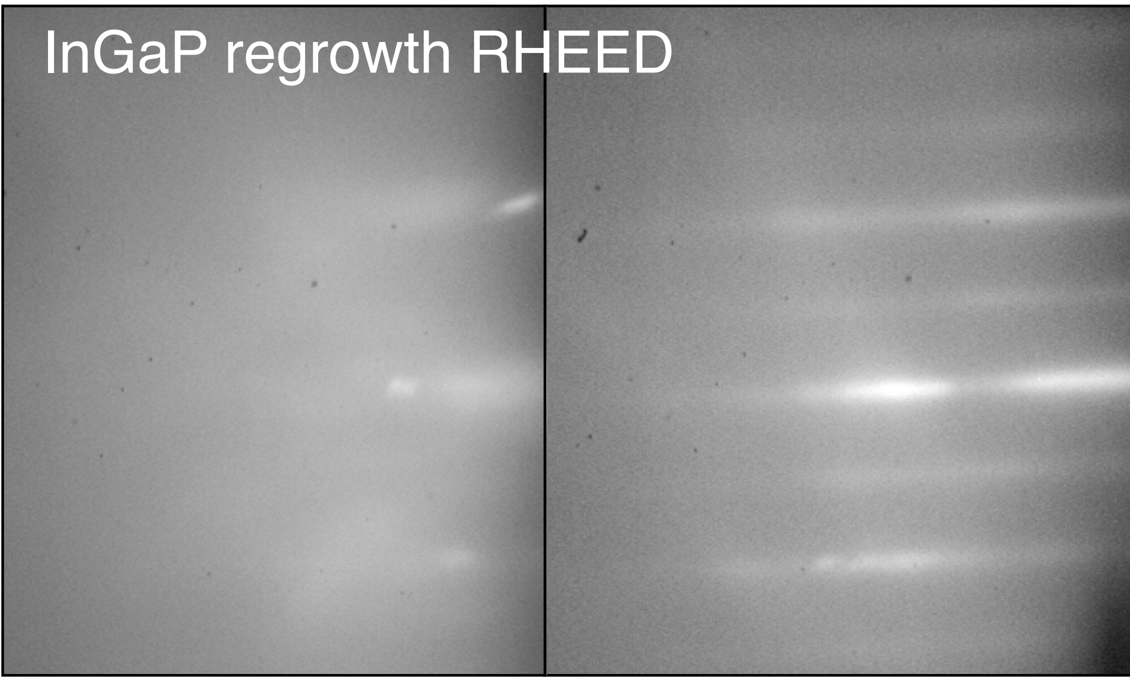
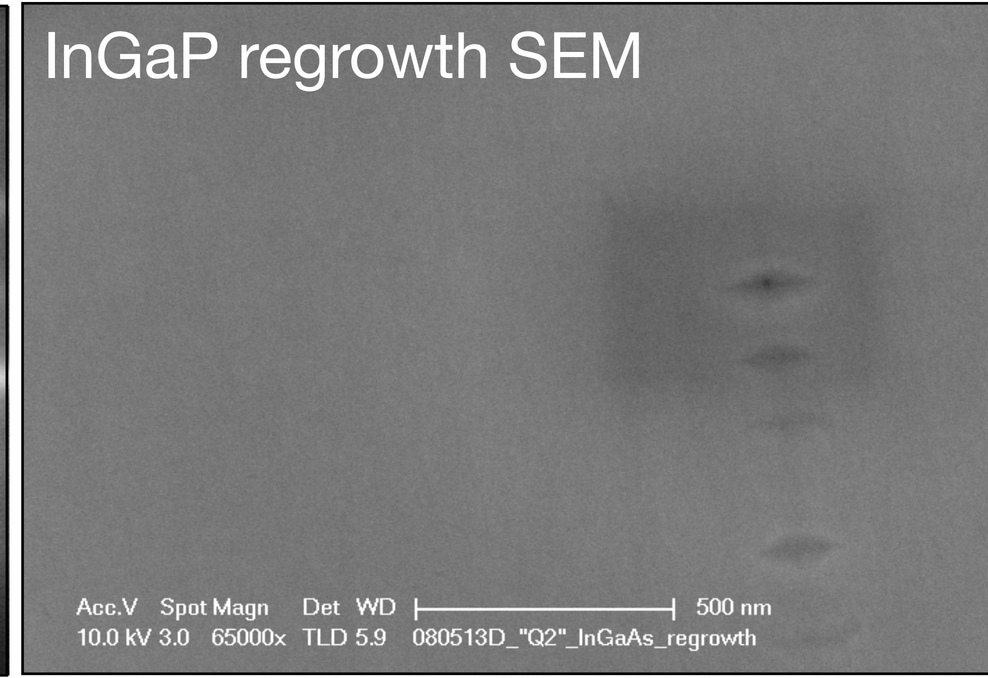
- Replace InP with InGaP
- Converts to InGaAs (good!)
- Strain compensation







Summary

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- **Surface clean before regrowth:**
  - UV ozone, 10% HCl, then H clean or thermal desorb
  - Lowest resistance regrown contacts: **Rc = 1.3 Ω-μm²** (1.3x10⁻⁸ Ω–cm²)
- **Planarization by photoresist: simple & repeatable**
  - No lithography needed
  - MBE + Planarization = **Self-Aligned Regrowth**
- **Gap-free regrowth ($n=4x10^{19}$ cm^{-3}) by MEE above 490°C**
- **InGaP etch stop prevents relaxation before regrowth**

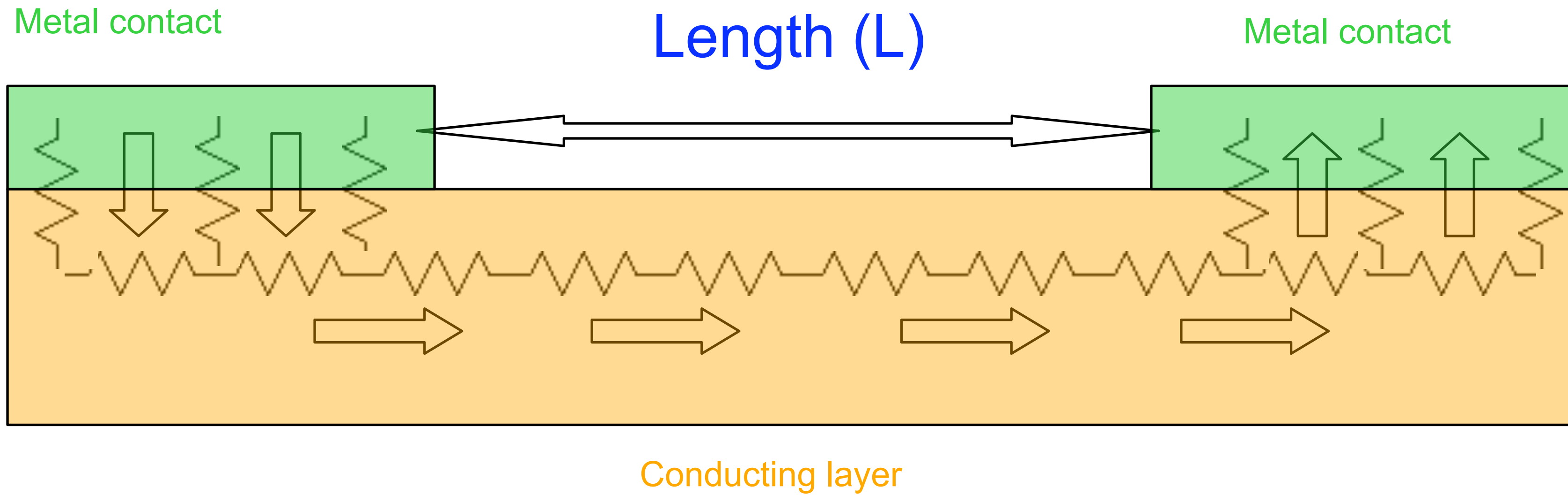
Acknowledgements

UCSB

- Chris Palmstrøm and Erdem Arkun (now at UCSB)
- IBM Yorktown: Yanning Sun, Edward Kiewra, Devendra Sadana
- SRC

Additional Slides

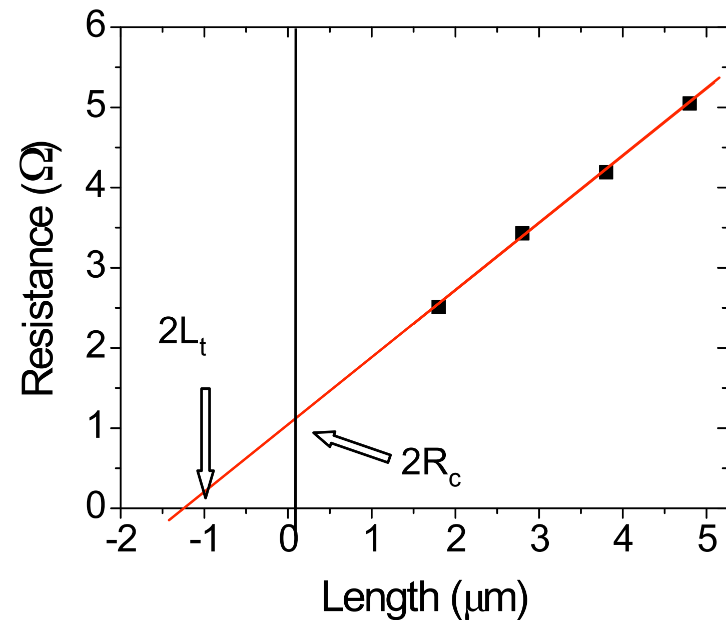
Transmission Line Method



$$R(L) = (R_{SH}/W)*(L+2L_t)$$

$$R(0) = 2R_c = 2L_t*R_{SH}/W$$

$$r_c = R_c*A_c \qquad r_c = R_{SH}*L_t^2$$



Slide courtesy Adam Crook, 2007

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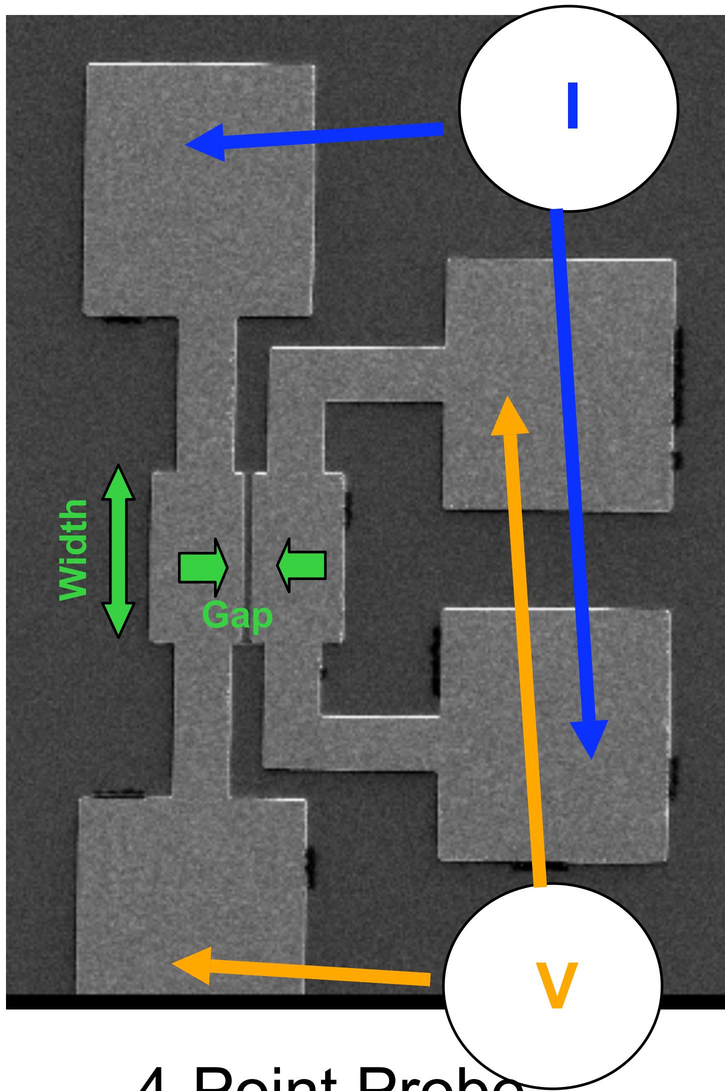
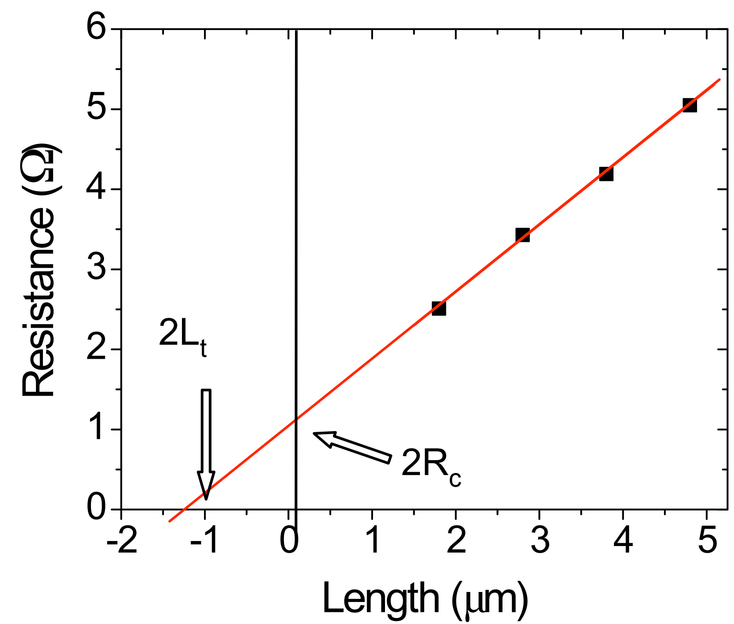


4-Point Probe
Resistance measurements



TLM Measurement

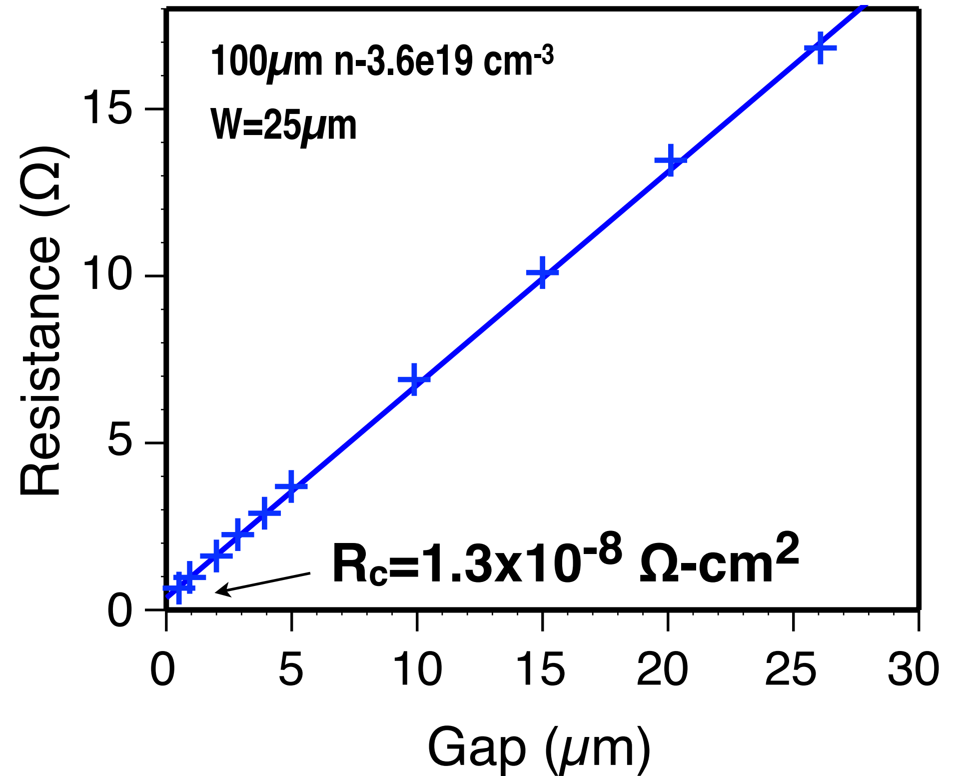


Image courtesy Adam Crook, 2007

Contact Resistance: In-situ Mo Contacts

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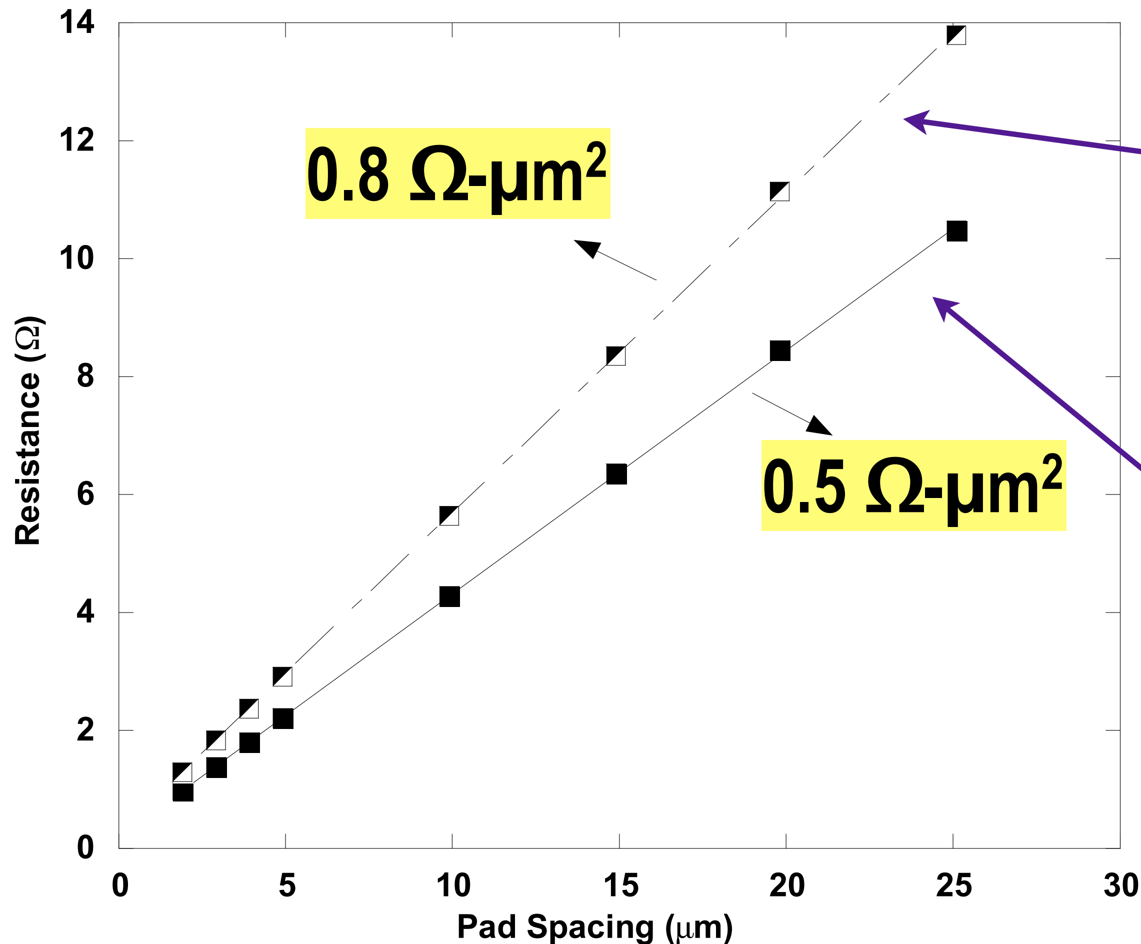
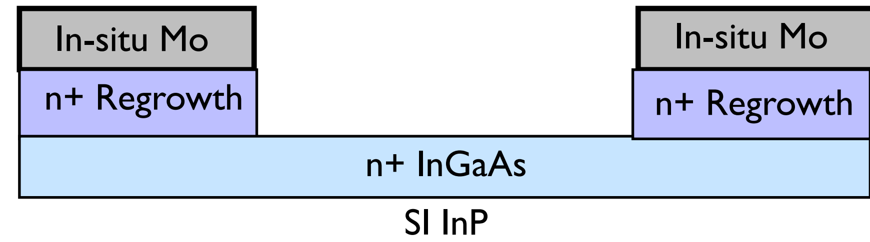
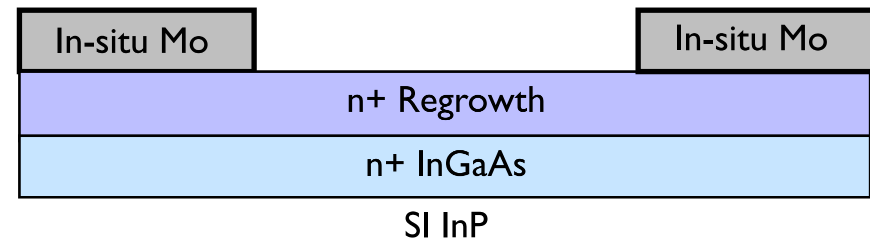


Step 2



Step 1

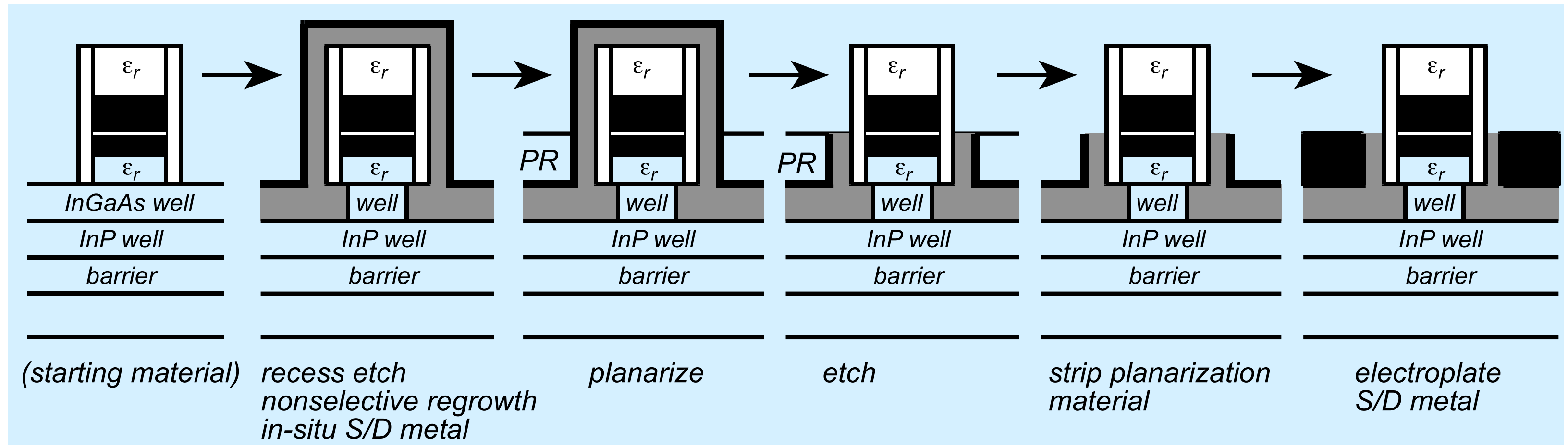


- InGaAs-InGaAs regrown interface resistance < 1 Ω -μm² on unprocessed surfaces.
- Regrown interfaces comparable with 0.5 Ω-μm² from continuous epitaxy.

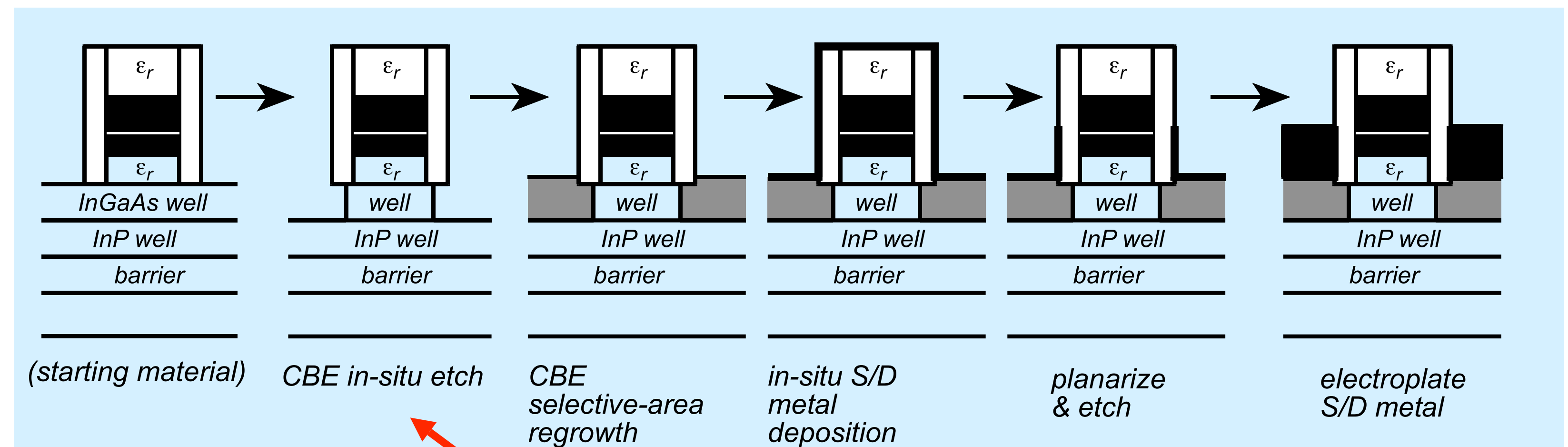
MOSFET Process Flow Detail

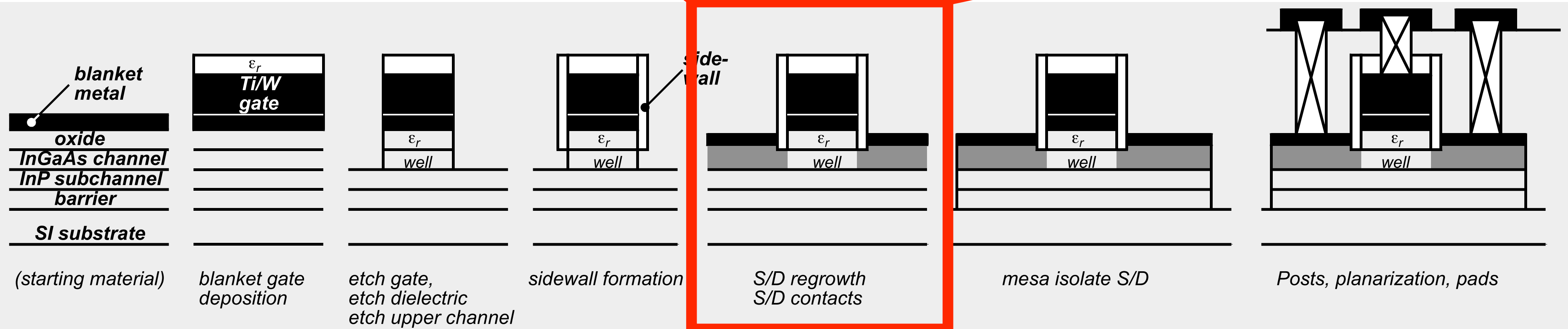
M. Rodwell, SRC Review, 2008

non-selective area S/D regrowth



selective area S/D regrowth





Process Flow: Gate Deposition

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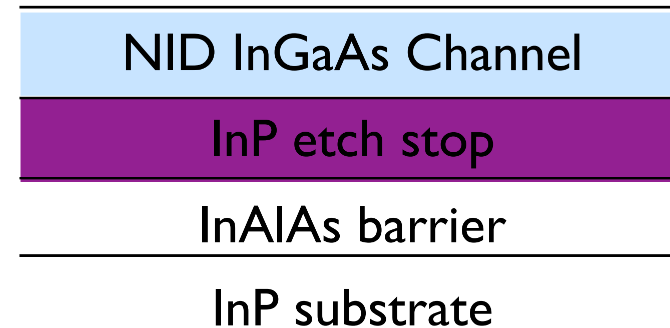
High-k first on pristine channel.

Tall gate stack.

Litho.

Selective etches to channel.



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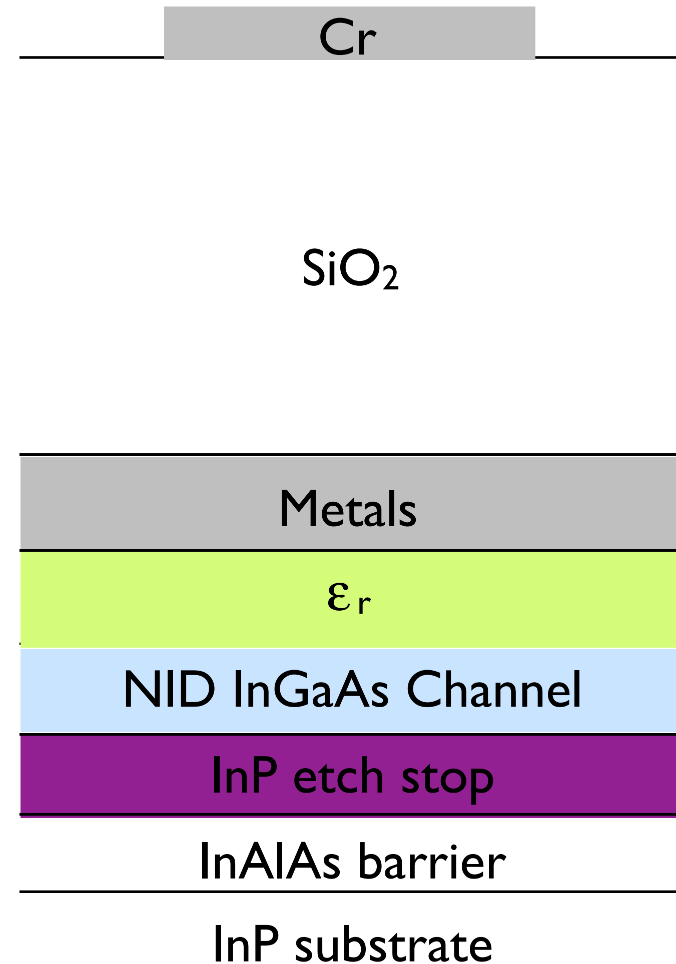

Process Flow: Gate Deposition

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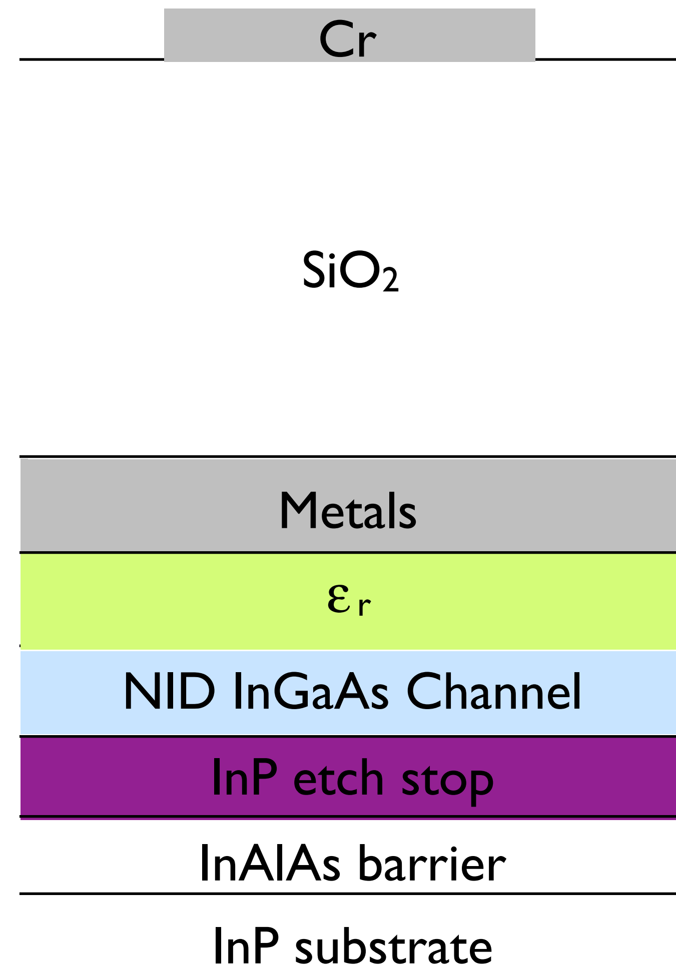
Selective etches to channel.

Critical etch process:
Stop on channel with no damage



Gate Stack: Multiple Layers & Selective Etches

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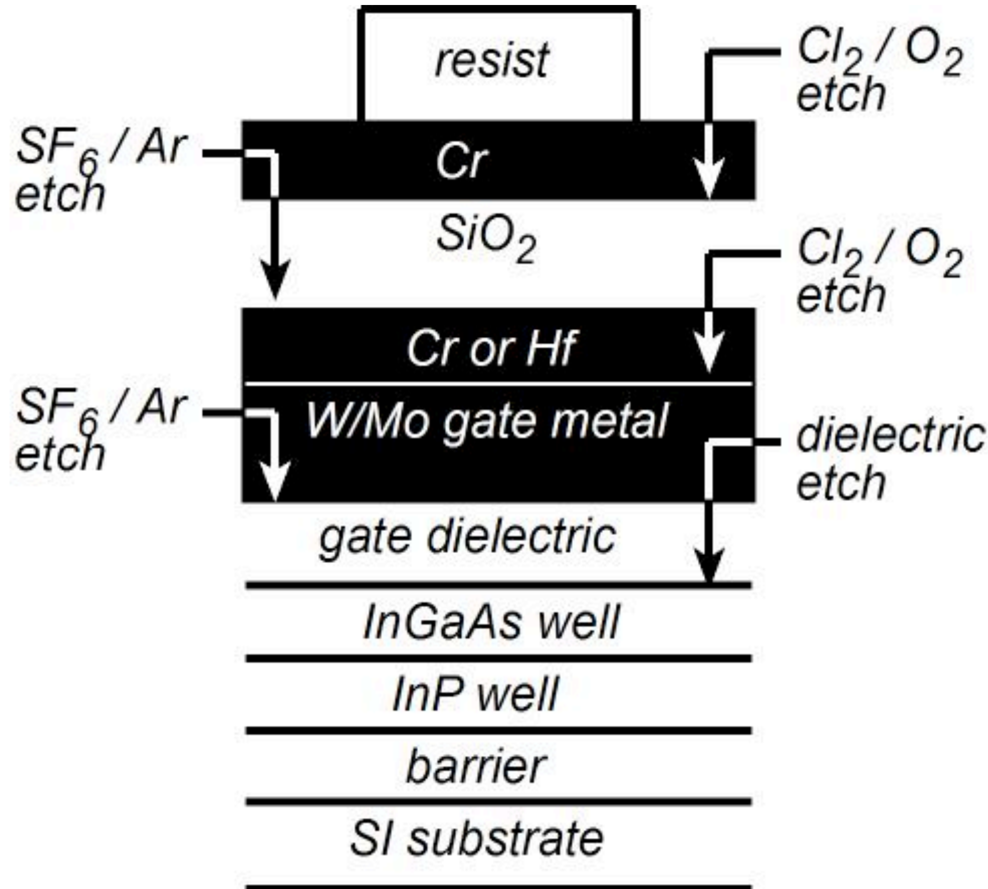
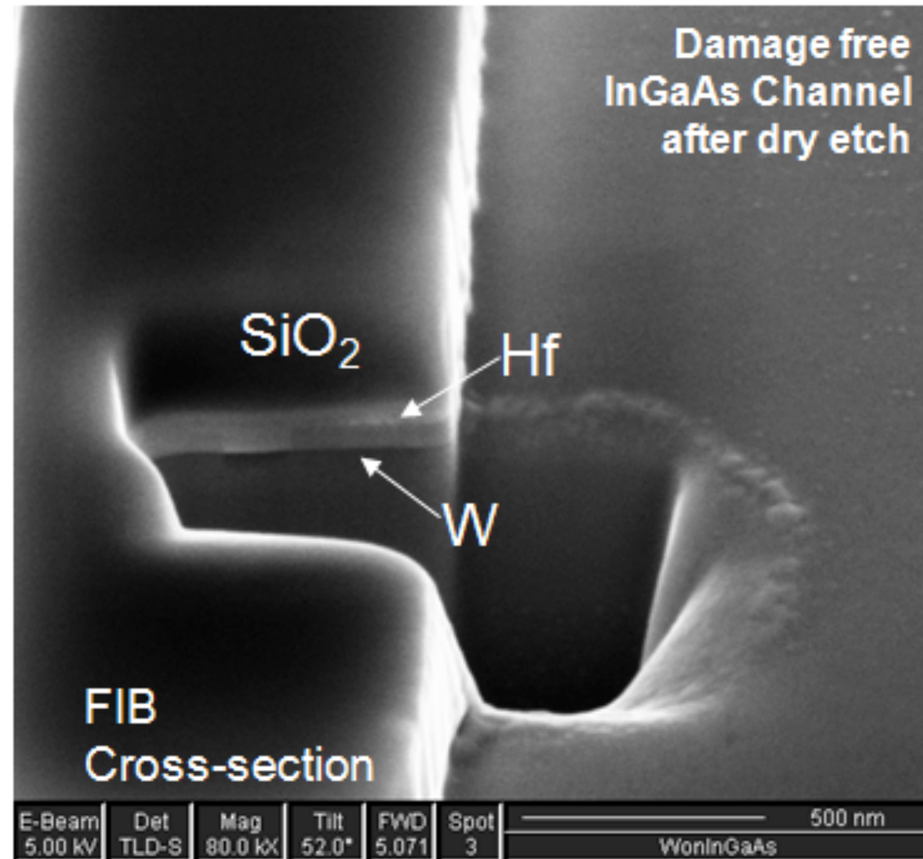
Key: stop etch before reaching dielectric, then gentle low-power etch to stop on dielectric

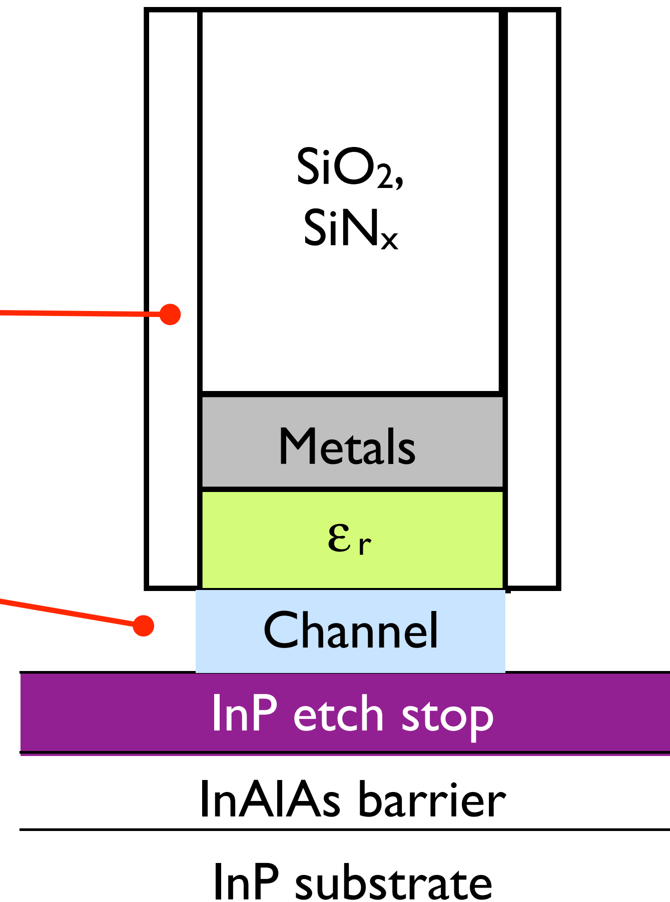




Process Flow: Sidewalls & Recess Etch

SiN_x or SiO_2 sidewalls
- Encapsulate gate metals

Controlled recess etch
- Slow facet planes
- Not needed for depletion-mode FETs

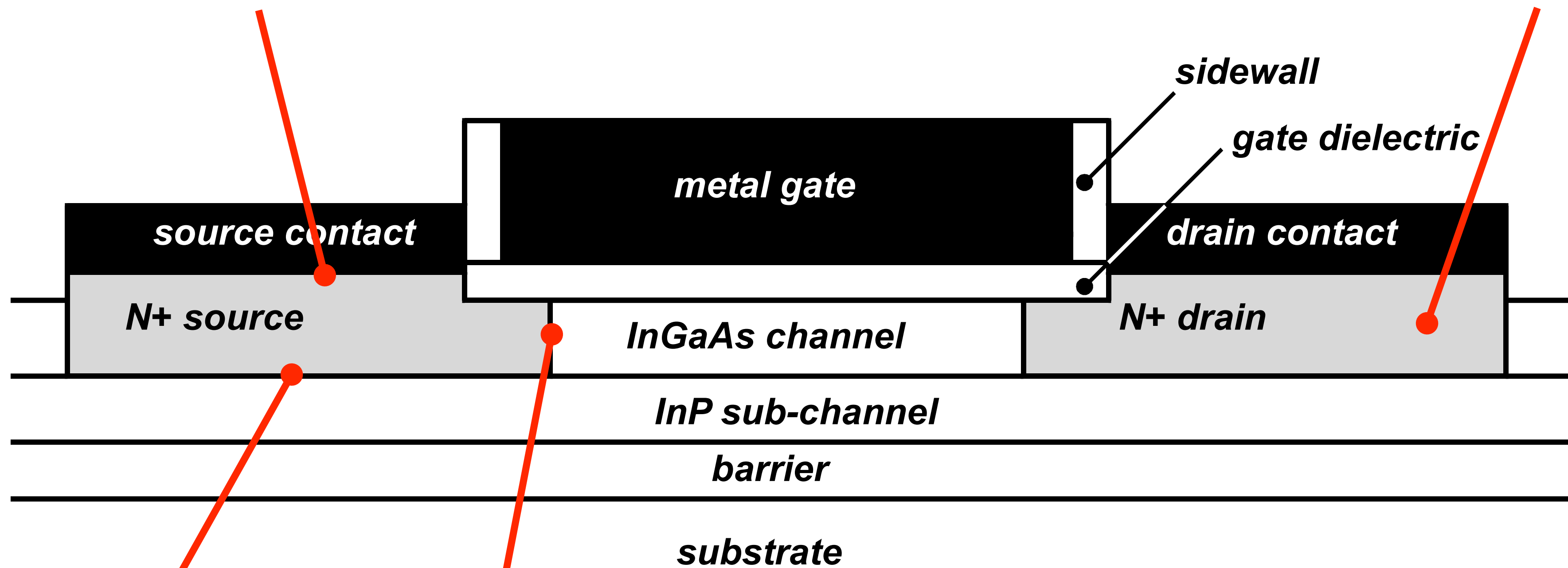


Regrowth Interface Resistances: Measured Data

When tested individually in separate experiments:

In-situ Mo Contact $\rho_c = 1\ \Omega\text{-}\mu m^2$

25 nm regrown InGaAs $R_{sh} = 70\ \Omega/sq$



InGaAs-InGaAs re-growth resistance $< 1\ \Omega\text{-}\mu m^2$.

InGaAs-InP re-growth resistance $= 6\ \Omega\text{-}\mu m^2$ (on thick InP).