Improved breakdown voltages for type I InP/InGaAs DHBTs

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***Abstract*— We have investigated the base-collector breakdown voltage of type I InGaAs/InP DHBTs, which is shown to be dominated by band-to-band tunneling in the base-collector grade. By optimizing the grade we obtain a 20% increase in the breakdown voltage compared with traditional grades.**

Keywords- InP heterojunction bipolar transistor

I. INTRODUCTION

Type I $In_{0.53}Ga_{0.47}As/InP$ double heterostructure bipolar transistors (DHBT)s have demonstrated impressive high frequency performance, with record f_{max} of 780 GHz [1], and simultaneously f_t and f_{max} of 560 GHz [2]. For further device scaling towards THz frequencies, the collector has to be thinned for shorter transit times and higher Kirk thresholds [3]. The thin collector can lead to low breakdown voltages, due to the high electric field causing band-to-band tunneling and impact ionization. We here show simulations and experimental data that the cutoff mode breakdown voltage of type I DHBTs with sub-100 nm thick collectors are set by band-to-band tunneling in the setback and grade region of the collector. Thus, by tailoring the design of the grade, it is possible to obtain a substantial increase in the breakdown voltage, without sacrificing RF-performance or drive current.

II. THEORY

Type I DHBTs utilize a setback and grade region to remove the conduction band barrier at the base collector junction, as illustrated in Fig. 1. The high field at the base-collector junction, combined with the small bandgap of the setback can result in a large band-to-band tunneling current, dominating the breakdown properties. We have developed a 2-band tunneling model taking the position dependent bandgap and effective masses of the setback and grade region into account. The imaginary k(x) inside the bandgap is written as

$$k(x) = \frac{1}{\hbar}\sqrt{\frac{m^*(x)}{2E_g(x)}\left[E_g^2(x) - 4(E - V(x))^2\right]}, \qquad (1)$$

where $V(x)=(E_c(x)+E_v(x))/2$, $E_g(x)$ the bandgap at position x,

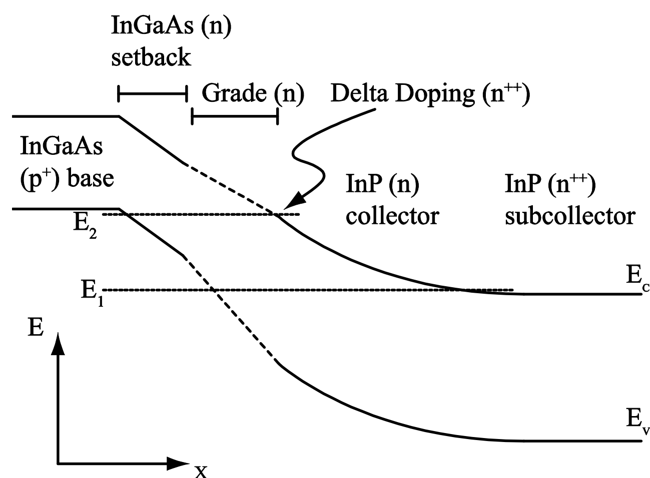

Figure 1. Schematic illustration of the collector structure of a InP DHBT. The grade region reomve the conduction band offset between InP and InGaAs. The delta doping next to the grade is used to offset the quasi-electric field induced by the grade.

$m^*(x)$ the mean value of the electron and light hole effective mass and E the energy in respect to the valence band edge. The band-to-band tunneling transmission is then obtained using the WKB approximation as

$$T_t = \exp\left(-2\int_{x_1}^{x_2}|k(x)|dx\right), \qquad (2)$$

where x_1 and x_2 are the classical turning points. The current is obtained by integrating over energy

$$J = J_0\int_{E_1}^{E_2} T_t(E)dE \qquad (3)$$

Where E_1 and E_2 are the energies inbetween which tunneling is allowed, and J_0 is given by

$$J_0 = \sqrt{\frac{2m^*(0)}{qE_g(0)}}\left(\frac{q}{\pi}\right)^3\frac{1}{\hbar^{2/3}}\varepsilon_p, \qquad (4)$$

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where ε_p is the peak electric field at the base-collector junction. We have here, for simplicity, used a constant field, effective mass and bandgap for integration over the transverse energy. The electrostatics of the base-collector junction is treated as a $p^{++}/n/n^{++}$ junction, with an assumed zero depletion width of the base and subcollector region.

We have also modeled the impact ionization rate, allowing for position dependent electron and hold impact coefficients $\alpha(x,\varepsilon)$, $\beta(x,\varepsilon)$ and dead-space distances $l(x)_{ds,n}$, $l(x)_{ds,p}$. Following [4], we write the generation rate equation as

$$\frac{\partial J_n}{\partial x} = -\frac{\partial J_p}{\partial x} = \alpha(x) J_n\left(x - l_{ds,n}(x)\right) + \beta(x) J_p\left(x + l_{ds,p}(x)\right). \quad (5)$$

The impact ionization multiplication factor M, is then calculated as $M=J_n(0)/J_n(L)$.

Our simulations show that the base-collector current is essentially set by tunneling in the high-field region of the setback region, as well as in the upper part of the grade. Tunneling in the InP-part of the collector is negligible. The breakdown voltage due to impact ionization ($M=\infty$) was further calculated to be substantially larger that the tunneling induced breakdown currents. Guided by the simulations, we designed new grading schemes to minimize with thin setbacks and grades.

III. Experiment

A. Fabrication

Three DHBTs with different grade designs were grown on 4" S.I. InP-substrates by the commercial vendor IQE. Triple mesa DHBTs were subsequently fabricated using a hybrid dry/wet etch process [2], forming emitter-base junction widths down to 180 nm. First, a $Ti/Ti_{0.1}W_{0.9}$ 5nm/500nm film is blanket sputtered onto the substrate, followed by a 100nm SiO_2 layer deposited by PECVD, and a 35 nm E-beam evaporated Cr film. The Cr-film will act as a mask for subsequent dry etching steps, and the SiO2 is used to protect the TiW and allow for easy removal of the Cr mask after the dry etching steps. The Cr is patterned using I-line lithography and a Cl_2/Ar ICP dry etch, which allows for formation of 150 nm wide Cr lines. The SiO2 and TiW is then etched in a SF_6/Ar ICP plasma. The TiW is slightly tapered during the etch, increasing the linewidth with 50-100 nm. A 25 nm SiN_x sidewall is formed using PECVD and a CF_4/O_2 ICP etch. The sidewall is used for improved adhesion and protection of the Ti interlayer. Using a low power Cl_2/N_2 ICP etch performed at a chuck temperature of 200°C, the Ti and n^{++} InGaAs emitter is etched away, stopping inside the InP part of the emitter. The SiO_2 and Cr layers are stripped away in a buffered HF etch, and a wet etch step removes the rest of the InP down to the InGaAs p^{++} base. In this way, we minimize wet etch steps that could lead to large emitter undercuts, as well as any dry etch damage to the base. The devices are finalized using a standard triple mesa wet etch process, with BCB for planarization/passivation. Fig. 2 shows a cross section image of a 180 nm junction width device.

The designs all used a 22nm thick p^{++} $In_{0.53}Ga_{0.47}As$ base, and a total collector thickness of 70 nm. Three different base-collector grade designs were implemented; the designs are

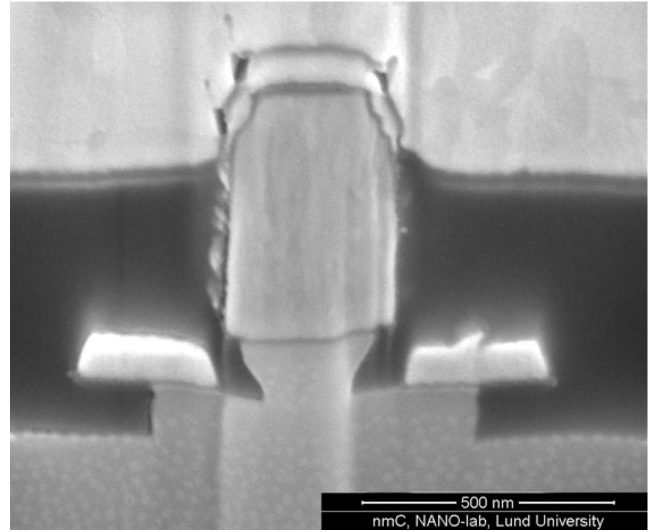

Figure 2. Cross-section FIB-SEM image of a finished DHBT. The base emitter junction width is 180 nm.

TABLE I. GRADE DESIGNS

DHBT 42			
Thickness (nm)	***Material***	***Doping (cm^{-3})***	***Description***
10	$In_{0.53}Ga_{0.47}As$	2×10^{17} : Si	Setback
18	InGaAs/InAlAs	2×10^{17} : Si	Superlattice grade
3	InP	3.4×10^{18} : Si	Delta Doping

DHBT 41			
Thickness (nm)	***Material***	***Doping (cm^{-3})***	***Description***
5	$In_{0.53}Ga_{0.47}As$	2×10^{17} : Si	Setback
10.8	InGaAs/InAlAs	2×10^{17} : Si	Sub-monolayer grade
3	InP	6.2×10^{18} : Si	Delta doping

DHBT 40			
Thickness (nm)	***Material***	***Doping (cm^{-3})***	***Description***
1	$In_{0.53}Ga_{0.47}As$	3×10^{17} : Si	Setback
6	InGaAs→GaAs	3×10^{17} : Si	Strained grade
4	InP	6.2×10^{18} : Si	Delta doping

summarized in table I. The InP drift collectors was doped to $N_d=2\times10^{17}$ cm^{-3} for DHBT 42 and 41, and $N_d=3\times10^{17}$ cm^{-3} for DHBT 40, chosen so that the collector should just be fully depleted at V_{cb}=0V. This doping level is 2-10 times higher than for earlier HBTs with similar collector thickness [5,6].

DHBT 42 utilizes a traditional UCSB chirped superlattice grade, using a 12-layer superlattice with a period of 15Å, and linearly changing the InAlAs thickness from 1.5Å at the base side to 7.8 Å at the collector side. The sub-monolayer grade of

TABLE II. BREAKDOWN VOLTAGES, β, MAXIMUM F_T, F_{MAX} AND J_{KIRK}

	BV_{ceo} (V)	BV_{cbo} (V)	β	f_t (GHz)	f_{max} (GHx)	J_{kirk} ($mA/\mu m^2$)
DHBT40	3.3	3.3	35	510	410	15
DHBT41	3.4	3.54	24	600	430	22
DHBT42	2.8	2.96	25	500	430	20

DHBT 41 has 21 layers, where the thickness of the InAlAs layer is set to 1.5Å, and the InGaAs is varied linearly from 16.5 down to 1.5 Å. The 6 nm-thick-grade of DHBT 40 is strained, graded from $In_{0.53}Ga_{0.47}As$ at the base-side to GaAs at the collector side.

B. Breakdown Voltages

Figure 2. shows measured I_{cbo} and I_{ceo} for the three different grades. The close to unity ratio between BV_{cbo} and BV_{ceo} is usual for transistors which are limited by tunneling breakdown. The breakdown voltages, defined at J_c=100μA/μm^2 (normalized to the *emitter* area) are shown in table II. By thinning down the graded region, we obtain a 20% increase in the breakdown voltages compared with the traditional design. Note that due to the high collector doping used here (~ 2×10^{17}cm^{-3}), a direct comparison with earlier reported breakdown voltages of DHBTs with similar collector thicknesses is not possible, which has used lower collector dopings of N_d~3-9×10^{16} cm^{-3}.

Figure 3 shows measured and simulated BV_{cbo} (defined at J_c=10μA/μm^2, normalized to the collector area), for transistor with collector areas ranging from A_{jc}=2-15μm^2. The superlattice regions for DHBT 41 and 42 have here been modeled as a linearly graded region, grading the bandgap and effective massed from $In_{0.53}Ga_{0.47}As$ to InP. The strained grade of DHBT 40 was modeled as a linearly varying grade between $In_{0.53}Ga_{0.47}As$ and GaAs (strained to InGaAs), using band parameters from k·p calculations [7]. While experimentally not exactly known, GaAs strained to $In_{0.53}Ga_{0.47}As$ should have a very small conduction band offset in the order of 50 meV, at the expense of a small bandgap of 0.9 eV. Good agreement between simulated and measured data is obtained, with deviations mainly originating from unknowns in the exact material parameters.

The temperature dependence of BV_{cbo} was further characterized for DHBT41 in the temperature range -55°C < T < 125°C. The transistor showed increasing breakdown voltage with decreasing temperature, with ΔBV_{cbo}=-2.2×$10^{-3}\Delta T$, as shown in Fig. 4. This negative temperature coefficient originates from the decrease in bandgap with increasing temperature, which increases the tunneling current. Calculations with temperature dependent bandgap give excellent agreement with the measured data. Note that breakdown related to impact ionization will have a positive temperature coefficient, due to the decreasing ionization rate with increasing temperature.

Our calculations of the impact ionization related BV_{cbo} gives a breakdown voltage of $BV_{cbo,impact}$ ~ 5.5V for all three grades, indicating that the breakdown is not set by impact ionization. The agreement with modeling and the temperature dependence show strong

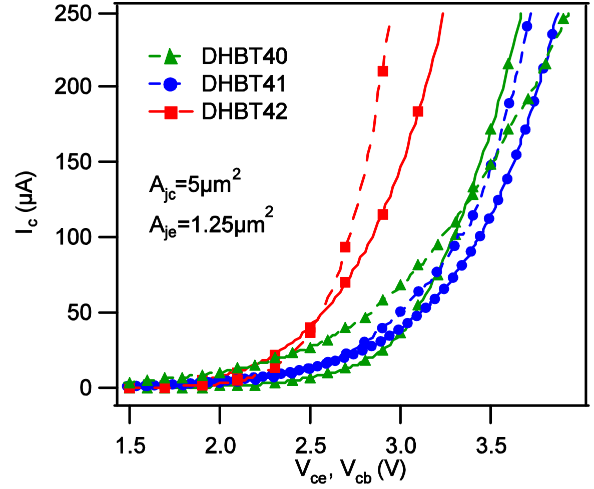

Figure 3. I_{cbo} (full) and I_{ceo} (dashed) for DHBT40-42

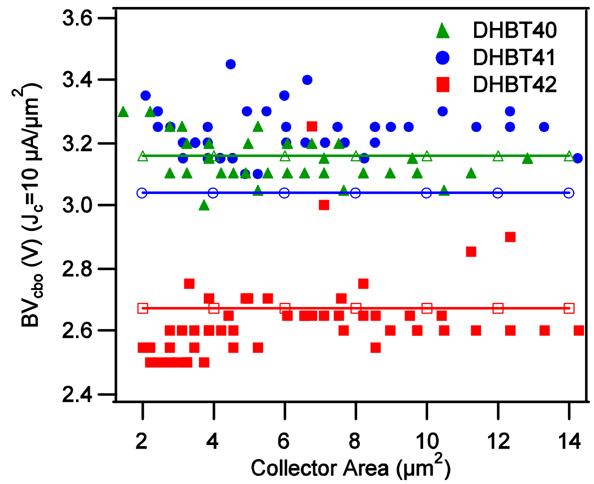

Figure 4. BV_{cbo} vs. collector area. Filled symbols are experimental values, empty symbols are the corresponding calculated values.

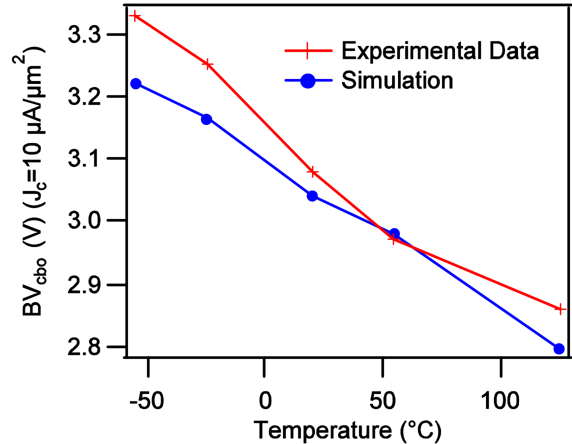

Figure 5. Experimental and simulated data for temperature dependent breakdown for DHBT 41.

TABLE III. OVERVIEW OF UCSB COLLECTOR DESIGNS

T_c (nm)	N_d (cm^{-3})	N_{delta} (cm^{-2})	$T_{setback}$ (nm)	T_{grade} (nm)	BV_{cbo} calc. (V)	BV_{cbo} exp. (V)	J_{kirk} ($mA/\mu m^2$)	Ref.
60	7.5×10^{16}	9.0×10^{11}	7.5	18	3.0	2.7	16	[5]
70	2.0×10^{17}	1.9×10^{12}	5	11	3.0	3.1	22	DHBT 41
75	3.0×10^{16}	9.0×10^{11}	10	24	3.7	3.6	11	[6]
100	9.0×10^{16}	9.0×10^{11}	15	24	4.1	3.9	11	[8]
120	3.0×10^{16}	9.0×10^{11}	15	24	5.4	5.0	9	[9]
150	3.5×10^{16}	1.1×10^{12}	15	24	6.5	6.2	12	[1]

evidence that the breakdown mechanism of these type I DHBTs originate from tunneling instead of impact ionization.

C. Transistor Measurments

The transistors were characterized by measuring the DC-67 GHz performance, with representative values of DC-current gain (β), f_t, f_{max} and J_{kirk} tabulated in table II, for transistors with emitter widths of ~ 180-220 nm. All designs show good f_t, with f_{max} limited by a fairly high base ohmic contact resistance (ρ_b ~ 10-30$\Omega/\mu m^2$, from TLM measurements). DHBT 42 and 41 show similar J_{kirk}, indicating that the thinner setback and grade of DHBT41 does not have a negative impact on the electron transport at the base-collector junction compared with the traditional, thicker grade. DHBT 41 further on showed the first operation of any transistor with simultaneously f_t and f_{max} above 500 GHz. The strained grade of DHBT 40 displays a lower Kirk threshold, possibly related to the 1 nm thin setback, or relaxation related defects induced from the strained growth. As shown in table III, the Kirk threshold of all three grades compare favorably with earlier UCSB DHBTs using longer setback and grades, as well as InGaAs SHBTs [10].

IV. COMPARISON WITH EARLIER UCSB DHBT DATA

Table III shows experimental data and breakdown simulations for different UCSB DHBT designs, with collector thicknesses ranging from 60nm up to 150 nm. Here the breakdown voltage is defined at J_c=10$\mu A/\mu m^2$ (*normalized to collector area*) Good agreement is obtained between simulated and experimental breakdowns. Except for DHBT 41, the designs utilize a traditional grade, with a 15Å period chirped superlattice. The higher doping and narrow 180 nm emitter-base junction used in the current devices allows for a substantially higher Kirk threshold. The reduced 5 nm thick setback thickness of DHBT41 increases the breakdown voltage any does not seem to degrade the Kirk threshold current. Further reduction in setback and grade layer could lead to further increase in breakdown voltage.

V. CONCLUSION

We have shown that the breakdown voltage of type I DHBTs are set by band-to-band tunneling in the setback and grade region of the base collector grade. By thinning down the setback and grade, improvement in breakdown characteristics can be obtained, while still allowing for large current densities. Excellent By using a strained GaAs/InGaAs grade, we have achieved large current densities with a very thin 1 nm setback and 6 nm grade.

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