Technology Development & Design for 22 nm InGaAs/InP-channel MOSFETs

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***Abstract*—Because of the low electron effective mass and the high resulting carrier velocities, we are developing InGaAs/InP MOSFETs for potential application in VLSI circuits at scaling generations beyond 22 nm. We will report device design, review gate dielectric growth processes, and describe in detail the development of process modules for fabrication of fully self-aligned enhancement-mode devices. Key design challenges include the effect of the low density of states upon drive current and the effect of the low carrier mass on vertical confinement. Target electrical parameters include ~5 mA/µm drive current and ~7 mS/µm^2 transconductance. Key fabrication challenges include formation of self-aligned N+ source and drain contacts with < 15 Ω–µm and < 1 Ω–µm^2 resistivity, and the formation and patterning of the gate metal and dielectric without damage to the thin underlying 4-6 nm channel layer.**

I. INTRODUCTION

SILICON MOSFETs continue to scale, and in production have reached 45 nm lithographic half-pitch [1]. In developing future scaling generations with yet shorter gate lengths L_g, to maintain a constant g_m / G_{ds} ratio, constant drain-induced barrier lowering ratio DIBL, and a proportional reduction of all device capacitances for a device of a given on-state current, the gate capacitance density $c_g = \varepsilon_{ox} / T_{ox}$ must be progressively and proportionally increased. Continued difficulties faced in further increasing $\varepsilon_{ox} / T_{ox}$ have encourage the investigation of the potential benefits of employing materials other than Silicon for the MOSFET channel [2, 3, 4, 5].

Several III-V compound semiconductor materials, specifically $In_{0.53}Ga_{0.47}As$ or (strained) $In_xGa_{1-x}As$ grown at the lattice constant of InP, and InAs at grown at the lattice constant of AlSb, show both very low electron effective masses m^* and large intervalley energy separations ($E_{\Gamma-L}$, $E_{\Gamma-X}$) between the primary low-effective-mass (Γ) and satellite higher-mass (L and X) valleys. The low m^* results in high electron velocities v under low applied fields, while the low Γ-valley density of states and the large intervalley energy separations result in high electron velocities under high applied fields.

Decreasing m^* increases the electron velocity, and under the questionable assumption of fixed control region charge density qn_s, increases the device on-state current $I_d = qn_s v W_g$ for a device of a given gate width W_g. Because the transistor is embedded in several extrinsic and wiring capacitances all proportional to W_g, this increased I_d / W_g reduces the capacitance charging times in logic gate operation. Independent of the effect upon qn_s, increasing the electron velocity reduces the carrier transit time $\tau = L_g / v$ under the gate, reducing the portion $C_{gs,\tau} = \tau \cdot (\partial I_D / \partial V_{gs})$ of the gate-source capacitance associated with the charge-control region.

Because replacing the Si channel with $In_xGa_{1-x}As$ might improve performance, the technology warrants detailed investigation. Decreased m^* unfortunately introduces several serious difficulties into device design [6, 7], and constrains the range of $T_{ox,eq}$ over which performance is improved. Additionally, to fabricate a MOSFET of the required performance, the required device structures, hence process flows, must differ considerably from those of present III-V HEMTs. These two issues will be addressed in detail below. In addition, high-ε_r gate dielectrics with low interface state densities D_{it} must be developed for III-V materials [8], and processes must be developed to grow III-V channel materials on Si substrates. These major issues we will not here address.

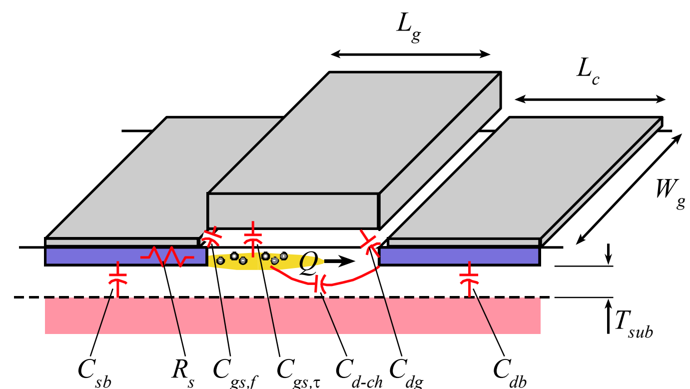

Figure 1: Idealized MOSFET for scaling analysis.

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II. FET SCALING

Consider FET scaling [9, 10, 11] in the constant-voltage, constant-velocity limit (Figure 1), neglecting for the moment the effects of a finite density of states. In scaling for $\gamma:1$ increased circuit bandwidth, we must then reduce by $\gamma:1$ all capacitances and all transport delays while keeping constant all resistances, voltages, and currents. We will calculate all parameters normalized to W_g.

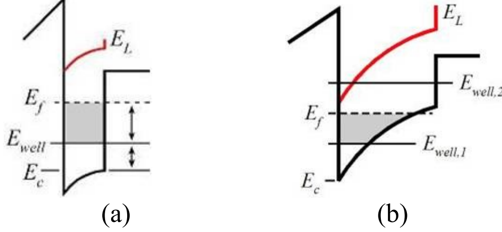

Figure 2: Band diagrams of (a) heterojunction-confined ("square") vs. (b) electrostatically-confined ("triangular") quantum wells. In either situation, because the centroid of the electron wavefunction is close to the surface, only the first well eigenstate lies in energy below that of the satellite (L and X) valleys. The Fermi level must be kept below E_L and E_X to avoid populating these lower-mobility valleys.

The device has transconductance $g_m/W_g \approx v\varepsilon_{ox}/T_{ox}$ and intrinsic gate capacitance $C_{gs,\tau}/W_g = \varepsilon_{ox}L_g/T_{ox}$. Reducing alone L_g by $\gamma:1$ would decrease the time constant $C_{gs,\tau}/g_m$. Considering below both the voltage gain (g_m/G_{ds}) and the parasitic device capacitances, we will find that W_g and T_{ox}/ε_{ox} must be proportionally reduced.

Consider first the output conductance G_{ds}. With fringing [12] capacitive coupling of order $C_{d-ch}/W_g \approx \varepsilon_{channel}$ between the drain electrode and the channel transport charge , $G_{ds} = C_{d-ch}/\tau$, hence $g_m/G_{ds} \approx \varepsilon_{ox}L_g/\varepsilon_{channel}T_{ox}$. As gate length is reduced $\gamma:1$, T_{ox}/ε_{ox} be reduced by the same proportion. To maintain constant g_m, W_g must then be reduced $\gamma:1$. The electrostatics of drain-induced barrier lowering (DIBL) are similar to those associated with the g_m/G_m ratio, and the two show similar trends.

Similar constraints are found when parasitic capacitances are considered. Even in the idealized case of zero overlap between the N+ source and drain regions and the gate electrode, there are at minimum fringing capacitances between gate and source of $C_{gs,f}/W_g \approx \varepsilon_{ox}$ and between gate and drain of $C_{gd}/W_g \approx \varepsilon_{ox}$. To reduce these capacitances in the desired proportion, W_g must be reduced by $\gamma:1$. Maintaining constant g_m and I_D then again forces a proportional reduction in T_{ox}/ε_{ox}.

Similar considerations apply when we consider the capacitances from the source and from the drain to the bulk (Figure 1), $C_{sb}/W_g \approx C_{db}/W_g \approx \varepsilon_{sub}L_c/T_{sub}$, as IC layout density will constraints will force $L_c \propto L_g$ and process design will force $T_{sub} \propto L_g$. Note that in HEMTs, where the substrate is undoped, C_{sb} and C_{db} are not present, there is instead a drain-source capacitance $C_{ds}/W_g \cong \varepsilon_{sub}$. In all these cases, reduction in the substrate capacitances forces a $\gamma:1$ reduction in W_g while maintaining constant g_m and I_d, hence requiring that g_m/W_g and I_D/W_g increase with scaling as $\gamma:1$. As IC wire lengths vary as the square root of the transistor die area, increased I_D/W_g is also desired for decreased charging times for the wiring capacitances.

IC layout density constraints suggest that the contact length L_c should decrease at the same rate as L_g. Because g_m/W_g and I_D/W_g vary as $\gamma:1$, to maintain constant R_S the normalized source /drain contact resistivity $\rho_c = R_S/W_gL_c$ must vary in proportion to $1/\gamma^2$.

Because of gate leakage by tunneling, T_{ox}/ε_{ox} has not been reduced in proportion to L_g for several scaling generations. In addition to degraded g_m/G_{ds} and DIBL, the transport capacitance $C_{gs,\tau}$ becomes a progressively smaller fraction of the total device capacitance. Transport delay τ and current-gain cutoff frequency f_τ become progressively less useful measures of device performance.

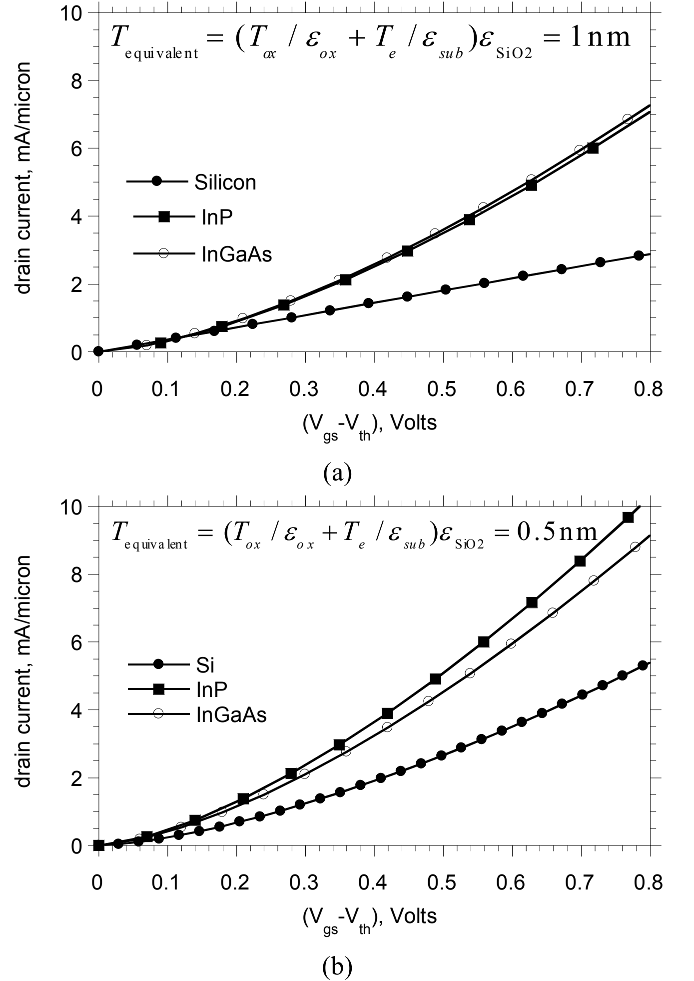

Figure 3: Simplified DC FET characteristics calculated in the ballistic limit. (a) InGaAs, InP, and Si devices at 1 nm equivalent oxide thickness. The InGaAs and InP characteristics are approximated using degenerate statistics at 0 K, while the Si characteristics are approximated using nondegenerate statistics at 300 K. (b) Devices at 0.5 nm equivalent oxide thickness, all approximated using degenerate statistics at 0 K. The stated EOT includes contributions both from the gate dielectric and from the nonzero electron wavefunction depth T_e.

III. Benefits & Limitations of low-m* channels

The benefit of a low-m* material is more due to increased thermal $v_{th} = (kT/m^*)^{1/2}$ or Fermi velocity -- $v_f = [2(E_f - E_c)/m^*]^{1/2}$ at zero Kelvin -- than it is due to high mobility. Although increased mobility will reduce resistance in the access regions, it is of marginal benefit in the transport through channels of very short gate length. In particular, from a simple drift-diffusion analysis in the nondegenerate limit, the drain current is approximately

$$I_d \approx (\varepsilon_{ox}/T_{ox}) v_{exit} W_g \, (V_{gs} - V_{th} - v_{exit} L_g / \mu_n) \qquad (1)$$

for $(V_{gs} - V_{th}) >> v_{exit} L_g / \mu_n$. Here, the channel exit velocity v_{exit} into the high-field region is v_{th}. From (1), it is sufficient to maintain a mobility $\mu_n >> v_{exit} L_g /(V_{gs} - V_{th})$. In particular, for an InGaAs channel, if $(V_{gs} - V_{th})$=0.7 V, v_{exit}=$3.3 \cdot 10^7$ cm/s and L_g= 22 nm, μ_n=1300 cm^2/V·s results in I_d only 10% below that which would result from infinite mobility. The benefit of low m^* is in increased v_{th} or v_f, and only to a lesser extent in increased μ_n

Low-m^* channels provide shorter transit times τ but bring increased drive current only if T_{ox}/ε_{ox} cannot continue to scale. We now consider this in detail.

First consider vertical scaling (Figure 2). Given a finite depth T_e of the centroid of the electron wavefunction, the gate capacitance density c_g becomes $1/c_g = T_{ox}/\varepsilon_{ox} + T_e/\varepsilon_{sub}$; the wavefunction must be kept close to the surface. The channel can be confined vertically by electrostatics, by a heterojunction, or by the two in combination. In all cases, the bound state energy ($E_{well,l} \sim \hbar^2\pi^2 l^2 / 2m_e^* T_w^2$ in the heterojunction-confined, infinite-well approximation) is high and only the lowest eigenstate lies at energies well below that of the high-mass satellite valleys. With only one eigenstate filled, the (unidirectional) density of states is $dn/dE = m^*/2\pi\hbar^2$.

Following the method of Natori [13], the transistor DC characteristics can be estimated to first order in the ballistic (negligible scattering) limit. With III-V channels, m^* is low yet qn_s is high, hence the 2DEG will be highly degenerate at high gate biases, and we can neglect with only small error the effect of kT, computing charge densities and velocities at $T = 0$ K. The sheet charge density is then $qn_s = q(m^*/2\pi\hbar^2)(E_f - E_c)$. The gate-source voltage is found from $V_{gs} - V_{th} = (E_f - E_c)/q + qn_s/c_g$, while the drain current is found from $I_D / W_g = (4/3\pi) v_f \cdot qn_s$.

From this calculation the DC characteristics of Figure 3 are found. Because of the large Fermi velocity, at 1 nm total equivalent insulator thickness, InGaAs & InP channels provide much larger I_D/W_g than silicon channels. Because of the low density of states, this advantage diminished at 0.5 nm. At 0.25 nm (not feasible in InGaAs because of minimum constraints on the depth of the bound state) the Si channel provides a decisive advantage in I_D/W_g. III-V channels, then, provide a decisive drive current advantage over Si only if either oxide cannot continue to scale or if the ballistic limit cannot be approached in Si because of degraded mobility in short-gate-length devices.

The benefit of the low-m^* channel is more evident in the device capacitance. Inclusive of the finite density of states, $C_{gs,\tau} = (T_{ox}/\varepsilon_{ox} + T_e/\varepsilon_{sub} + 2\pi\hbar^2/q^2 m^*) L_g W_g$. Assume a 22 nm gate length L_g For the MOSFETs of Figure 3a, $C_{gs,\tau}/W_g$ = 0.21 fF/μm for the InGaAs channel and 0.71 fF/μm for the Si channel. For the MOSFETs of Figure 3b, $C_{gs,\tau}/W_g$ = 0.25 fF/μm for the InGaAs channel and 1.35 fF/μm for the Si channel. These numbers should be compared to expected gate-source, gate-drain fringing capacitances of ~0.3 fF/μm; with sub-22-nm gate lengths, the III-V channel devices are dominated by extrinsic parasitic capacitances, and the transport capacitance $C_{gs,\tau}$ becomes negligible. There is little benefit in further scaling the gate length

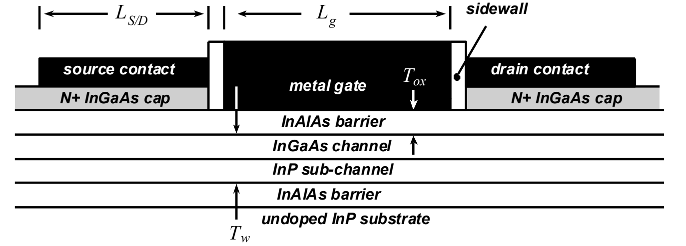

Figure 4: Cross-section of InGaAs/InP HEMT in a planar form suitable for large-scale IC fabrication.

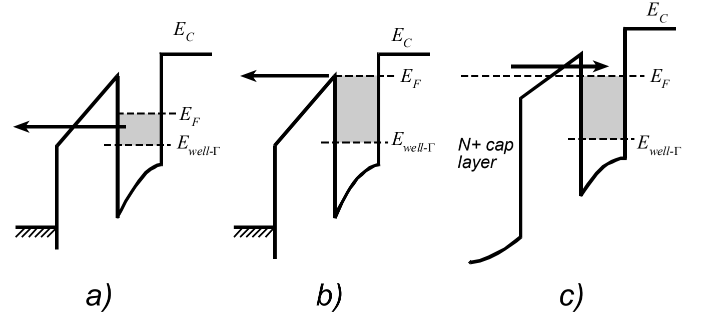

Figure 5: Band diagrams addressing transport considerations in HEMTs. Tunneling through the InAlAs gate barrier (a) sets a minimum barrier thickness. Thermionic emission over the gate barrier (b) sets a maximum feasible 2DEG sheet carrier density proportional to the band offset. Because the gate barrier also lies under the source and drain contacts (c), large gate barrier energies will increase the source and drain resistances.

The above calculations neglect non-parabolic terms in the InGaAs & InP E-k band structure, include Si band degeneracy, but neglect Si band anisotropy, treating the bands as spherical with m^*/m_e=0.36. Because the Si devices operate under conditions of weak degeneracy, DC characteristics at 1 nm thickness were computed using the thermal velocity, and for 0.5 nm thickness were computed using the Fermi velocity. More accurate treatments use Fermi-Dirac integrals [14].

The low m^* also constrains vertical scaling (Figure 2). With thin wells the combined effects of the high ground state energy ($E_{well} \sim \hbar^2\pi^2 / 2m_e^* T_w^2$ in the infinite-well approximation) and high electron density ($E_f - E_{well} \approx qn_s[2\pi\hbar^2/m^* q]$) can together raise the channel Fermi

energy to that of the L valley minimum, populating these bands and greatly reducing mobility. The low electron effective mass therefore constrains both vertical scaling and the maximum useful channel carrier density. For a 5 nm InGaAs well $n_s \sim 8\cdot 10^{12}/\mathrm{cm}^2$ [15] can be reached before significant population of the satellite valleys. This is comparable to the electron densities reached at 700 mV gate overdrive for the InGaAs-channel devices of Figure 3. Given the above constraints on the well thickness, it is not yet clear whether acceptable DIBL or g_m / G_{ds} can be obtained for devices with gate lengths shorter than 22 nm.

These scaling difficulties must also be addressed to enable development of > 1-THz-f_τ InGaAs Schottky-barrier field-effect transistors (HEMTs). Such devices would enable low-noise preamplifiers for sub-mm-wave radio receivers in the 50-500 GHz range. It should be noted that almost 17 years were required to double the bandwidth of InGaAs HEMTs [16, 17, 18], suggesting the presence of serious scaling challenges. The above analysis suggests that ~20 mS/μm as an upper limit to g_m / W_g for an InGaAs channel; this, together with extrinsic capacitances of ~0.3 fF/μm at source and drain, sets a minimum ~30 fs time constant contributing to $1/2\pi f_\tau$. Vertical scaling limits, and the effect upon g_m / G_{ds} and therefore upon $f_{\max}$, warrant detailed analysis.

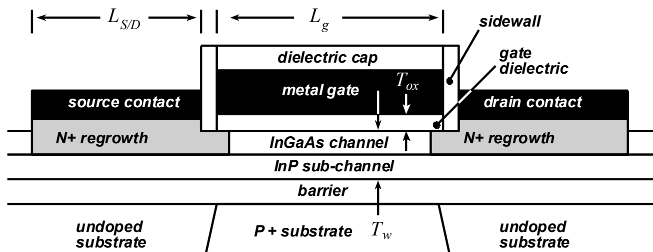

Figure 6: Cross-section of InP-based MOSFET with regrown extrinsic N+ InGaAs/InAs source and drain regions. The gate stripe extends a distance W_g perpendicular to the figure. L_g is the gate length, T_{ox} the gate dielectric thickness, and T_w the thickness of the InGaAs/InP quantum well.

IV. DEVICE STRUCTURE AND PROCESS FLOW

The device structure must now be defined and the process flow developed. The device structure must differ considerably from that associated (Figure 4) with present III-V Schottky-barrier FETs (HEMTs).

In a HEMT, the wide bandgap barrier layer placed between the channel and the gate electrode also lies under the source and drain Ohmic contacts. The barrier for a $\sim \mathrm{In_{0.5}Ga_{0.5}As} / \mathrm{In_{0.5}Al_{0.5}As}$ interface is ~0.5 eV. Larger barriers might be obtained from InAs/AlSb interfaces, but other difficulties are encountered. As in MOSFETs, tunneling through the gate barrier (Figure 5a) sets a minimum gate thickness; unlike MOSFETs, thermionic emission (Figure 5b) over the barrier sets a maximum sheet carrier density qn_s. In the source and drain regions, carriers must be conducted over this same barrier (Figure 5c), high barriers make it more difficult to obtain low access resistance.

These considerations lead us to the device structure of Figure 6, very similar to a Si MOSFET wherein wide-gap barrier layers do not lie under the source and drain. As with a MOSFET, N+ doped regions must be formed in the source and drain after gate deposition. This is a considerable challenge in III-V technology; in almost all production III-V processes, all doped regions are formed during wafer epitaxial growth, with subsequent wafer processes defining only the locations of mesas, contacts, and insulating layers.

Consider the target performance for the access regions. We seek I_D / W_g ~7 mA/μm at 700 mV gate overdrive. A source access resistance of $R_s W_g$=10 $\Omega-\mu$m would introduce ~70 mV voltage drop on the access resistance, reducing the on-state current by ~10%. If the contact width L_C=25 nm, a ρ_c = 0.25 $\Omega-\mu\mathrm{m}^2$ contact would contribute $R_s W_g = \rho_c / L_C$=10 $\Omega-\mu$m resistance. If there were a 20 nm lateral extension of N+ material between the edges of the Ohmic contact and the gate, an N+ sheet resistivity of 400 Ω would introduce an additional $R_s W_g$=4 $\Omega-\mu$m resistance.

The N+ source and drain regions can be formed, as in Si, by ion implantation after formation of the gate electrode [19]. Difficulties with implantation include intermixing during implantation of the InGaAs channel and the underlying InAlAs layer, and incommensurate sublimation of In, Ga, and As during the subsequent anneal. Both effects render it difficult to control the stochiometry and alloy composition of the implanted InGaAs channel; both effects are made more serious by the extremely low ~ 5 nm required thickness of the InGaAs channel layer.

Instead, we are developing a fabrication process which forms the N+ source/drain regions by epitaxial regrowth after gate stack formation. Figure 7 shows the overall process flow. After wafer growth by MBE, a gate oxide (Al_2O_3 or ZrO_2) is deposited by MBE or by ALD and capped by a thin metal layer which encapsulates the gate oxide and sets the gate work function. The wafer is the coated with W gate metal and encapsulated by dielectric.

The gate is then patterned by RIE, and the gate dielectric etched. Gate dielectric sidewalls are then formed by CVD conformal deposition and anisotropic RIE etching. The InGaAs channel removed by a short selective wet-etch which stops on the InP subchannel. Self-aligned N+ source and drain access regions and contacts are then formed. The regrowth process flows will be described in more detail below. Subsequent to regrowth, transistors are mesa isolated by RIE etching, vias are deposited, the wafer planarized by Benzocyclobutene (BCB) dielectric, and interconnect metal and pads deposited.

Figure 8 shows the process flow for non-selective-area source-drain regrowth. After recess etching to expose the InP subchannel, the wafer is loaded into an MBE system and N+ InGaAs grown. Without breaking vacuum, the wafer is moved to an electron-beam evaporation chamber, and Mo source/drain contact metal deposited. Contact resistivity is ~1 $\Omega-\mu\mathrm{m}^2$. The regrown N+ InGaAs and Mo contact metal cover the gate, short-circuiting the source and drain. These

layers are removed over the gate by planarizing the wafer with photoresist and subsequently etching. Mo contact metal has high sheet resistivity. We are developing a process for self-aligned Au contact metal deposition by electroplating, although present devices used optically aligned and lifted-off Au metal.

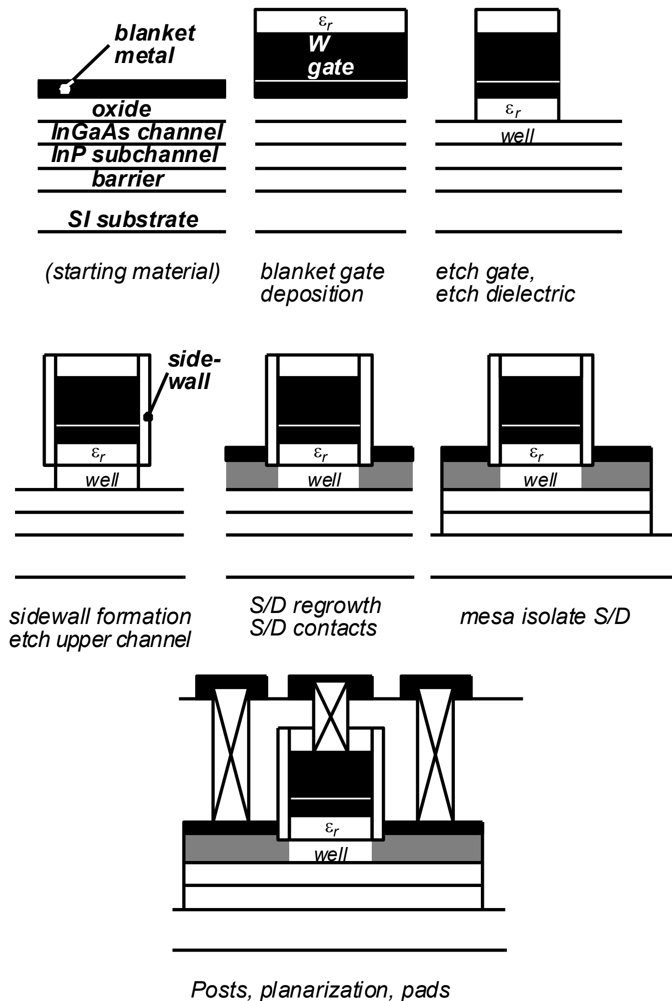

Figure 7: Process flow for formation of the III-V MOSFET.

Figure 9 shows the process flow for formation of the N+ source and drain regions by selective-area regrowth by chemical beam epitaxy. The InGaAs source and drain regions are then grown on the InP sub-channel; with CBE, polycrystalline growth does not initiate on the gate dielectric cap or sidewalls. Subsequent to S/D regrowth, blanket contact metal is deposited, and is removed over the gate electrode by planarizing and etching. Further self-aligned S/D contact metals can then be deposited by electroplating.

Process modules have been developed for the gate stack and sidewalls, for source/drain contacts, and for the interconnect back-end steps. Figure 10 shows a completed device. Functioning devices have been fabricated, albeit with very low on-state current density resulting from a high access resistance believed to originate from failure of the non-selective regrowth to under fill the recess regions. Process development is ongoing in both the selective-area and non-selective area process, and results will be reported both at this conference and elsewhere.

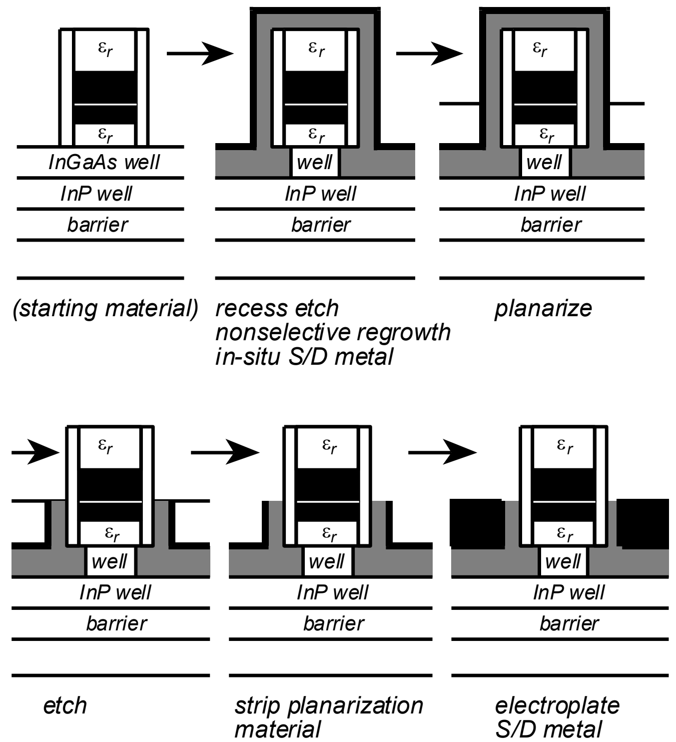

Figure 8: Process flow for non-selective-area N+ source/drain regrowth by MBE.

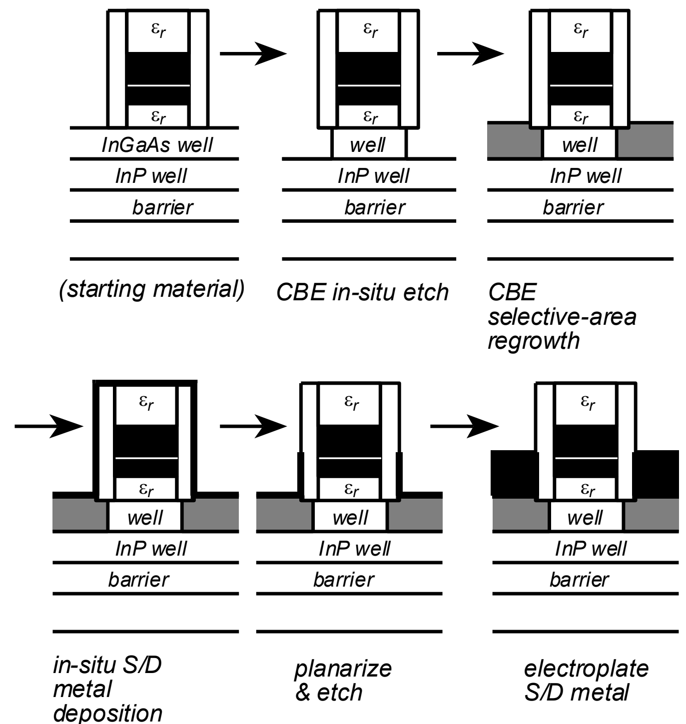

Figure 9: Process flow for selective-area N+ source-drain regrowth by chemical beam epitaxy (CBE)

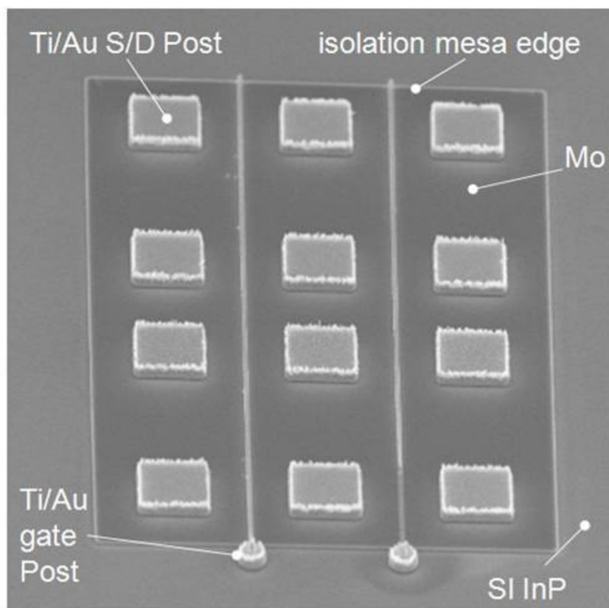

Figure 10: SEM of completed III-V MOSFET with non-selective-area MBE regrowth of the N+ source and drain regions.

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